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FPGA-Based Hardware Accelerators for 10/40 GigE TCP/IP and Other Protocols

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FPGA in MicroTCA systems not only offer efficient implementations of various I/O interfaces.
FPGA cards can also serve as high-performance, low-latency and low-power data processors to offload compute intensive tasks from CPUs.
Today's networking protocol implementations typically are software-based and, therefore, exhibit milliseconds of latency. At the same time, the packet handling puts a high load onto the CPU. At
line rates of 10 GigE, or faster, this limits performance and causes additional latencies. TCP/IP Offload engines which are state-of-the-art in server technology offer help and, with the advent of
programmable SoCs and FPGAs, become feasible for MicroTCA systems acceleration.
We will introduce a new technique that uses hardware-acceleration of networking protocol stacks, specifically targeted for MicroTCA Systems. By being able to optimize for a specific application
and its underlying network protocols, we can go beyond a state-of-the-art TCP/IP Offload Engine (TOE) and, thereby, can reach userspace latencies faster than 1 microsecond and be much closer to
the theoretical bandwidth limits.
Typically, to the implementor the burden is the significant efforts when implementing Network protocols in VHDL or Verilog. However, High-Level Synthesis, where an FPGA can be designed starting from a C, C++, or SystemC description, recently became a very valid and efficient design flow option. Our talk focuses on methodologies suitable for protocol and streaming media designs and how to use automatic synthesis of interfaces such as AXI-4 Lite and AXI-4 Stream Interfaces,
or simple FIFO and Memory access.

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