



RF-Generator for MTCA.4

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- Some informations about SINTEC
- SAMC-DDS1400
 - Main Features
 - Measurements on Prototype V1.0
 - Next steps in development



- SINTEC Microwave Systems GmbH was established in 1996
- SINTEC has a staff of 4 engineers out of 8 employees
- SINTEC focusses on the design and development of RF and microwave systems for the communication- and space business as well as for defence systems in the frequency range up to 40GHz
- SINTEC is ISO9001-2008 certified



All major steps of the product development process are located inhouse:

- System and circuit simulation with Agilent Genesys
- Circuit layout with Altium designer
- Mechanical 3D-design with PTC Creo Elements
- PCB assembly with stencil printer and automated pick and place machine
- PCB soldering using a vapour phase
- Bare die assembly using a semiautomatic wedgebonder
- Automated Optical Inspection (AOI) system for PCB assembly quality control
- Test facilities including Spectrum Analyzer, Vector Network Analyzer, Signal Source Analyzer (SSA) Noise Figure Meter and several Power Meters up to 40 GHz and 50 GHz for the SSA
- PC controlled temperature and climate chambers for system characterisation and reliability tests from -40°C up to +180°C

Product Photo

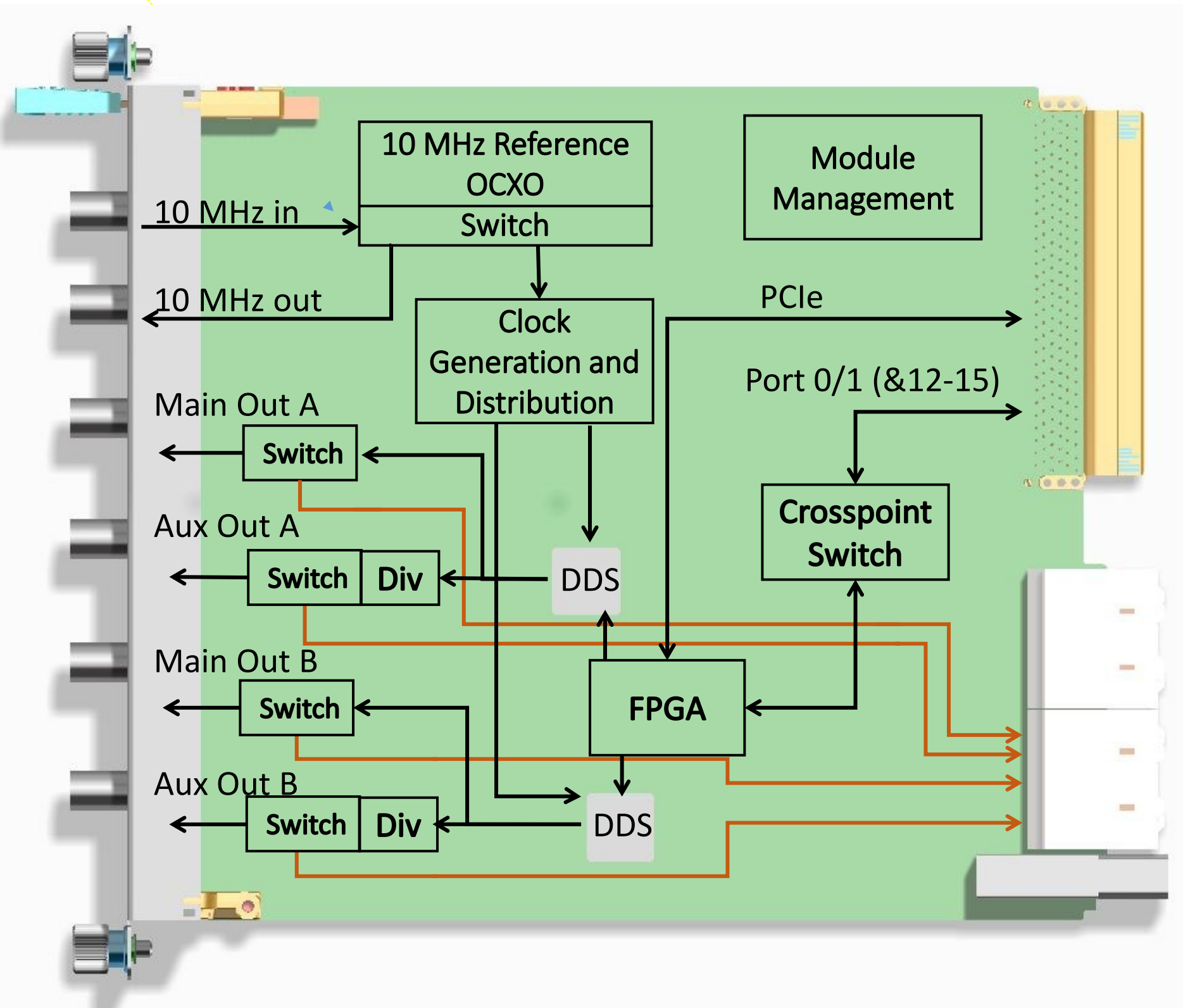


Main features



- 2 main outputs from 10 MHz to 1400 MHz
 - Frequency tuning resolution to 190 pHz
 - Output power range: -50 .. +10 dBm in 0.1 dB steps
 - Output modes: CW, triangle, sawtooth, chirp, frequency hopping
 - 2 auxiliary outputs: divided from main outputs with /1 to /32
- Internal or external 10 MHz reference source
 - 10 MHz output
- The main and auxiliary outputs can be connected to the RTM connector via switches

Block Diagram

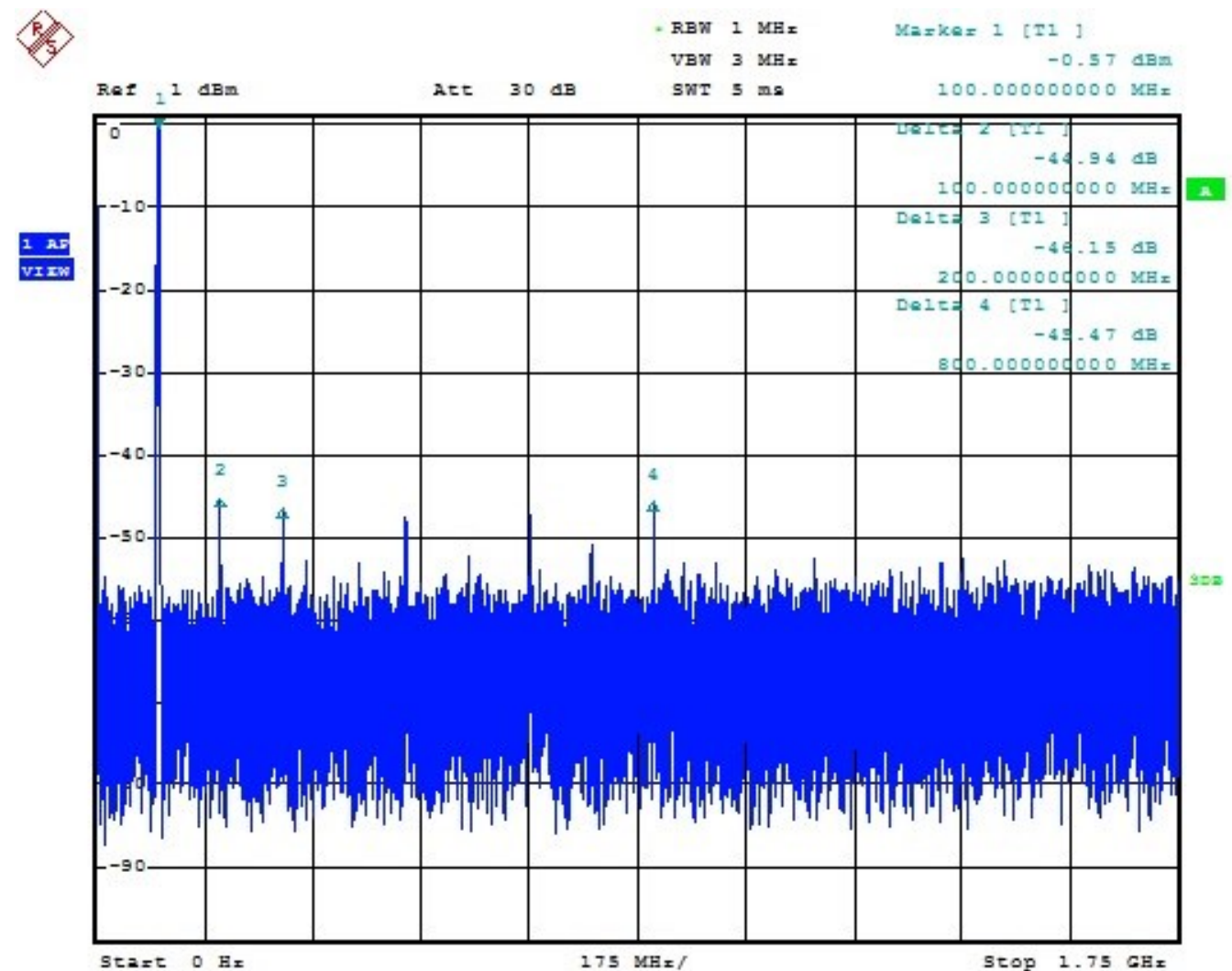
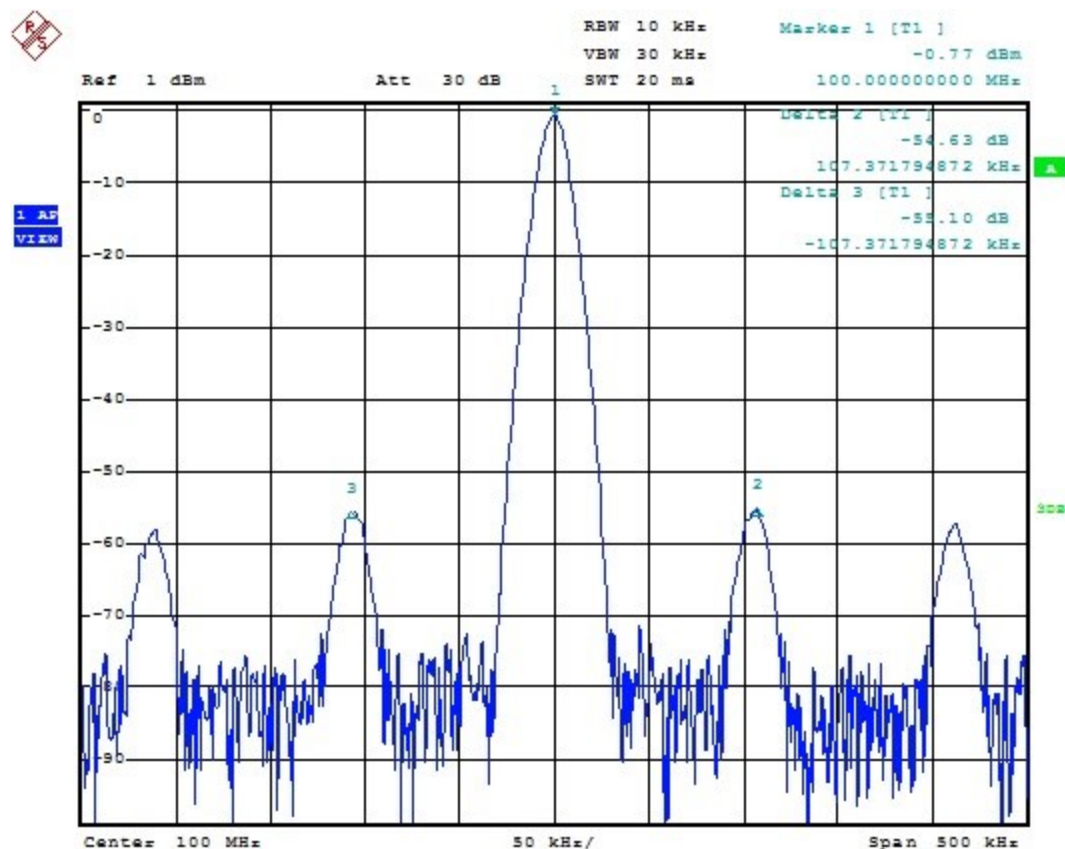




- DDS
 - AD9914: 3.5 GSPS Direct Digital Synthesizer with 12-Bit DAC
 - Frequency tuning resolution to 190 pHz
 - 16-bit phase tuning resolution
 - 12-bit amplitude scaling
 - 8 frequency/phase offset profiles
- 3.5 GHz Clock
 - 875 MHz VCSO locked to a 10MHz reference clock
 - frequency doubler, amplifier and filter

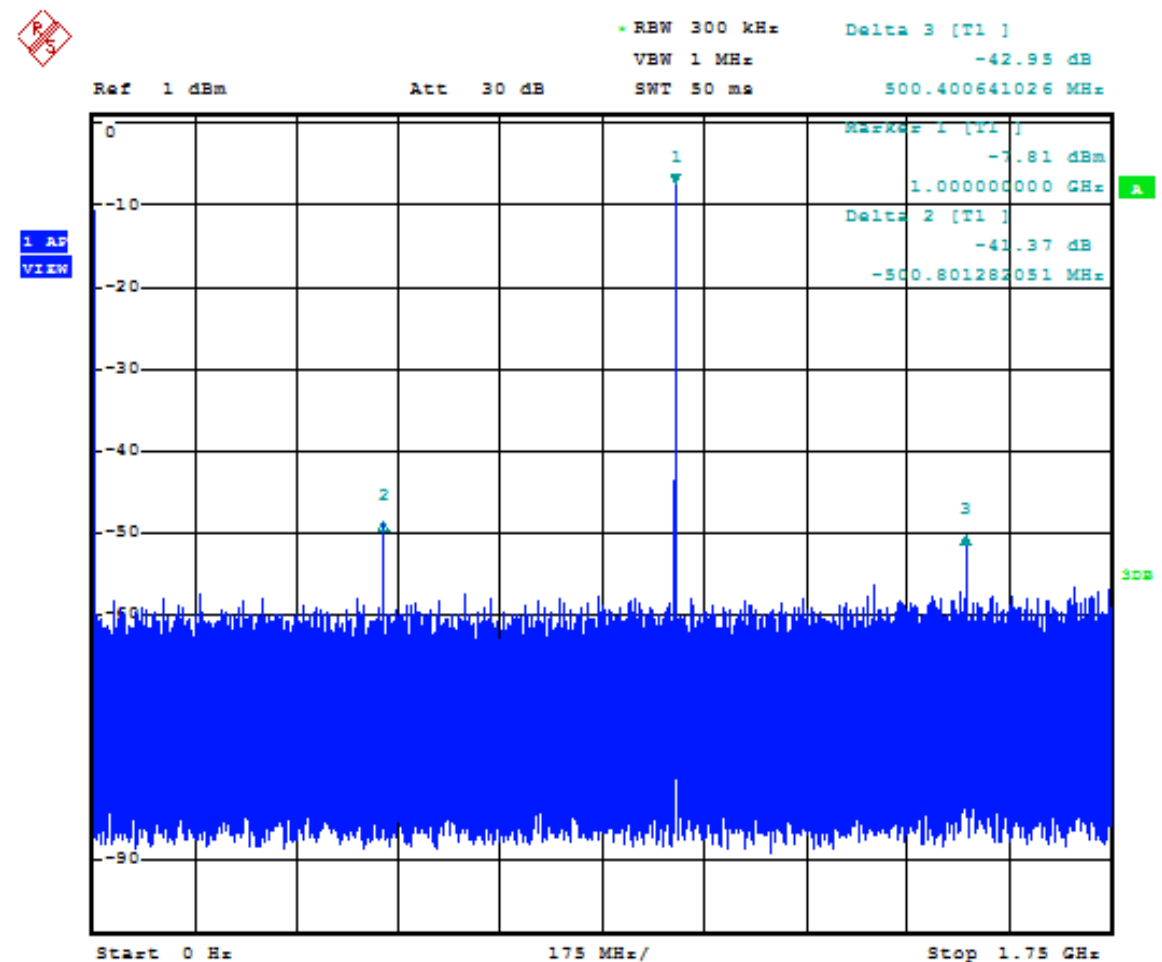
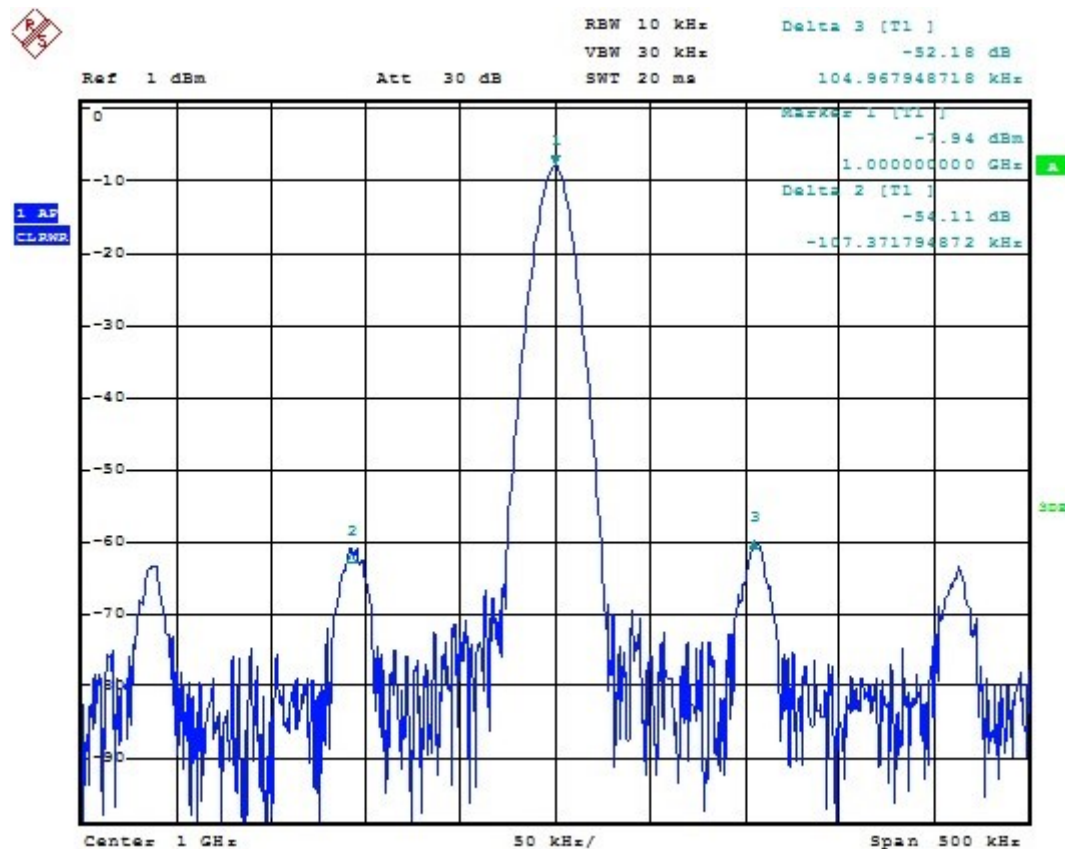


- CW-Signal
 - 100 MHz @ 0 dBm
 - Range: 0 MHz to 1750 MHz
 - Harmonics < -40 dBc
 - Spurious < -50 dBc



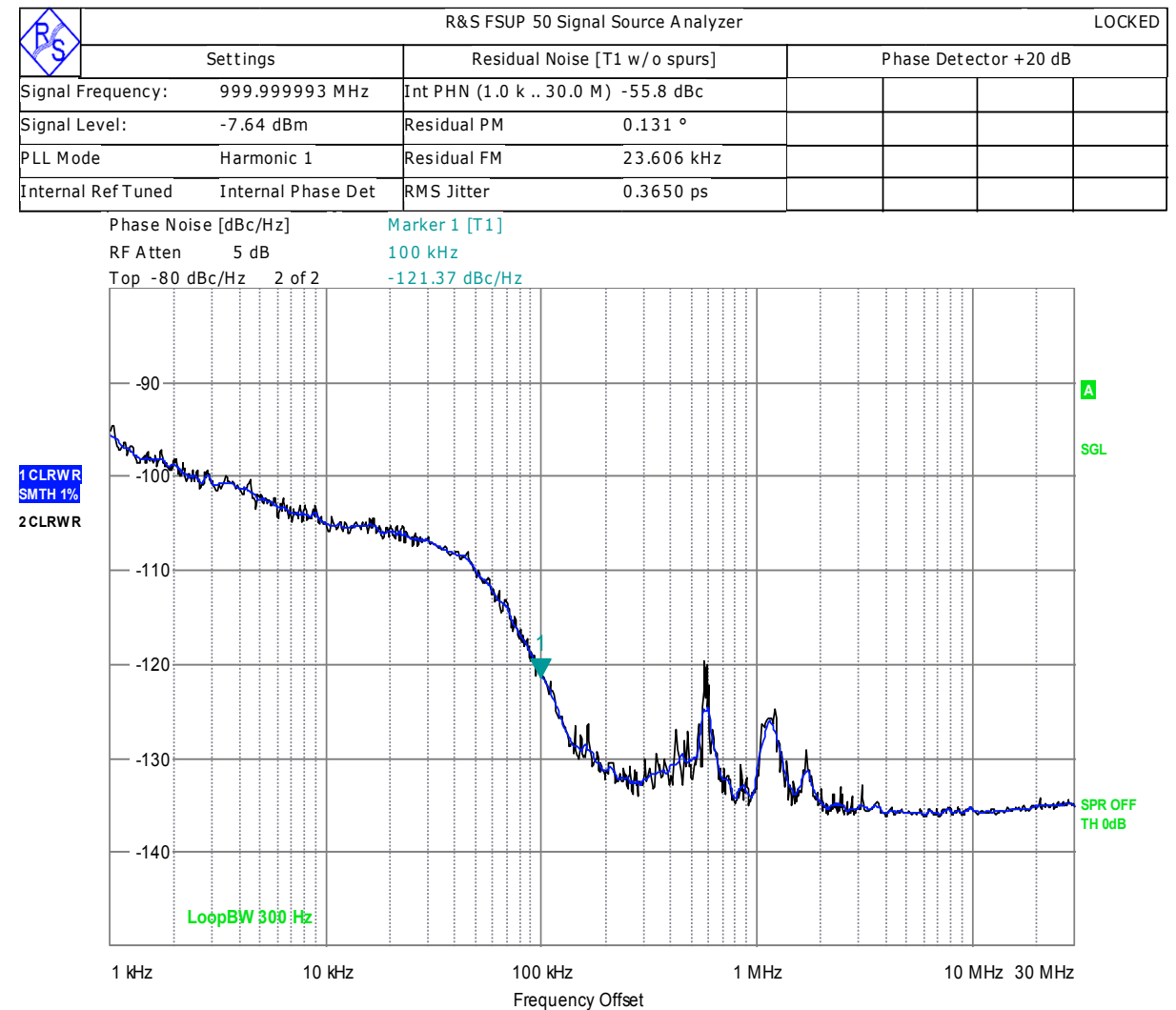


- CW-Signal
 - 1000 MHz @ 0 dBm
 - Range: 0 MHz to 1750 MHz
 - Spurious < -40 dBc
 - Optimization in next Rev. for power and spurious





- Phase Noise:
 - 1000 MHz @ 0 dBm
 - 1 kHz to 30 MHz
 - < -120 dBc/Hz @ 100 kHz
 - 365 fs RMS Jitter
- Goal for next revision:
 - < 200 fs RMS jitter



Next Steps



- Next board revision in Q1/2016
 - Optimisation regarding phase noise and spurious
 - FPGA on board instead of FPGA module
 - New Zone 3 connector (for RF)
 - Changes in mechanical design
 - Shielding box for RF isolation
- After internal test useable for beta test field user as preview version



Thank you for your attention

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