SP Devices





# New SP Devices MTCA Digitizers designed for medium speed applications in Physics

## 4th MTCA WORKSHOP

SP Devices

PCI Express

PXI Express

Micro-TCA.4

USB3.0

# Status review

# PROVEN HARDWARE CONCEPTS

| Product | Res. | Num. Ch. | Sample Rate | ADX Inside | DBS Inside | Analog BW | Offset | Interface | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | USB3 | PCIe | MTCA | PXIe |
| ADQ108 | 8 bit | 1 | 7 GS/s | ✓ | | 2 GHz | Fixed | ✓ | ✓ | ✓ | ✓ |
| ADQ1600 | 14 bit | 1 | 1.6 GS/s | ✓ | ✓ | 750 MHz | Fixed | ✓ | ✓ | ✓ | ✓ |
| ADQ412 | 12 bit | 4 | 1 GS/s | | | 2 GHz | Fixed | ✓ | ✓ | ✓ | ✓ |
| ADQ412 | 12 bit | 2 | 2 GS/s | ✓ | | 1.3 GHz | Fixed | ✓ | ✓ | ✓ | ✓ |
| ADQ412-3G | 12 bit | 4 | 1.8 GS/s | | | 2 GHz | Fixed | ✓ | ✓ | ✓ | ✓ |
| ADQ412-3G | 12 bit | 2 | 3.6 GS/s | ✓ | | 1.3 GHz | Fixed | ✓ | ✓ | ✓ | ✓ |
| ADQ412-4G | 12 bit | 4 | 2 GS/s | | | 2 GHz | Fixed | ✓ | ✓ | ✓ | ✓ |
| ADQ412-4G | 12 bit | 2 | 4 GS/s | ✓ | | 1.3 GHz | Fixed | ✓ | ✓ | ✓ | ✓ |
| ADQ412AC-4G | 12 bit | 4 | 2 GS/s | | | 1.5 GHz | Variable | ✓ | ✓ | ✓ | ✓ |
| ADQ412AC-4G | 12 bit | 2 | 4 GS/s | ✓ | | 1 GHz | Variable | ✓ | ✓ | ✓ | ✓ |

VOLUME DEPLOYED PRODUCT

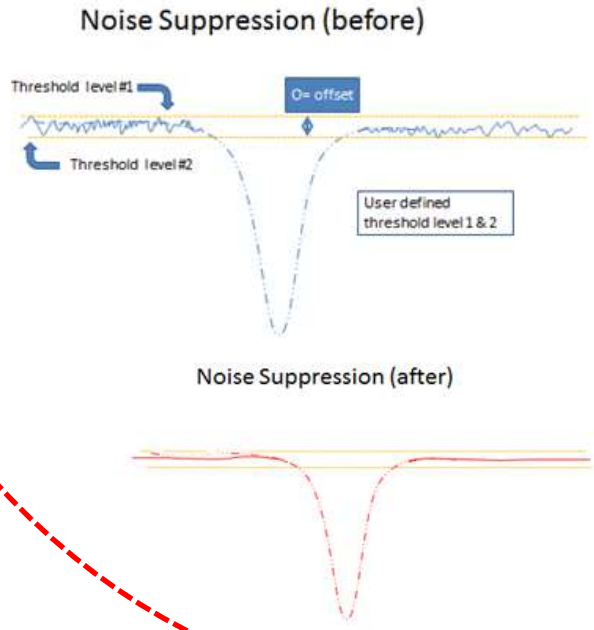
## ADQ V6 Series available in double width, mid-size AMC.0 MTCA.4 form factor

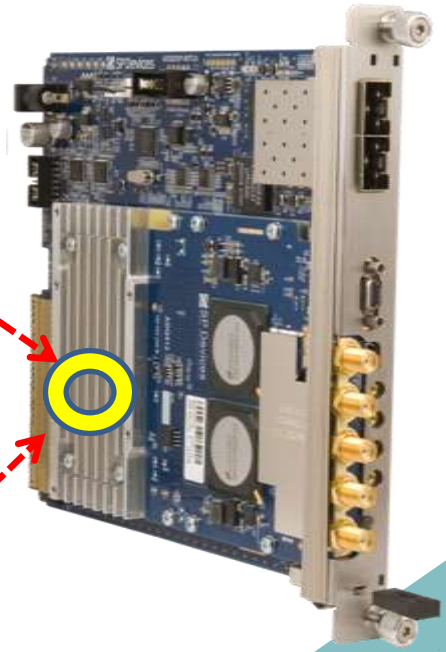
# PROVEN DIGITAL ARCHITECTURE

## Embedded processing evolution: from scratch to…

***Example of embedded processing:***

- *Noise suppression*
- *Zero suppression*
- *Digital filtering*
- *Peak detection*
- *SSD storage*



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# ADQ14

## NEW PLATFORM/ NEW TECHNOLOGIES

# NEW ADQ14 SERIES

## The hub in the application

**Connections for an efficient real-time system**


AFE
AFE
AFE
AFE

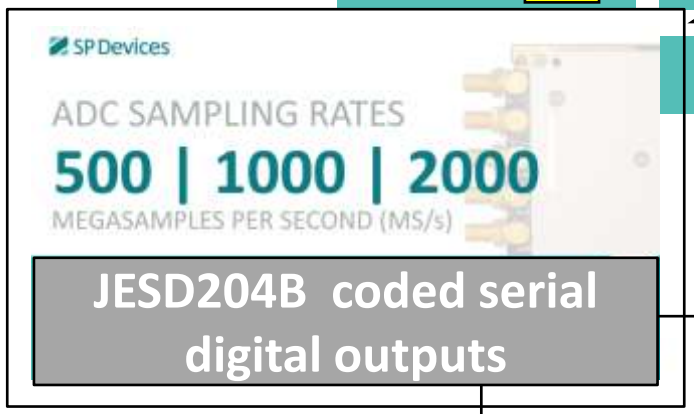
ADC
ADC
ADC

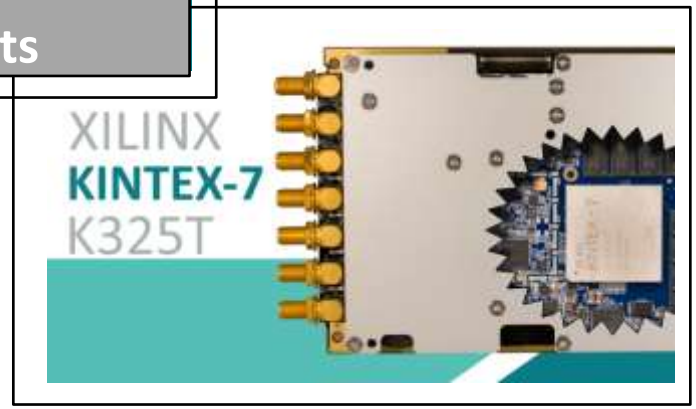
FPGA
ADX
DBS
OPEN FPGA

USB3.0
PCIe G2x8
MTCA
DRAM

TRIGG

LTI-UNIT SYNC

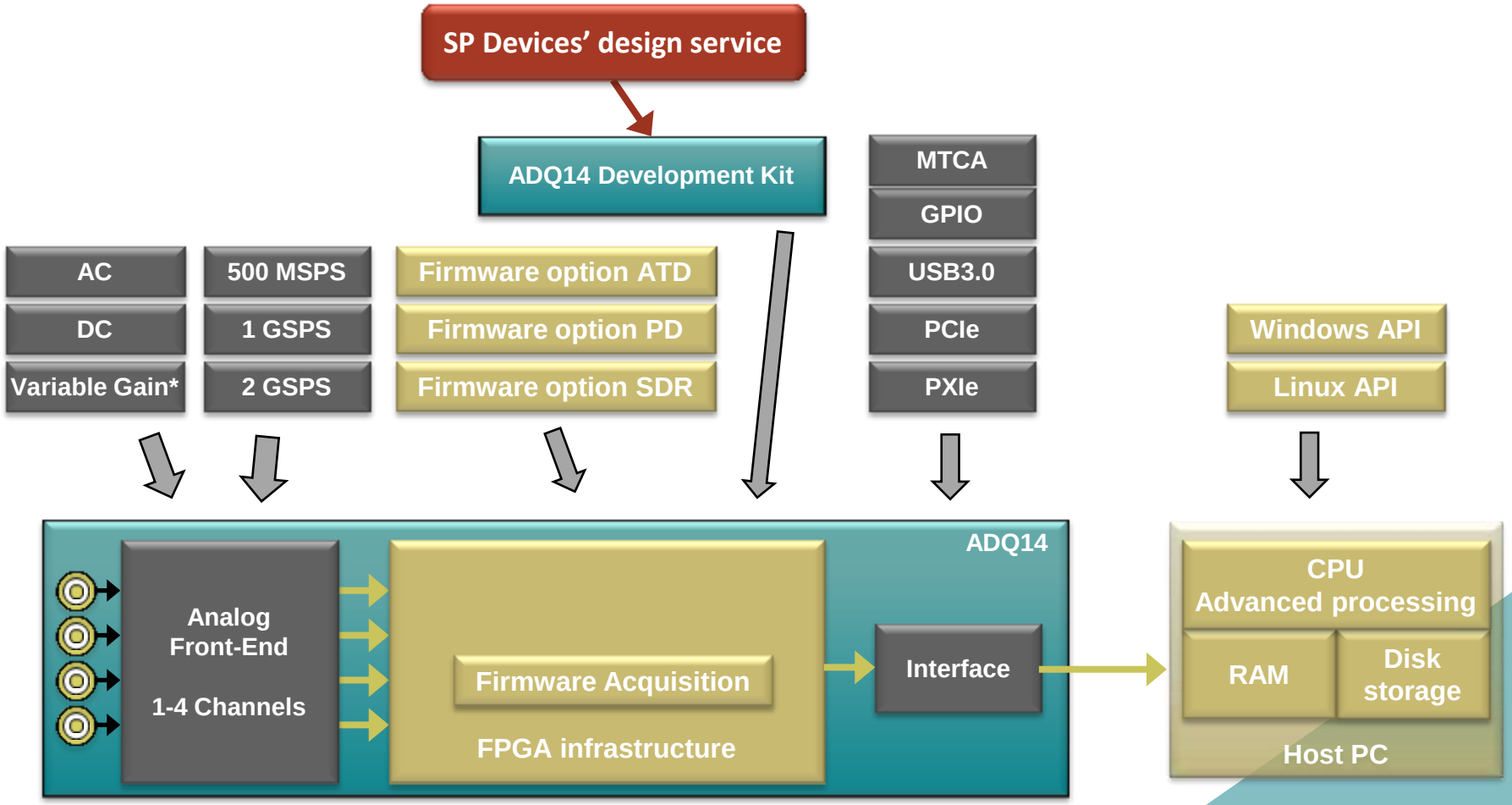


# NEW ADQ14 SERIES

## ADQ14, a flexible platform

One solution for all measurement tasks




**Select options to meet a specific demand.**

* ADQ14DC only

# ADQ14 OVERVIEW

## ADQ14, a new 14-bit digitizer family

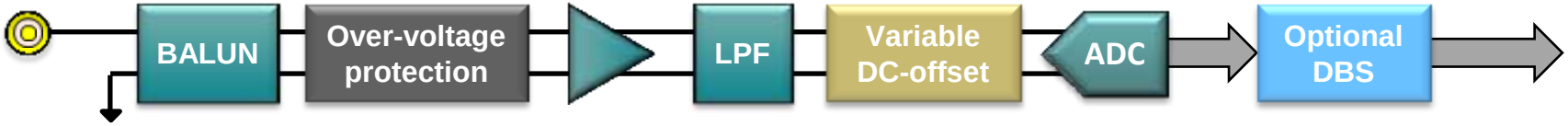
### DC-coupled analog front-end option

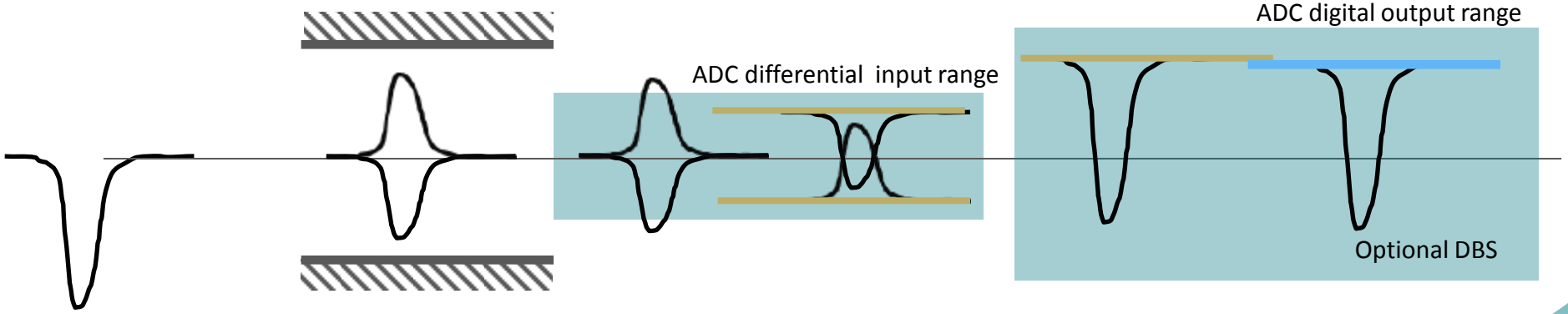
| Product | Res. | Num. Ch. | Sample Rate | ADX Inside | DBS Inside | Analog BW | Multi unit sync | Interface | | | | Firmware | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | USB3 | PCIe | MTCA | PXIe | DAQ | ATD | PD | RF |
| ADQ14DC-4C | 14 b | 4 | 1 GS/s | | ✓ | 700 MHz | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| ADQ14DC-2X | 14 b | 2 | 2 GS/s | ✓ | ✓ | 1.2 GHz | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

- Xilinx Kintex7 FPGA
- ADQ14 Development Kit opens the FPGA
- 50Ω
- DC-coupling
- Variable DC-offset
- Trigger in/out


# ADQ14DC analog front-end

## Pulse capture with variable bias and Digital Baseline Stabilizer




Input signal single-ended; most common source output. 50 ohms termination.

Differential for signal integrity.

Overvoltage protection.

DC-coupled buffer and anti-aliasing filter for noise reduction.

User controlled DC-offset to use entire signal range into ADC.

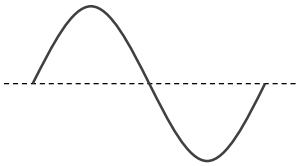
Digitized signal.

Baseline is locked to a user defined level by DBS. Suppress low frequency noise and temperature drift.

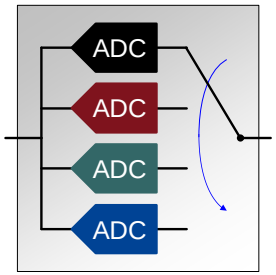
# ADQ14 DIGITIZER

## ADX interleaving technology

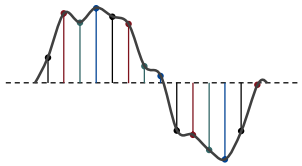
### SP Devices' technology for signal quality enhancement



High frequency input signal

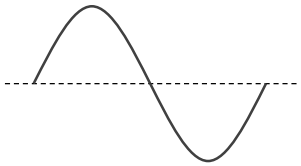



Interleaved ADCs for high sample rate

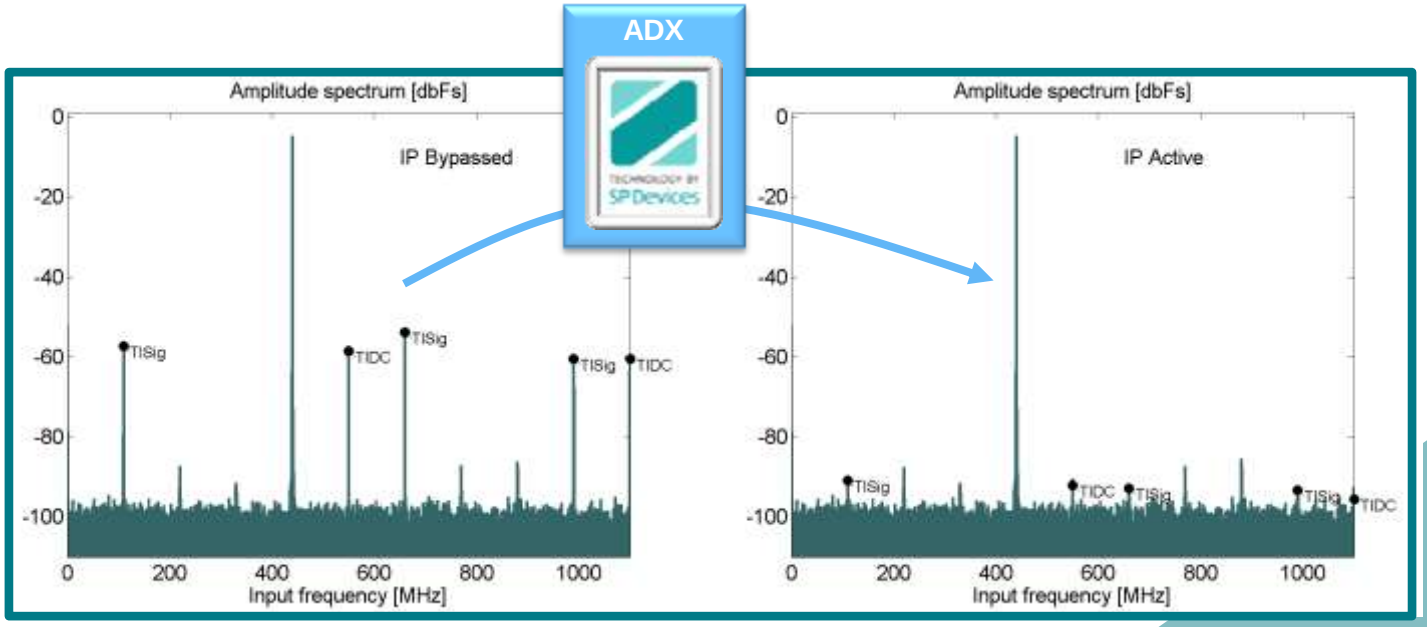


Typical distorted time-interleaved signal


ADX* corrects for time-interleaving



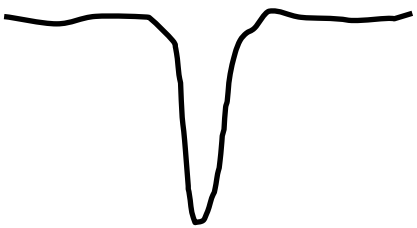
Signal restored by ADX



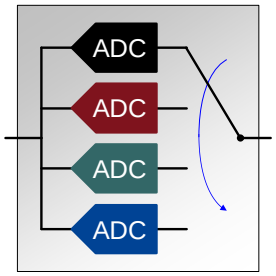

* ADX is included on interleaved ADQ14 at 2 GSPS

# DBS interleaving technology

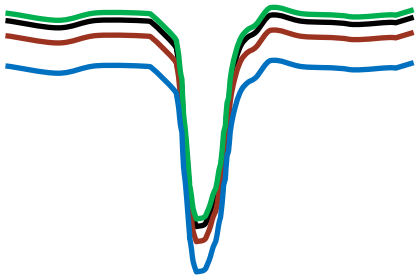
## SP Devices' technology for digital baseline stabilization



High frequency input signal

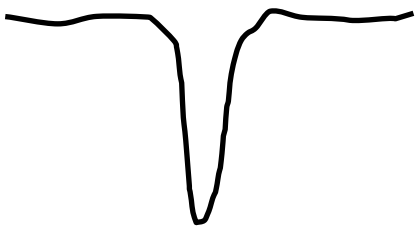



Interleaved ADCs for high sample rate



Typical distorted time-interleaved signal


DBS * corrects for base-line differences



Signal restored by DBS

* DBS is included in the standard firmware ADQ14-FWDAQ and in the firmware packages for pulse data; ADQ14-FWATD and ADQ14-FWPD

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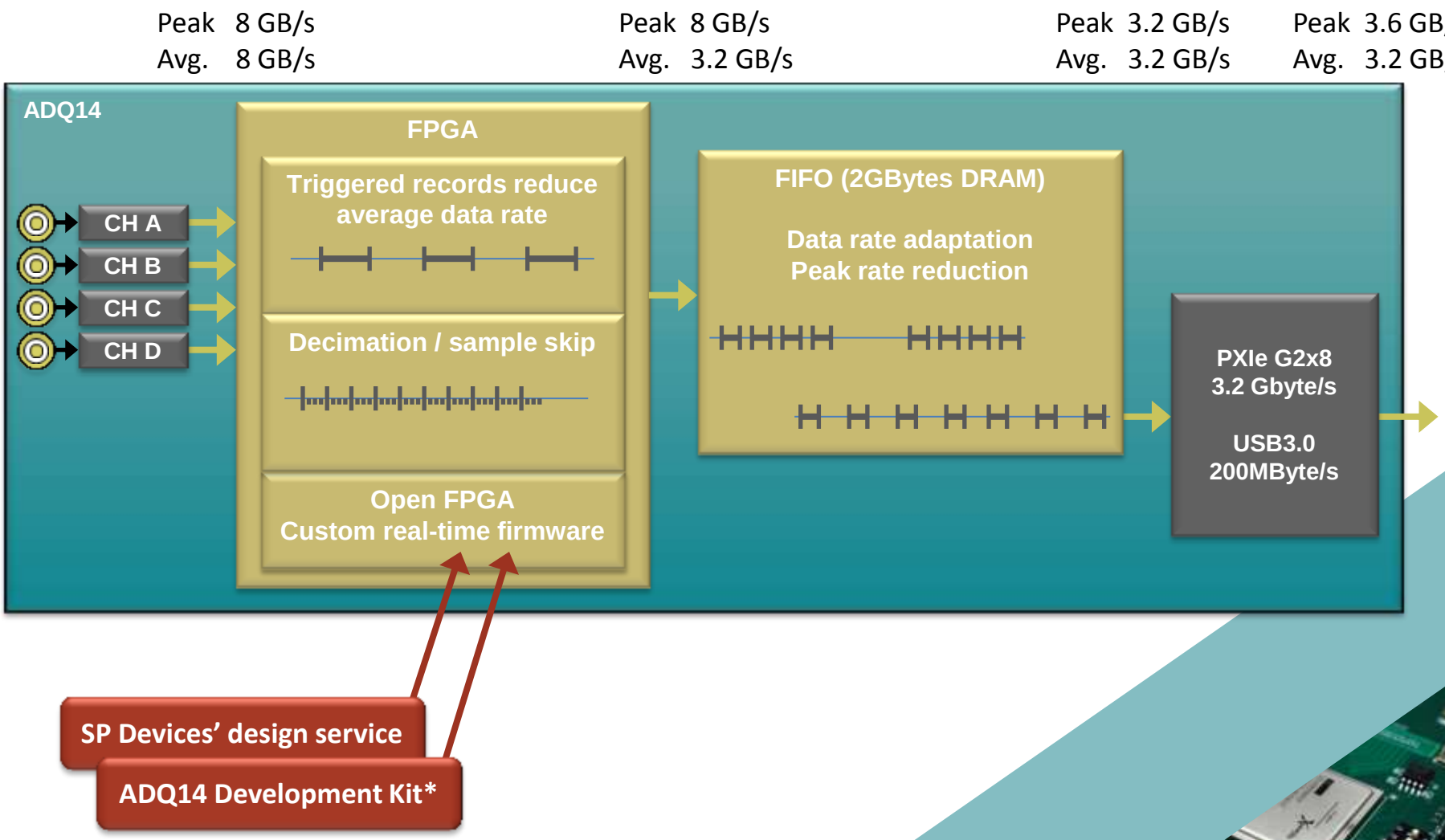
# ADQ14
## SYSTEMS DESIGN

# System design

## Data rate reduction basics



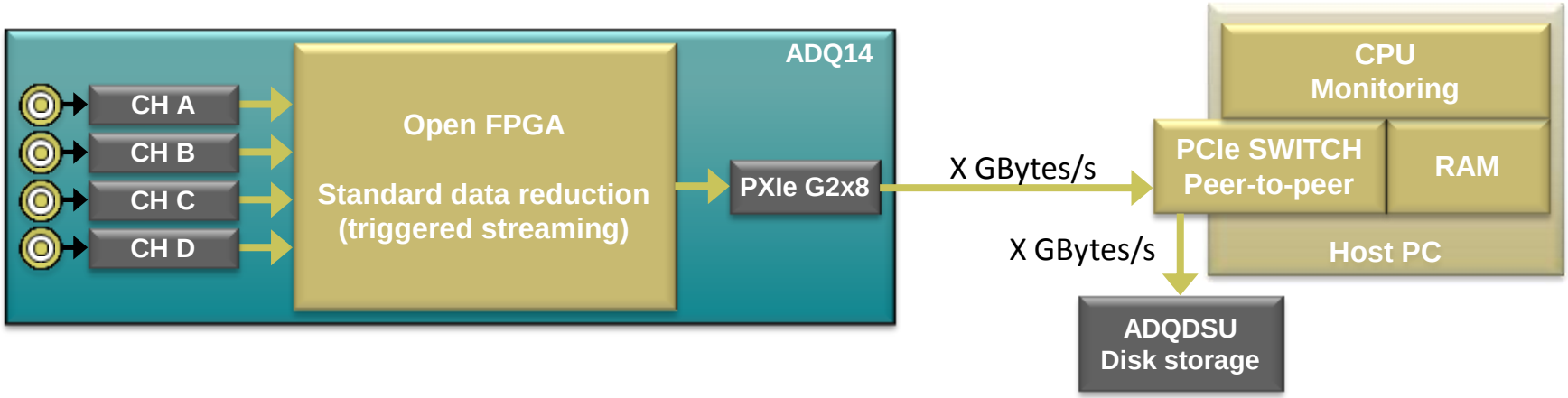

* ADQ14 Development Kit is purchased separately

# ADQ14 DIGITIZER

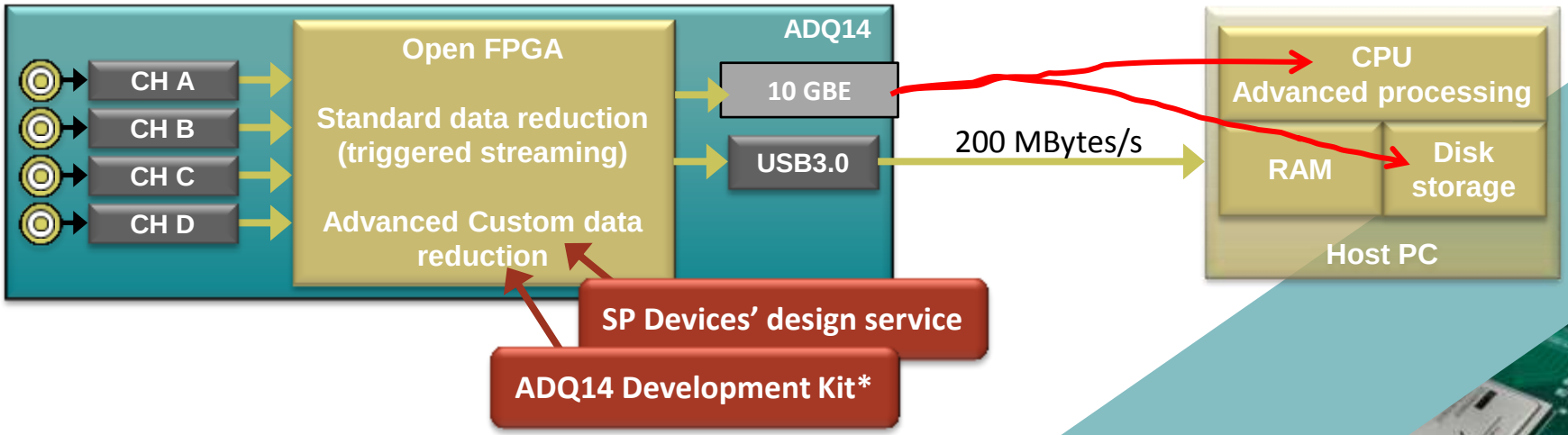
## System design

### Optimized for data storage

### Peer-to-peer streaming for maximum data storage capacity (real-time)




### Data processing on ADQ14 for reduced data set and saved disk space




* ADQ14 Development Kit is purchased separately

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# ADQ14
## FIRMWARE PACKAGES

# ADQ14 DIGITIZER

## ADQ14–FWATD

**Firmware option for scheduled time domain signals**

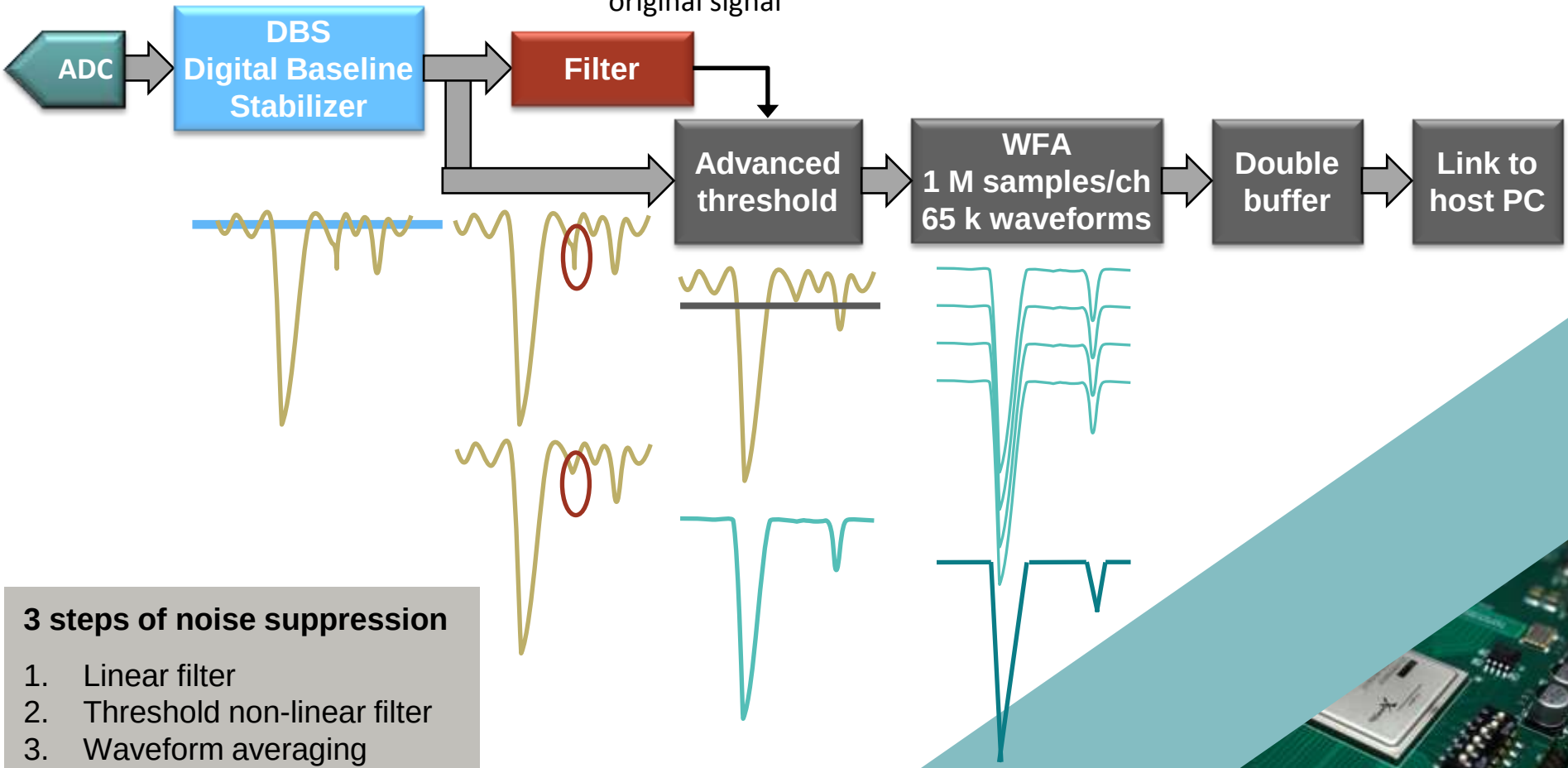
Baseline is stabilized for temperature and slow drift.

Filter to reduce noise into thresholding

Non-linear suppression of noise improves peak detection. Selection from original signal

Waveform Averaging suppress uncorrelated noise.

Double buffer eliminates dead-time and allows for simultaneous read-out to host PC while recording.



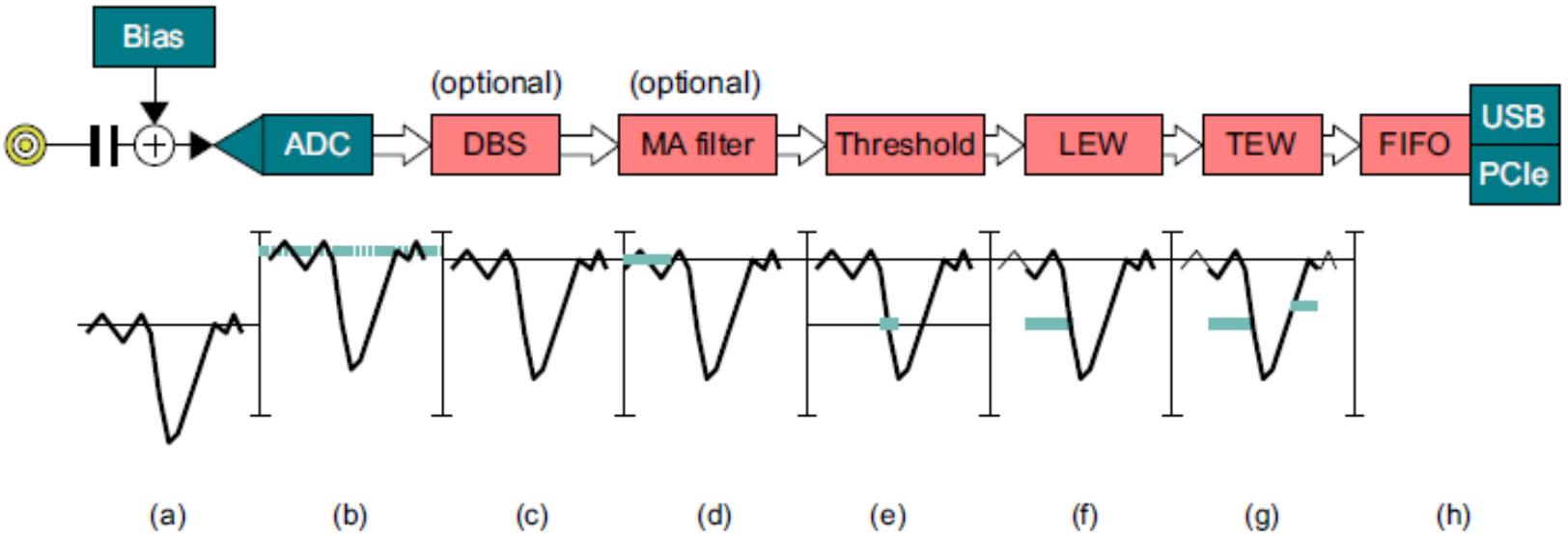

**3 steps of noise suppression**

1. Linear filter
2. Threshold non-linear filter
3. Waveform averaging

# ADQ14 DIGITIZER

## ADQ14–FWPD

**Firmware option for random pulse data capture**

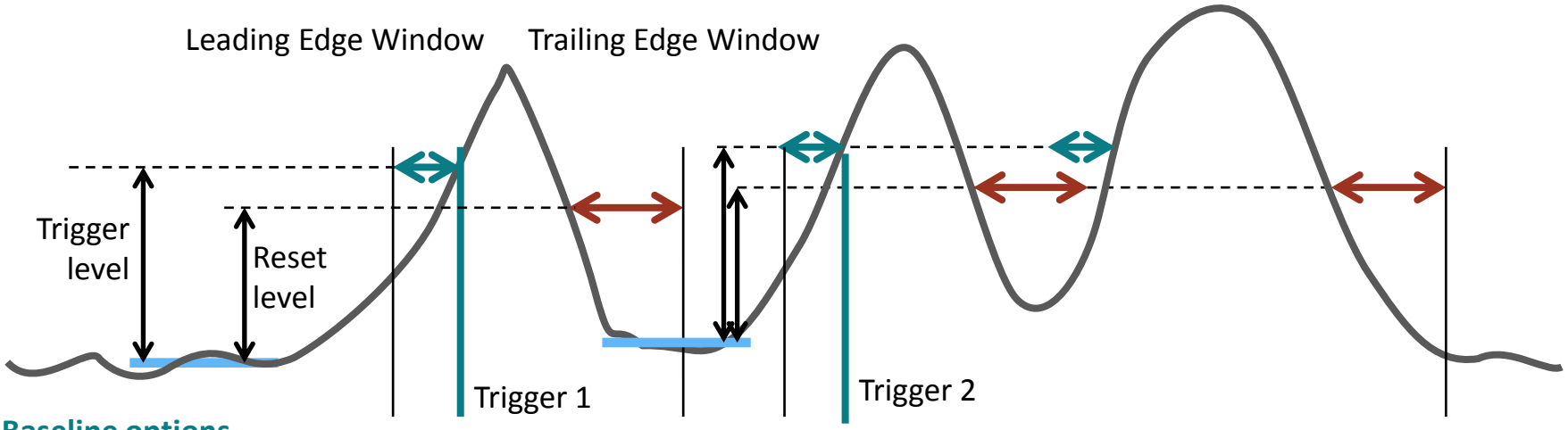



- Adapt and detect pulses in an optimal way.
- Core is an adaptive reference level and detect rapid changes, pulses, relative that level.
- Only valid data is recorded.
- This saves valuable data transfer time and disk space
- It reduces the processing burden when analyzing the data

| # | DESCRIPTION |
|---|---|
| a | The analog signal is a unipolar pulse (negative in this example) |
| b | To fully use the range of the ADC an analog bias can be added to the signal. The bias level is controlled via software in 31 steps rail to rail. |
| c | The Digital Baseline Stabilizer, DBS, is an SP Devices' proprietary algorithm for baseline stabilization in pulse data systems. The DBS output is a controlled baseline level set at a user defined value. |
| d | Moving average filter to track the baseline. This an alternative to using the DBS. DBS is tracking the base line at low update rate whereas MA will have a very high update rate. |
| e | The trigger operation is based on a level trigger relative to the MA or DSB output. |
| f | Leading Edge Window, LEW, is the pre-trigger data. This is used for studying the rising edge of the pulse. |
| g | Trailing Edge Window, TEW, is the post pulse data. This is used for studying the falling edge of the pulse. There is a hysteris available for defining the end of the pulse. |
| h | The FIFO buffers the data to absorb bursts of very high activity. |

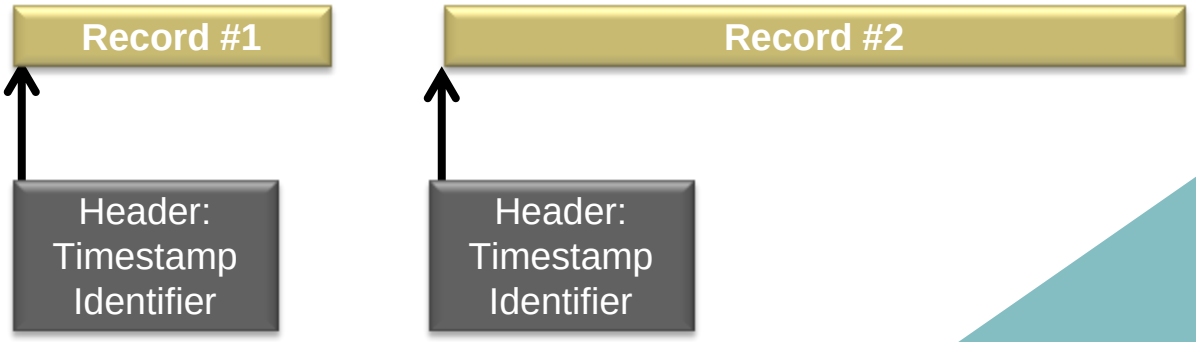
# ADQ14–FWPD

**Firmware option for random pulse data capture**




**Baseline options**

- **Moving average filter**
- **DBS Digital Baseline Stabilizer**

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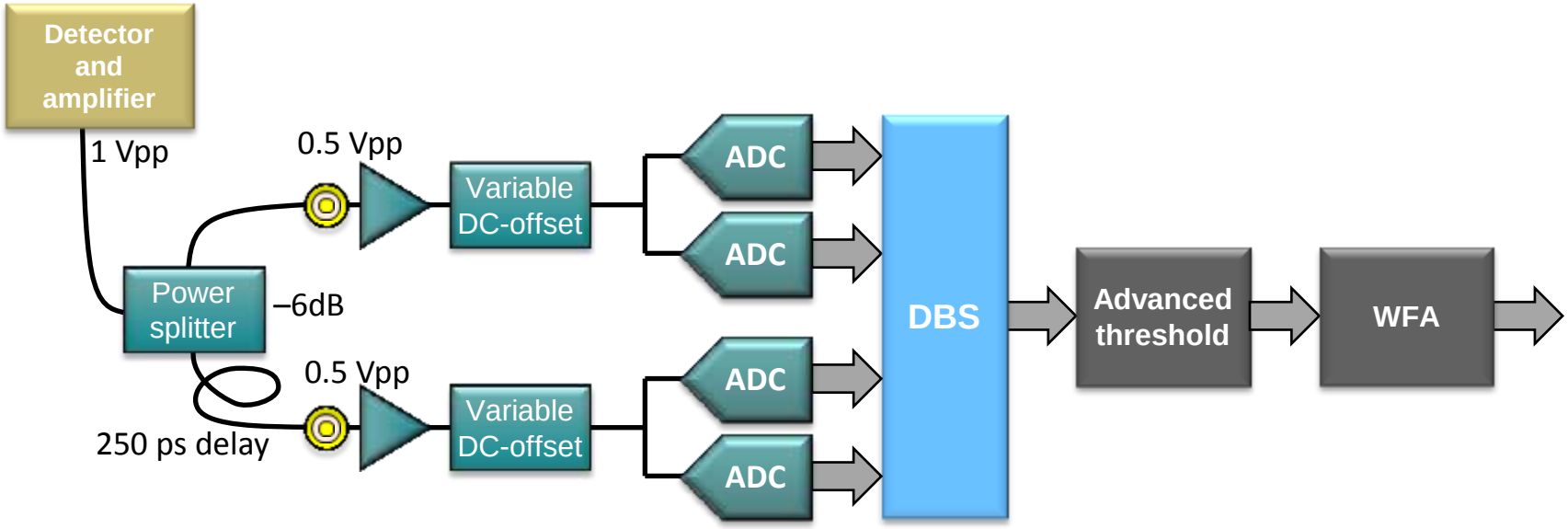
# ADQ14

## ADVANCED APPLICATIONS

# ADQ14 Advanced applications

## Getting 4 GSPS at 14 b resolution




External interleaving with power splitter

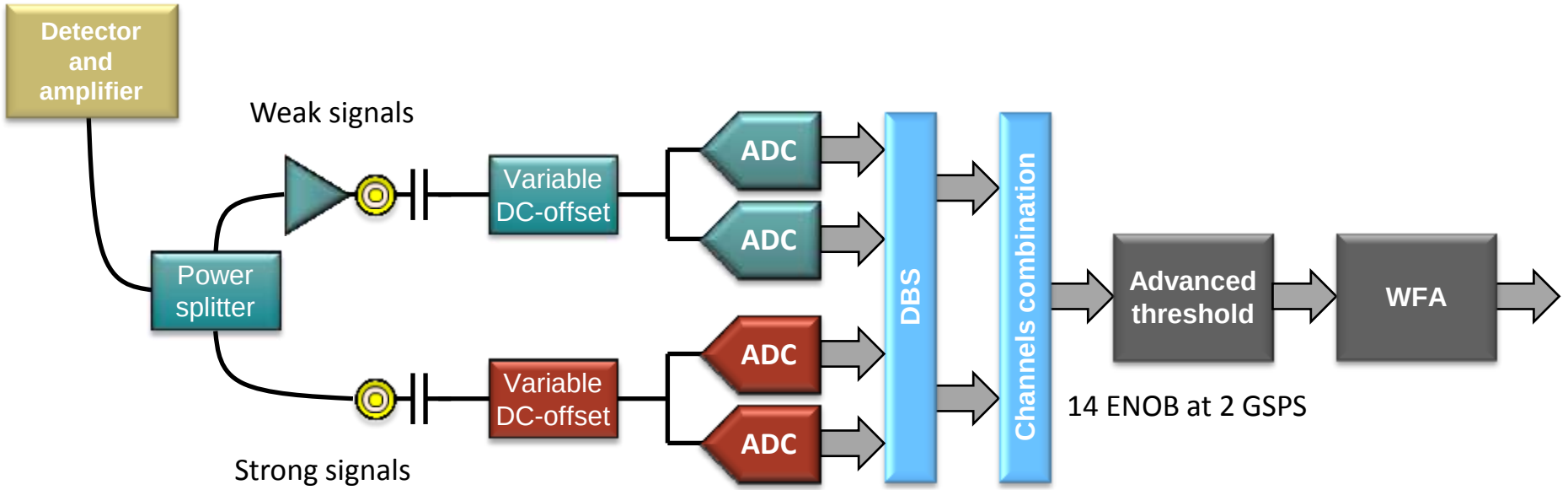
DBS handles baseline matching

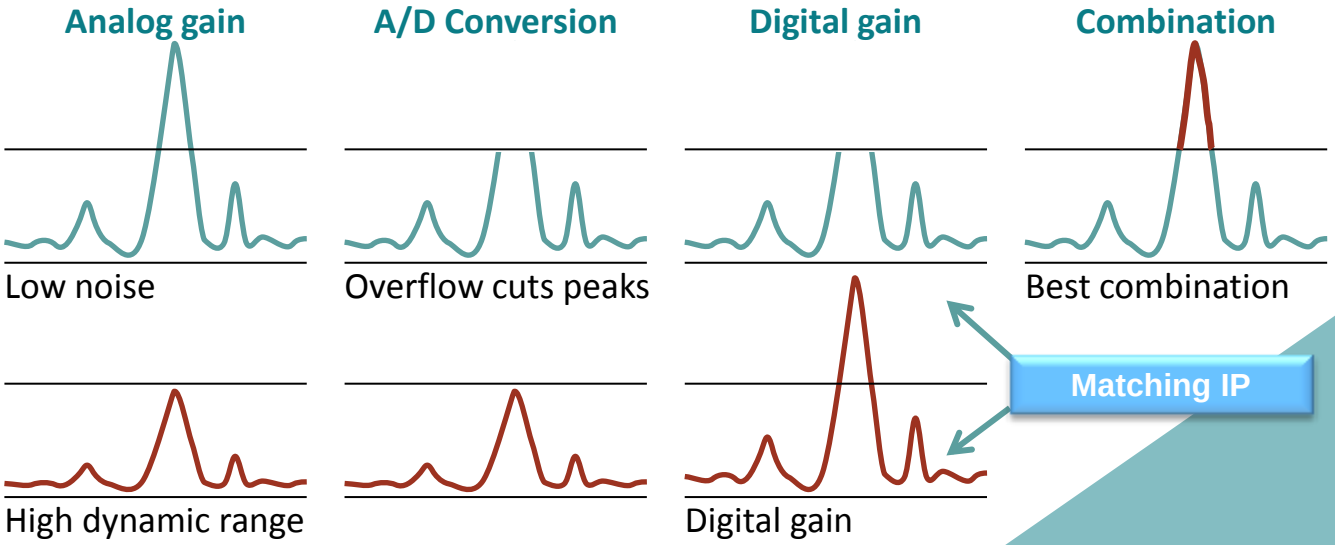
WFA up to 1 ms waveform duration.

See application note 15-1581

# ADQ14 Advanced applications

## Getting 14 ENOB at 2 GSPS




See application note 15-1450

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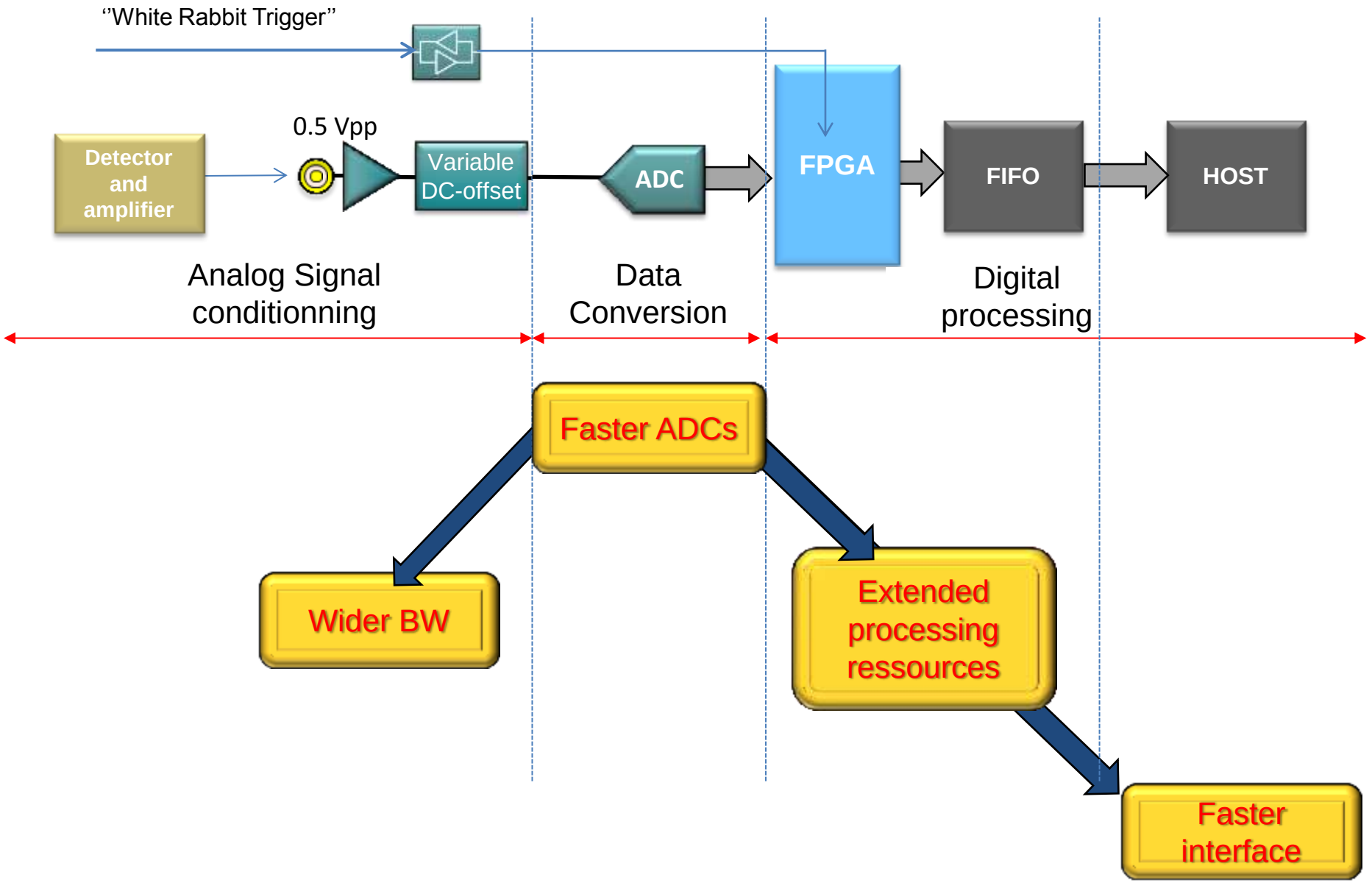
# POSSIBLE FUTURE ENHANCEMENTS

# POSSIBLE FUTURE ENHANCEMENTS

**REQUIREMENTS FOR FASTER DIAGNOSTICS MEAN REQUIREMENTS FOR:**



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# Thank you !


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