Mezzanine style RTMs

a “simple” route towards custom MTCA.4 signal conditioning

A beginners view 3 months into the first MTCA project

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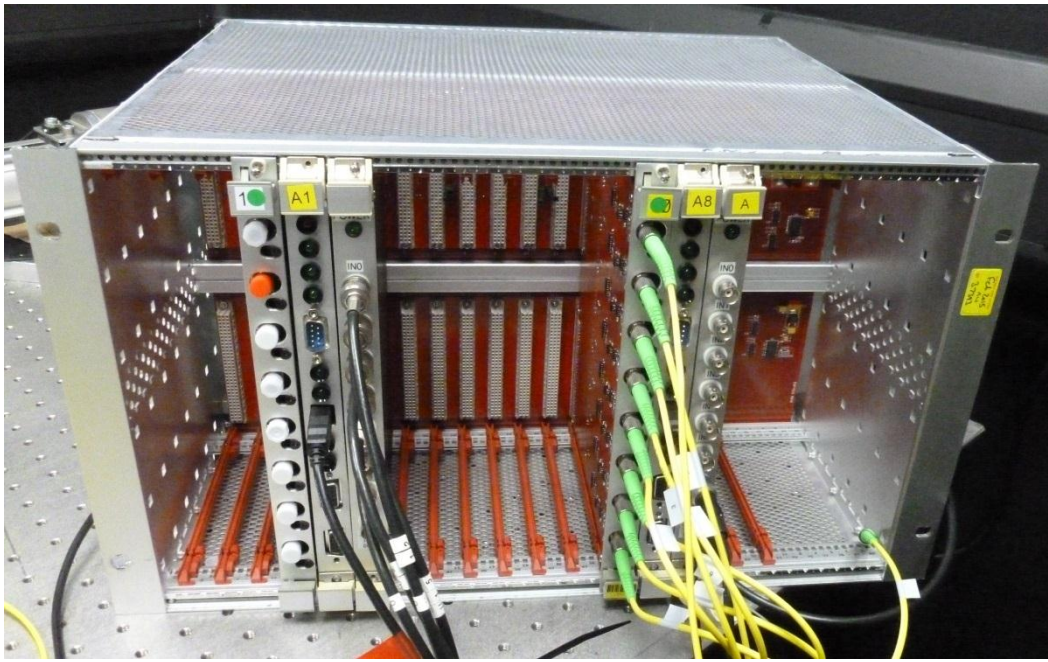
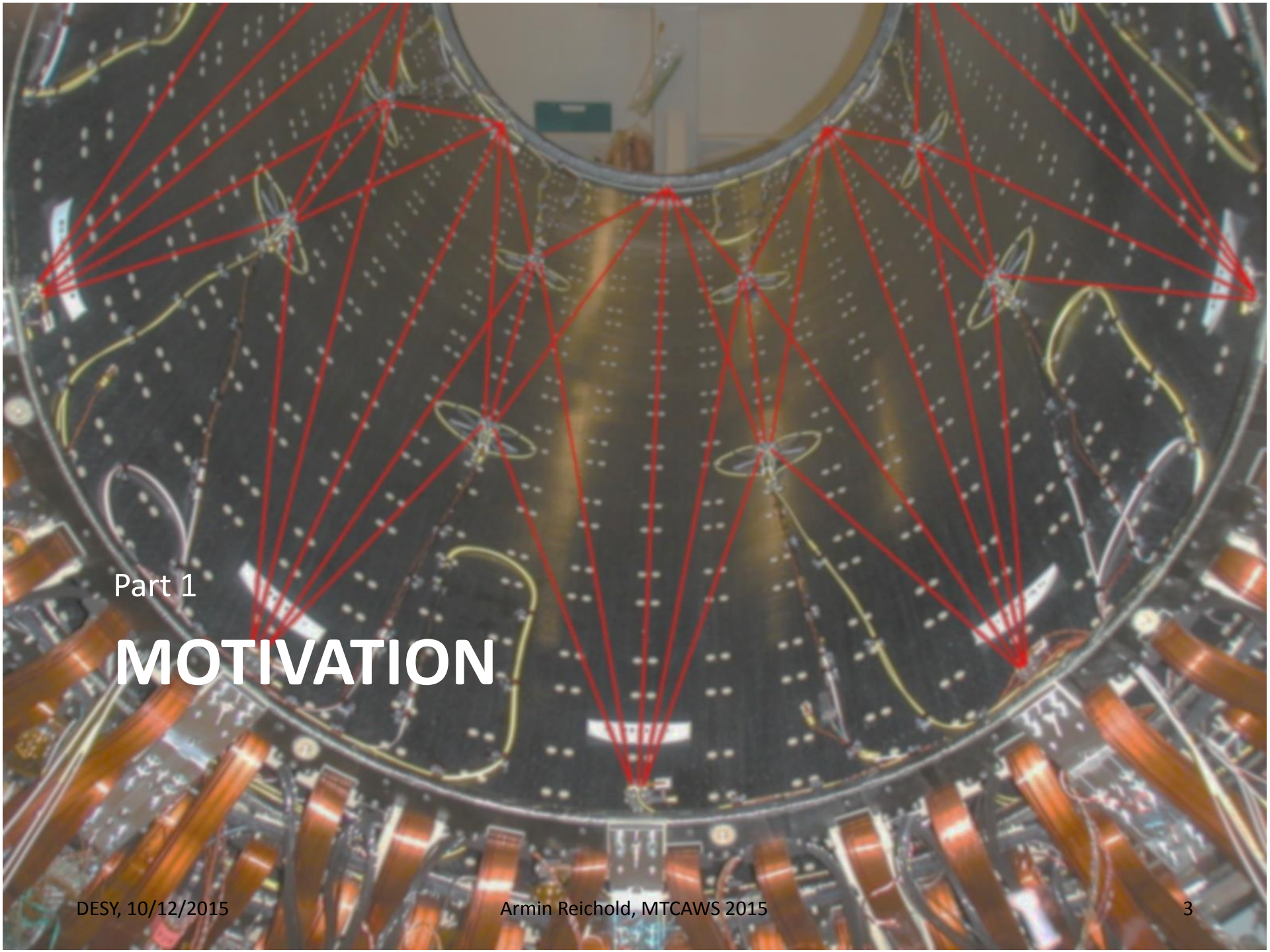
Overview

1. Motivation
   - Strategic needs at Oxford physics
   - From measurement to DAQ problem
   - Pilot project needs
2. Design Strategy
3. Pilot project status
4. ~~Summary~~ no time



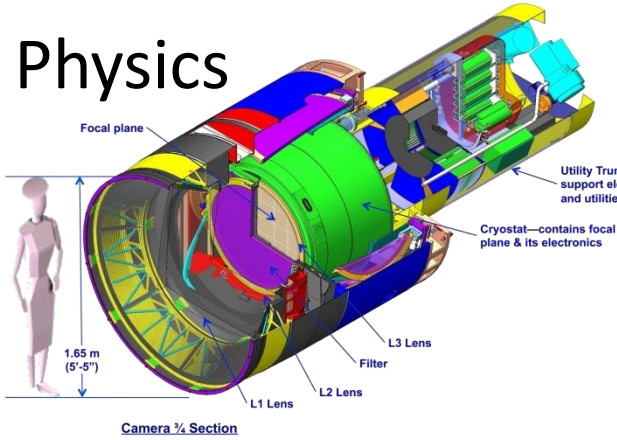


Part 1

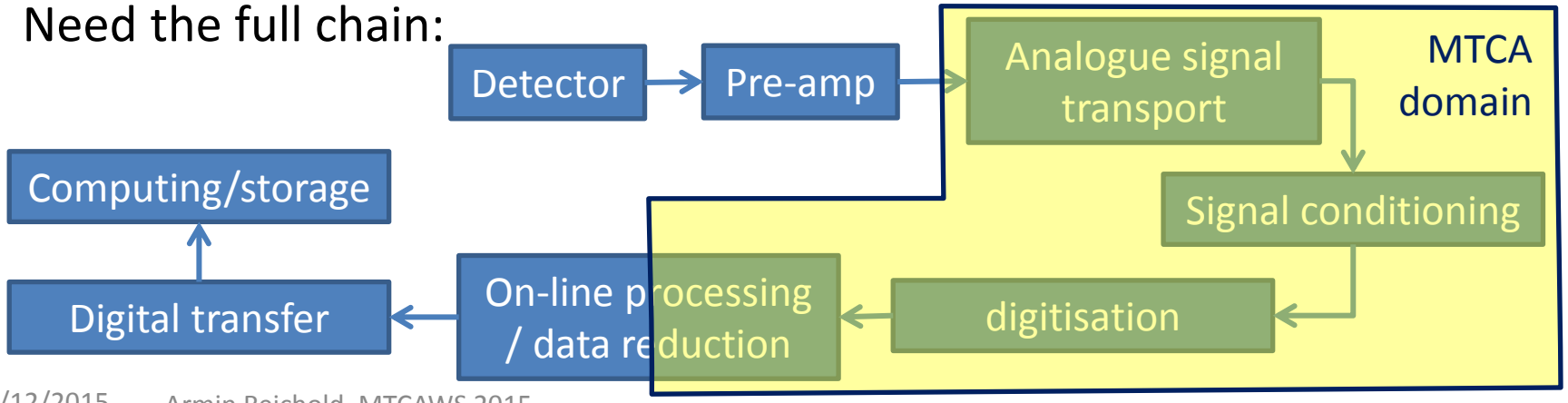
MOTIVATION

Motivation

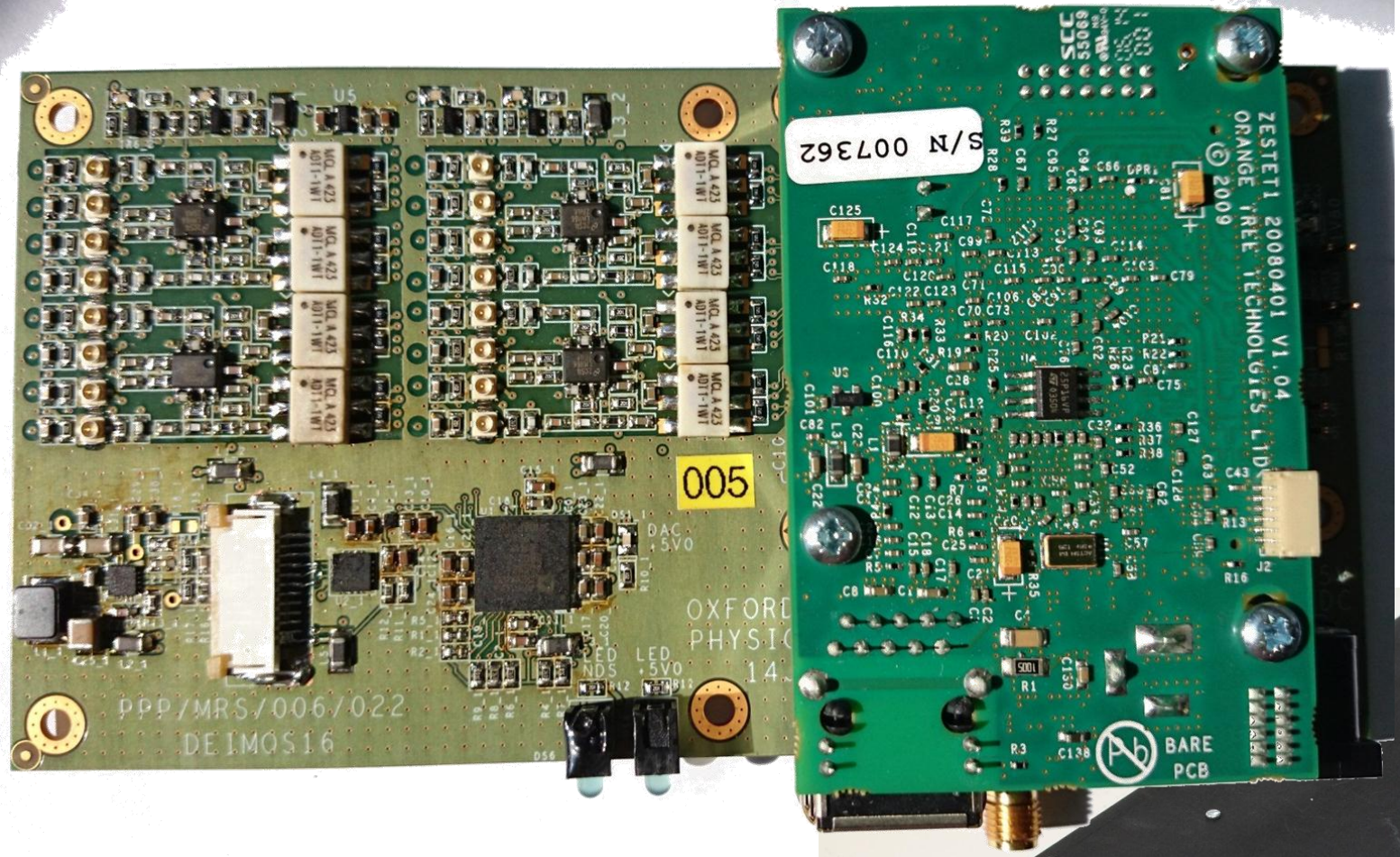
Strategic DAQ needs in Oxford Physics

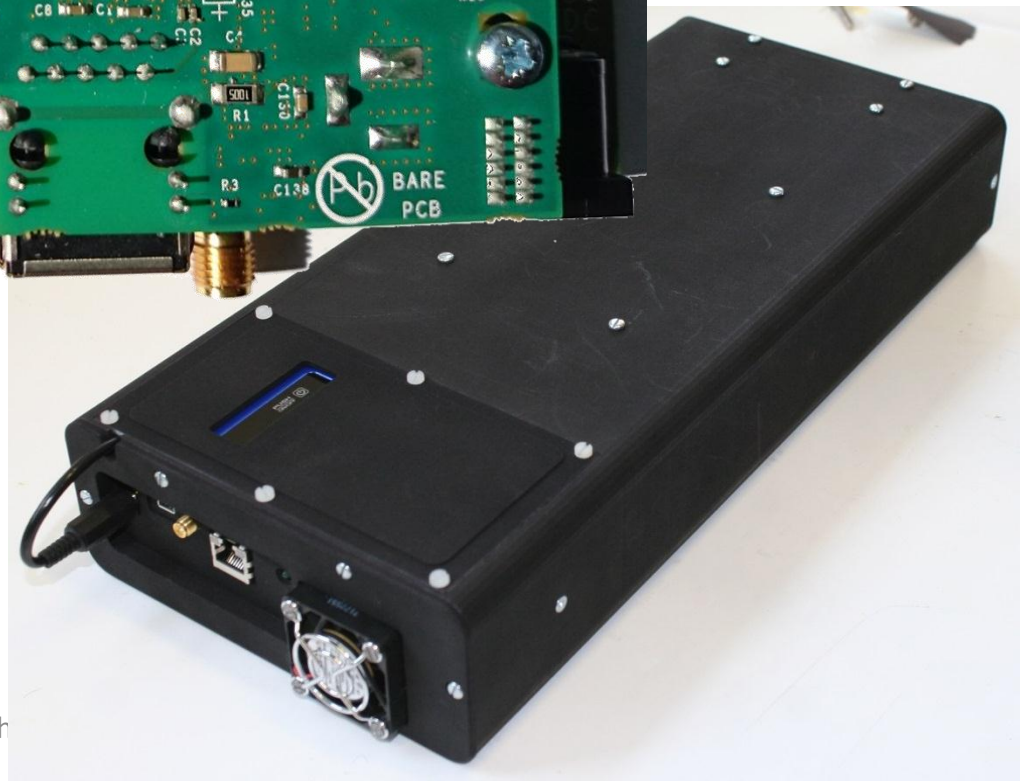


- Characterised by a large range of
  - Number of channel from few to $3*10^9$ (LSST)
  - data rates from few 100 b/s to 20 GB/s
  - signal frequencies from DC to multiple GHz
  - signal types:
    - Optical: 0 to 100 MHz optical intensities from nW to mW,
    - Optical: photon counting from Hz to MHz
    - Electrical: charge pulses from particle detector O(1000e) in O(1ns),
    - Electrical: continuous wave forms from squids O(1μV) at 0 to O(10kHz),
- Large near line computing needs (LHC, ATCA, COB, …. Not my forte)
- Harsh front end environments (radiation damage, radio purity, vacuum, miniaturisation)
- Need the full chain:



Examples:
Backpack prototype



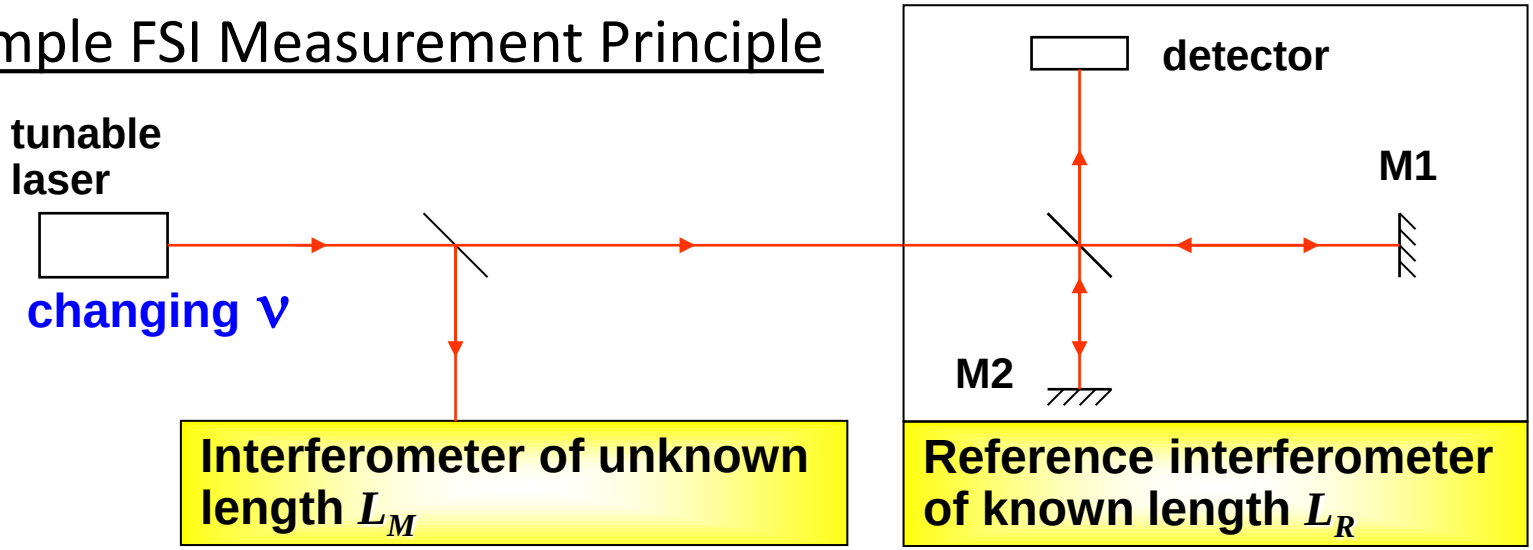


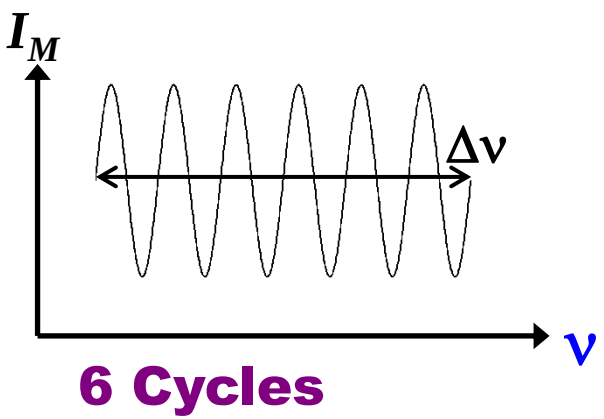
- Portable neutron detection
- 16 channel integrating TIA
- transformer coupled to differential ADC
- 30MHz (max 65MHz).
- serial LVDS to zestet1 fpga daughter card.
- Self calibrating

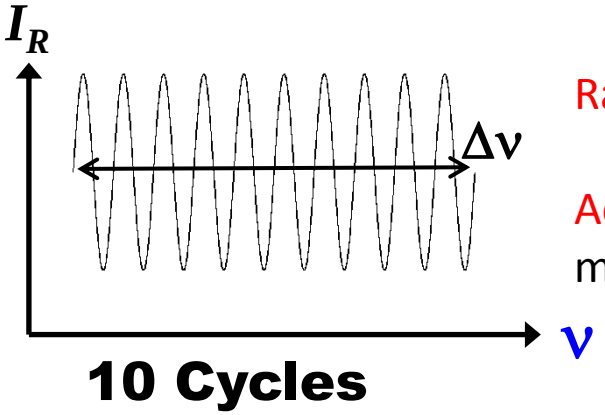
Motivation

(from measurement to DAQ problem, acute)

Simple FSI Measurement Principle







Range: 20cm to 20m

Accuracy: < 0.5 microns per meter

Measured length L_M = 6/10 (x L_R) = 0.6 x Reference length

Motivation

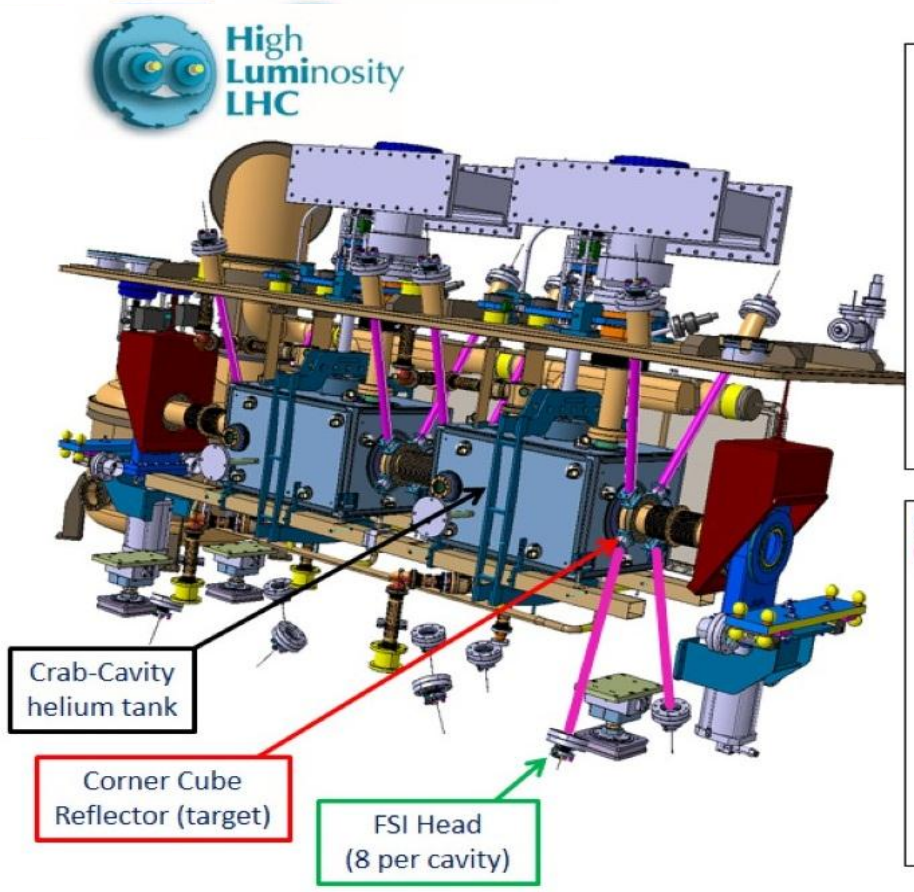
(FSI technology driven FUTURE requirements)

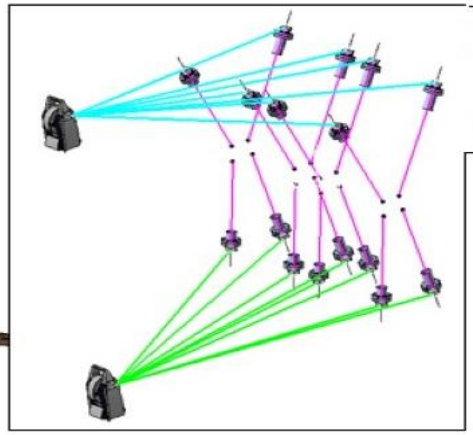
- Laser limit: signal frequency: $f_{signal} < 17$ MHz
- Oversampling: ≥ 5 points per fringe
- DAQ resolution: 16 bits
- Data rate: ≤ 170 MB/s per channel
- Simultaneous channels: from 8 to O(few 100)
- But luckily ….
- Burst mode
  - burst duration: buffer limited, 0.1 to 2 sec
  - Gap duration: transfer limited, variable to get full transfer
- Compute intensive, GPU based near-line processing

Motivation (acute scientific pilot project needs **via commercial route!**)

- **Accelerator Physics:** LHC-upgrade crab cavity alignment

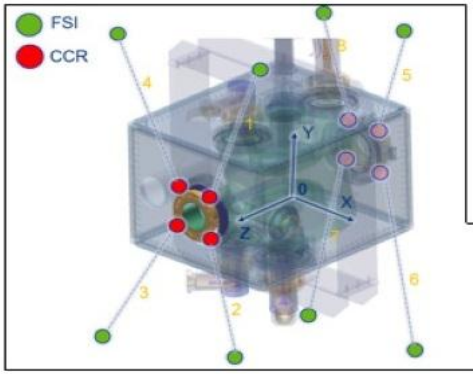
CRAB-CAVITY POSITION MONITORING SYSTEM





FSI head positions in external referential coordinate system

FSI measurements + Pos.calc.algorithms



Helium tank thermal contraction compensation

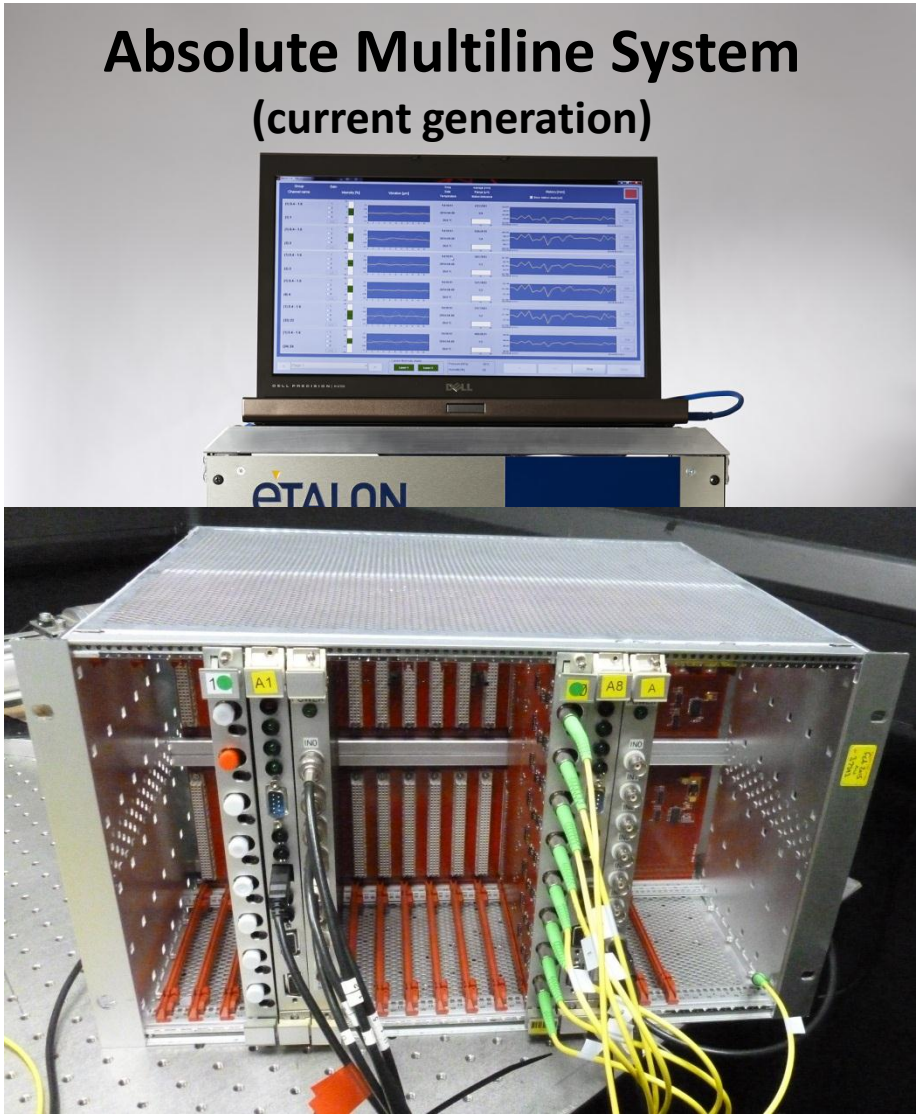
Helium tank/CCR targets geometry measurements (CMM)

HELIUM TANK (CRAB-CAVITY) POSITION

- Short term project
- Handled via commercial and science routes

Motivation (acute commercial pilot project needs)

- Commercial FSI system by Etalon AG
- Current DAQ
  - Fully custom crate and boards
  - Readout: N*USB2 @ N*40 MB/s ⇔2.5 MB/s per channel
  - ADC: 2.77 MHz at 14 bit
  - Buffer 1: ≈ 8 MB per channel near ADC
  - Channels: 16 to 96
- Future DAQ
  - uTCA.4 based solution
  - Custom optical signal conversion RTM
  - ADC: 125 MHz at 16 bit
  - Buffer 1: ≈ 170 MB per channel near ADC
  - Buffer 2: O(10 GB) on compute AMC
  - Readout :
    - Initially: 2*10 Gb/s Ethernet @≈ 1 to 2 GB/s ⇔ ≤ 82 to 164 MB/s per channel[1)] {via compute AMC UDP link}
    - Finally: 1*PCIe x4 Gen3.0 @≈ 3 GB/s ⇔ 250 MB/s per channel[1)] via MCH
  - 12 to few 100 channels
  - High availability integration into wider MTCA control systems



1) assuming 12 chan total

Part 2

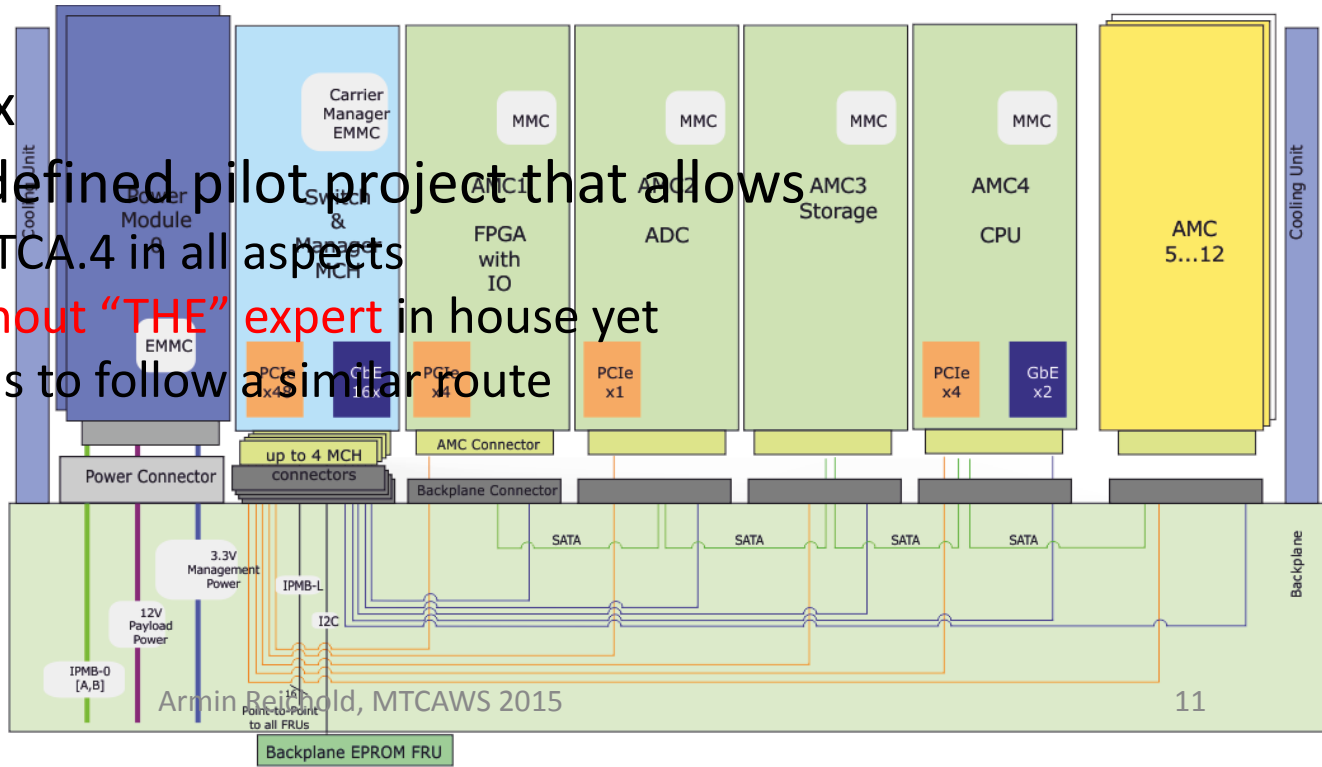
DESIGN STRATEGY

How to build MTCA.4 components without knowing MTCA.4

Design Strategy

- Now: too many custom elements in our chain ➔ Replace some digital custom elements with standard components
- Particularly FPGA & digital data transfer aspects develop rapidly in industry due to large markets
- MTCA.4 offers some elements but not the full chain ➔ still need custom developments
- But …
- MTCA.4 = complex

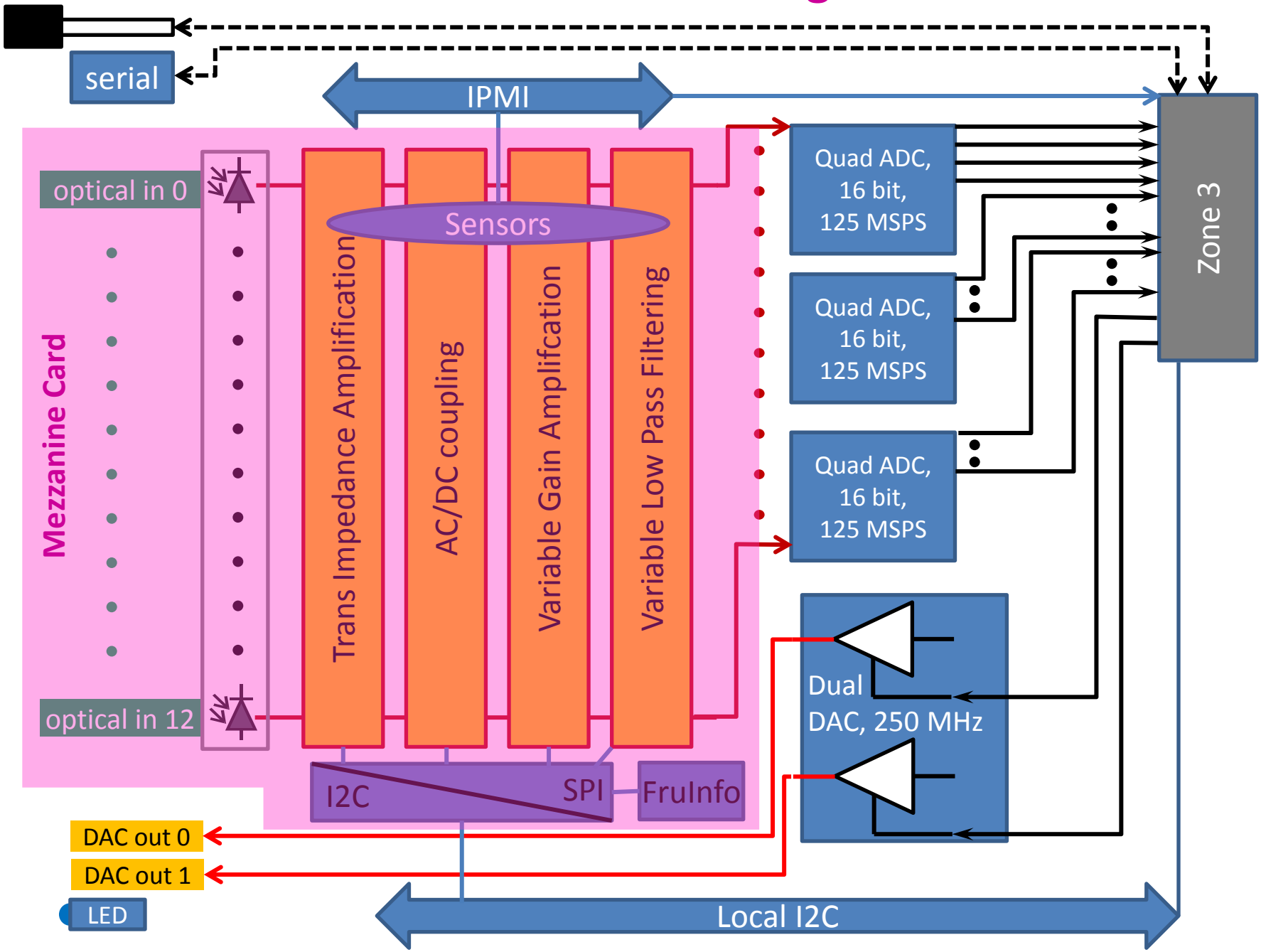
➔ start with a well-defined pilot project that allows
  - learning about MTCA.4 in all aspects
  - development without "THE" expert in house yet
  - future applications to follow a similar route



Design Strategy

- Pilot project = optical to electrical FSI front-end
- AKA signal conditioning RTM
- Split MTCA.4 specific aspects from analogue problems
- AKA raisin picking
- Divide RTM into
  - mezzanine card = analogue front-end
  - RTM carrier = all MTCA aspects (IPMI, Zone3, ADC, power …)

RTM-Raisin Picking



Part 3

PILOT PROJECT STATUS

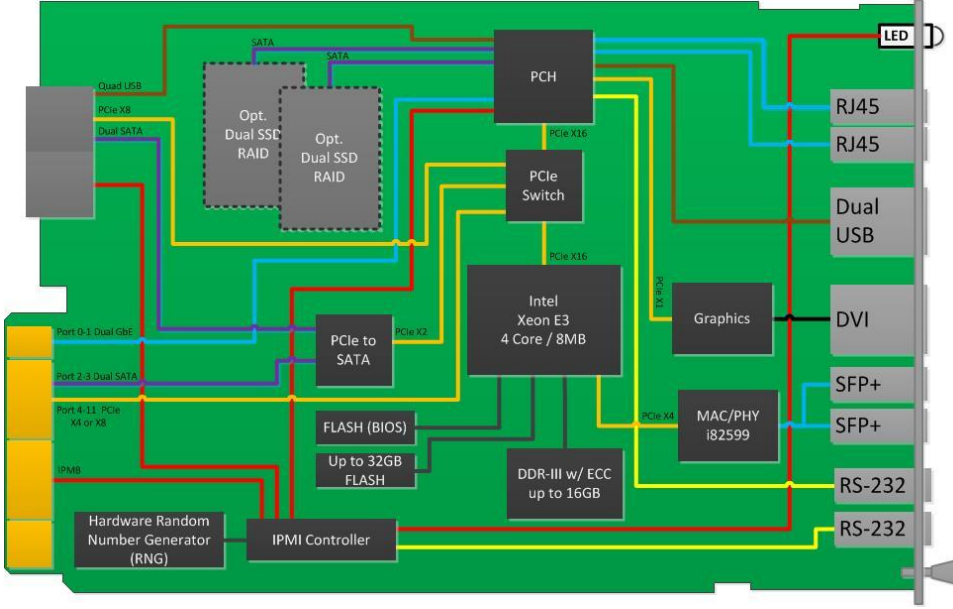
Pilot Project Requirements

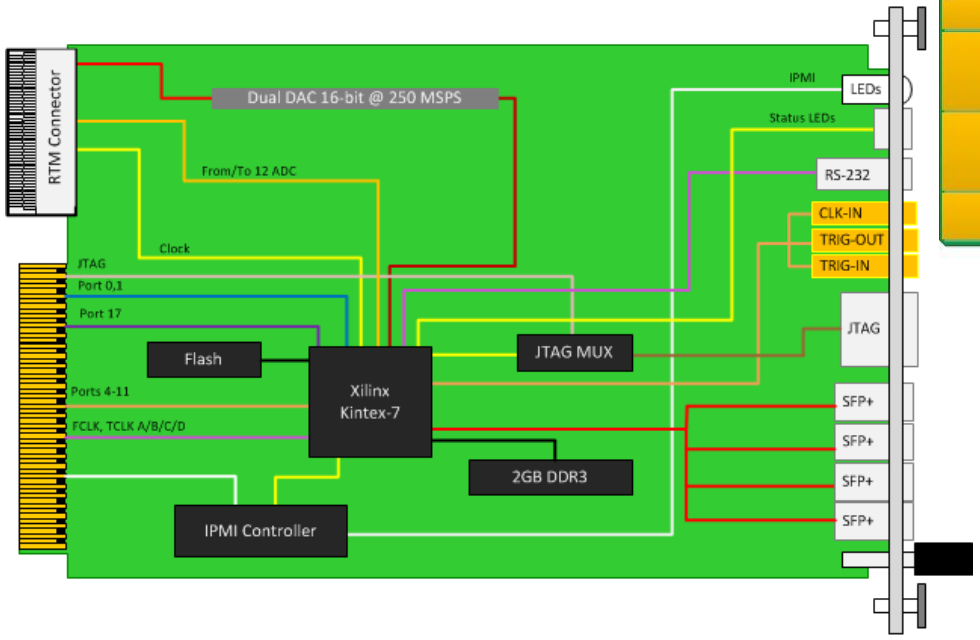
Num channels, N	8-16 (chose **12**)
Fibre connectors	**LC** sockets with PIN receptacle or pig tail
RMS Noise (full chain , gain=1 P_{opt}=0)	**$4*10^{-4}$** full scale (26 counts RMS @ 16 Bit)
signal frequency f_{sig}	DC to **62.5 MHz**
Linearity[1)]	< **1%**, full scale, correctable offline
Cross talk (any pair, any f_{sig} any P_{opt})	< 0,5 * RMS_max
Zero-Offset variation ΔV_{off}	+/- 0,5% full scale, correctable offline
Gain variation δg (all channels, any f_{sig})	+/- 2%
Optical input power P_{opt}	0 µW to 160 µW
min. wavelength range Δλ	1500 nm to 1620 nm
Gain g	1 to **160**
Number of gain steps N_g	>= 32 steps, logarithmic
coupling	AC/DC switchable
Anti-Aliasing-Filter control (minimum)	0,5 MHz / 5 MHz / 25 MHz / 62.5 MHz (= $f_{Nyquist}$)
Mezzanine Power P_{mez}	20 W
Temperature sensors (via IPMI)	2 on mezzanine 2 on RTM carrier
Voltage sensors (via IPMI)	one “per voltage” on mezzanine one “per voltage” on carrier
DAC (optional)	2x DAC, 250 MHz, on RTM front panel via SSMC

1) full chain , gain=1, P_{opt}= 0 to 160 µW, f_{sig} =Dc to 50 MHz)

Pilot Project Status

(the “easy” part = buy stuff)

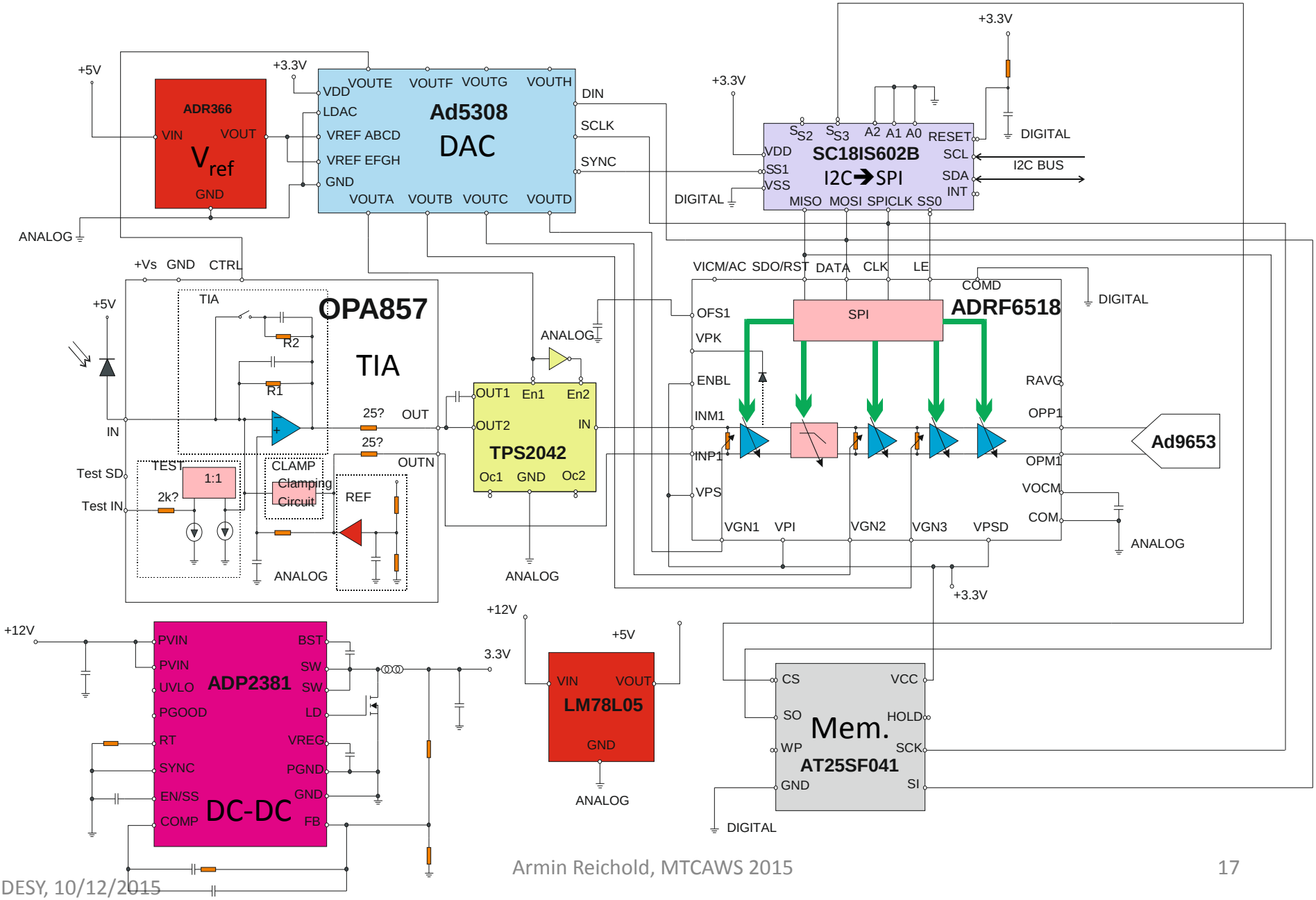




Based on

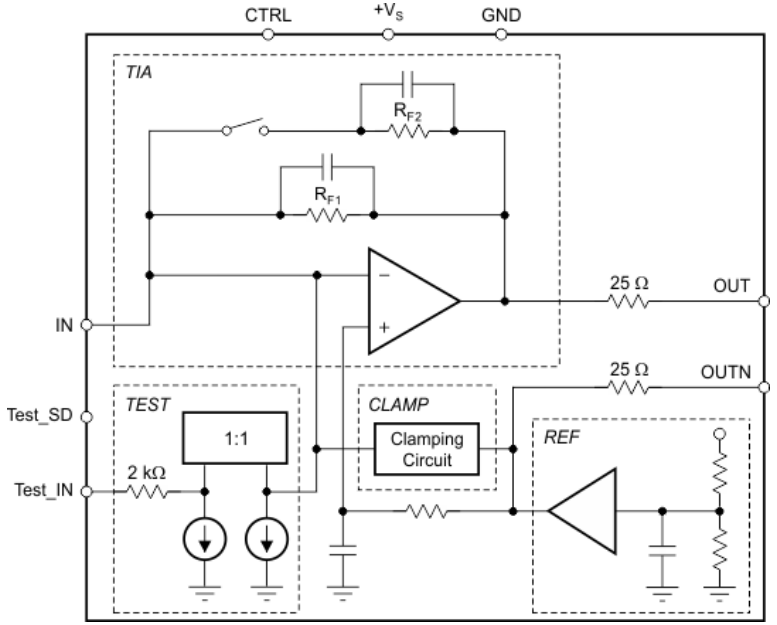
- VadaTech AMC523 for ADC
- AMC725 for compute (interim)

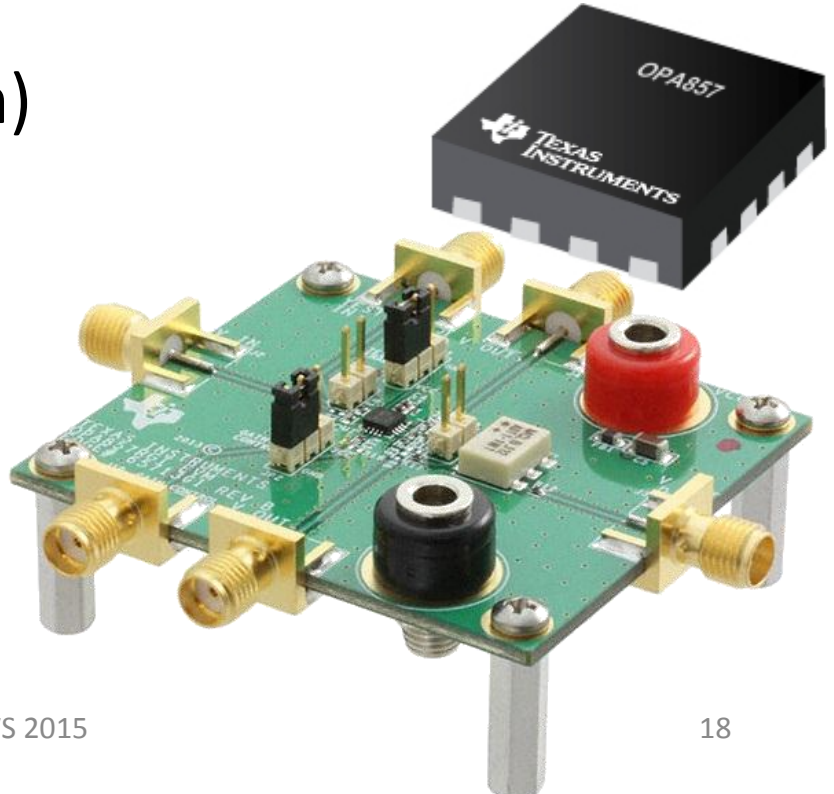
Single Channel Concept



Key components

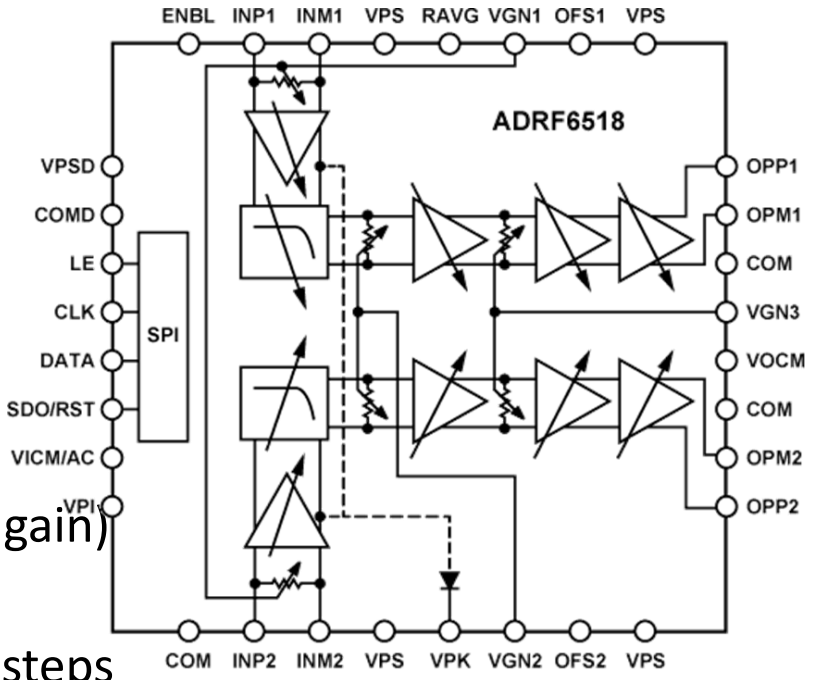
- Texas Instruments OPA857
- Diode trans-impedance amp.
- 3x3mm
- Two stage variable feedback
- Bandwidth: 115 MHz (high gain)
- 130 MHz (low gain)
- Ultralow Current Noise:
  14.7 nA_{RMS} (NPBW = 85.7 MHz)
- Evaluation board testing now

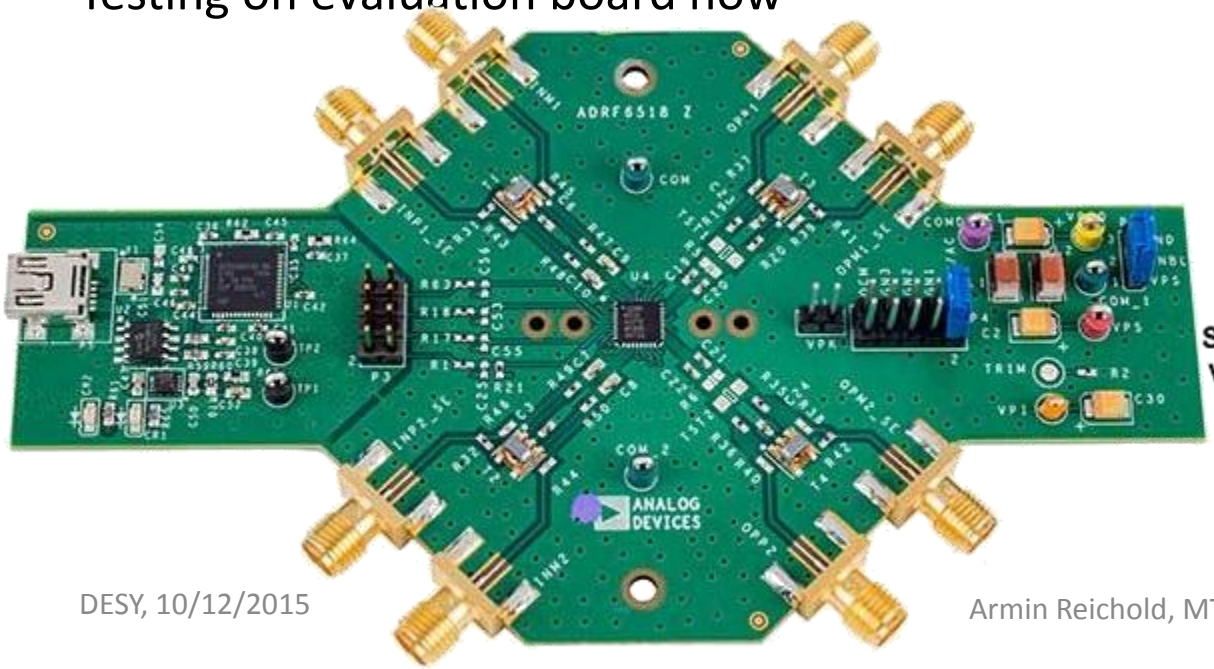


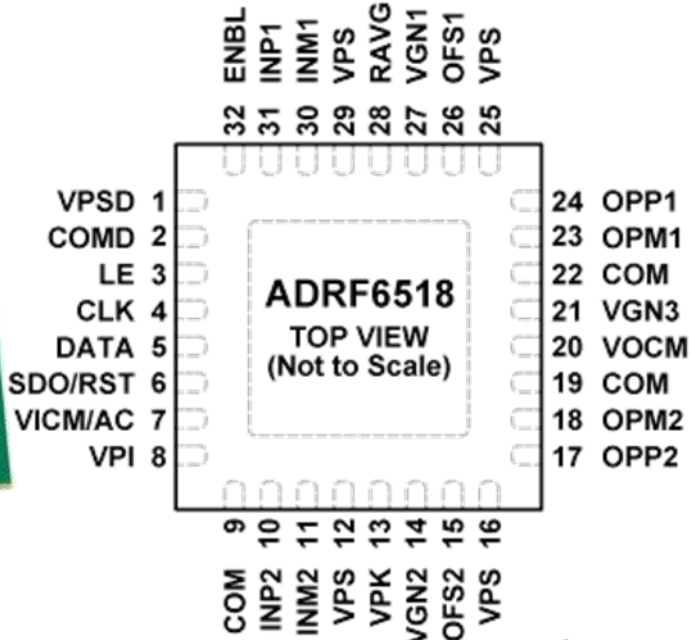


Key components

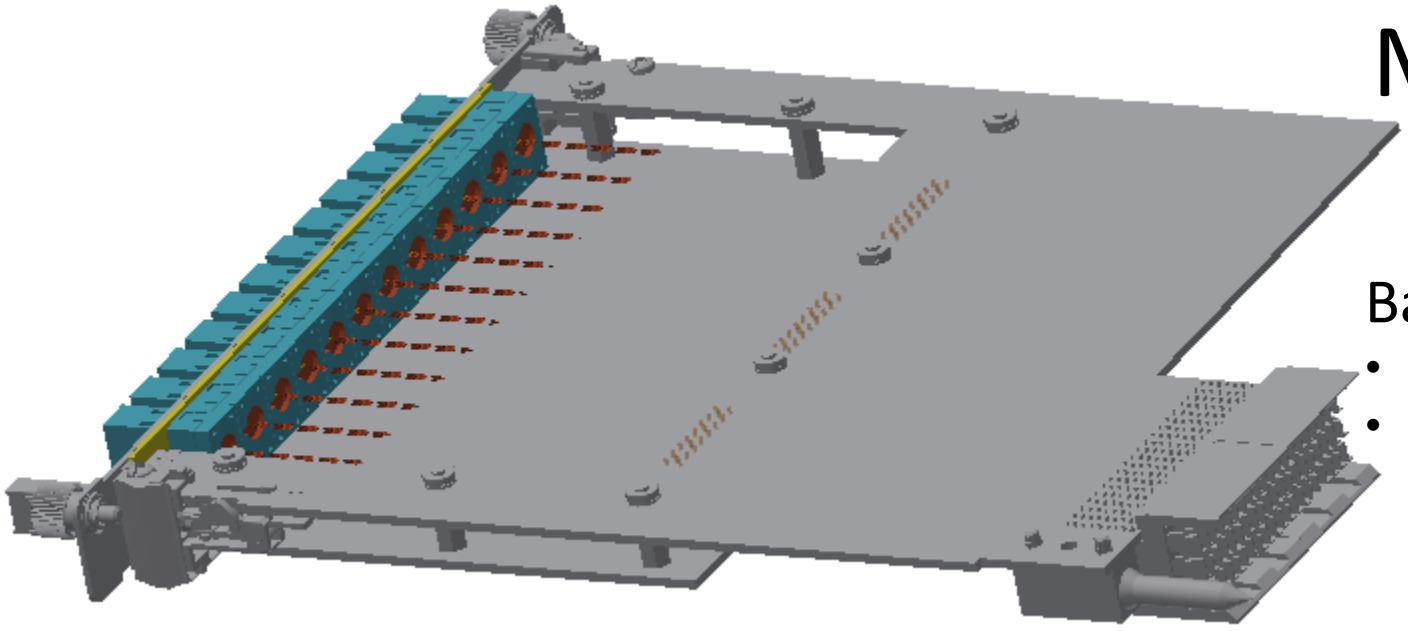
- Analog Devices ADRF6518
- Gain control: 72 dB (analogue) 30 dB (SPI)
- 5x5 mm chip
- Power = **0.4 W**
- ±1 dB gain flatness: 300 MHz
- –3 dB small signal bandwidth: 650 MHz (high gain) 1100 MHz (low gain)
- 6-pole Butterworth: 1 MHz to 63 MHz 1 MHz steps
- Testing on evaluation board now





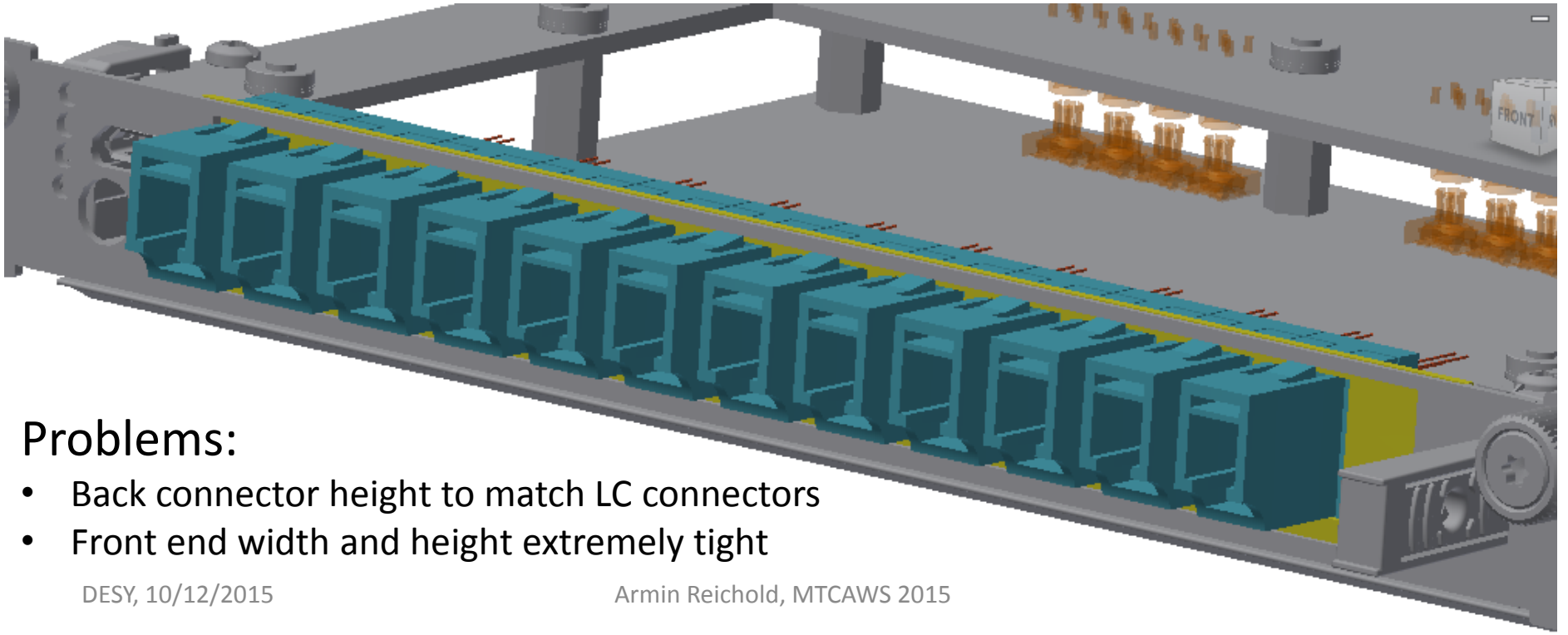


Mechanical Design



Based on:

- LC receptacles with PIN
- 10 mm board separation



Problems:

- Back connector height to match LC connectors
- Front end width and height extremely tight

Special Features

- Local I2C bus controls mezzanine (gain, filter, linearity data)
- Variable delay for clock/trigger on carrier adjusts slot delay
- Response linearisation
  - ADC:
    - Full ADC response stored on carrier per channel
    - FPGA linearises ADC response online using simulink generated processing block
  - Mezzanine:
    - gain and offset stored on mezzanine EEPROM per channel & per gain & per filter setting
    - Correction parameters available for offline use


LOONEY TUNES
"That's all Folks!"