



Science & Technology Facilities Council

Technology

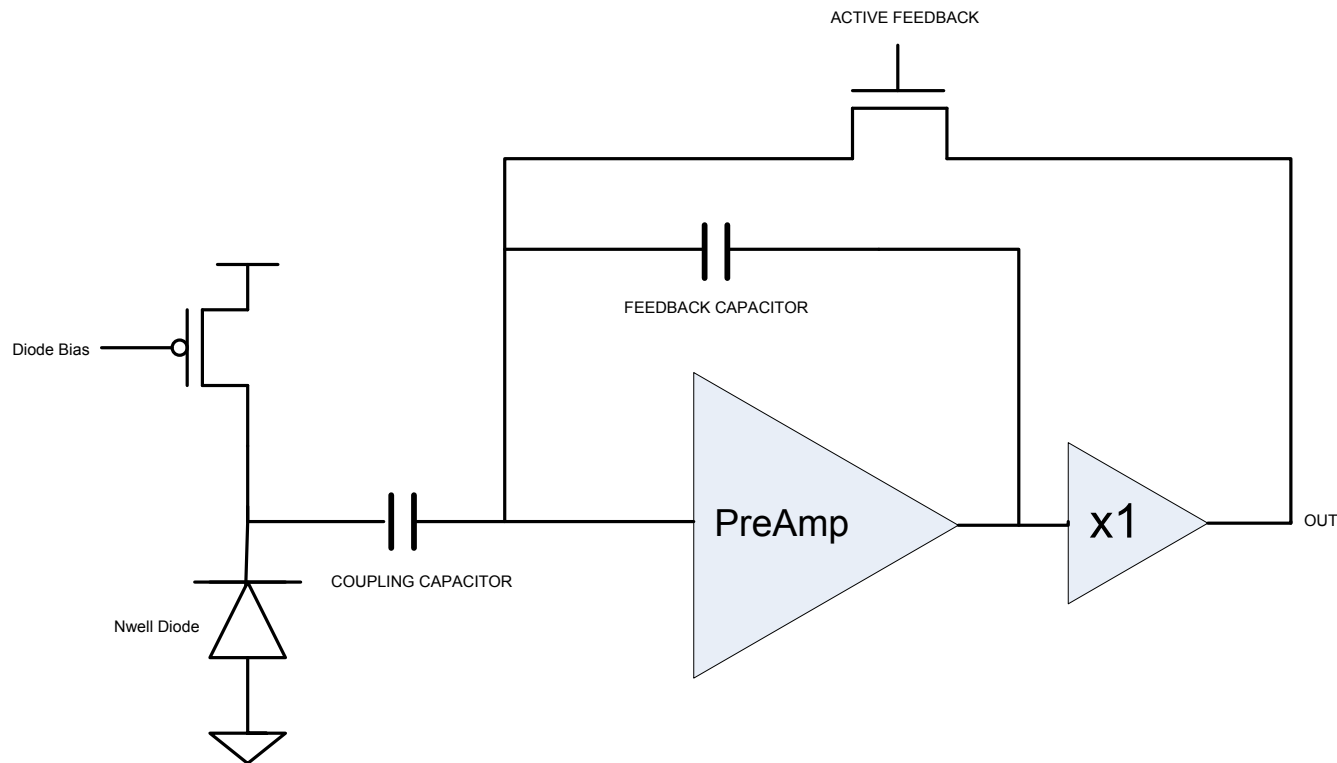
**ATLAS CMOS Strip
Regular Meeting
29/09/15**

HR-CHESS2 Update

**D. Das, STFC-RAL, UK
29/09/15**



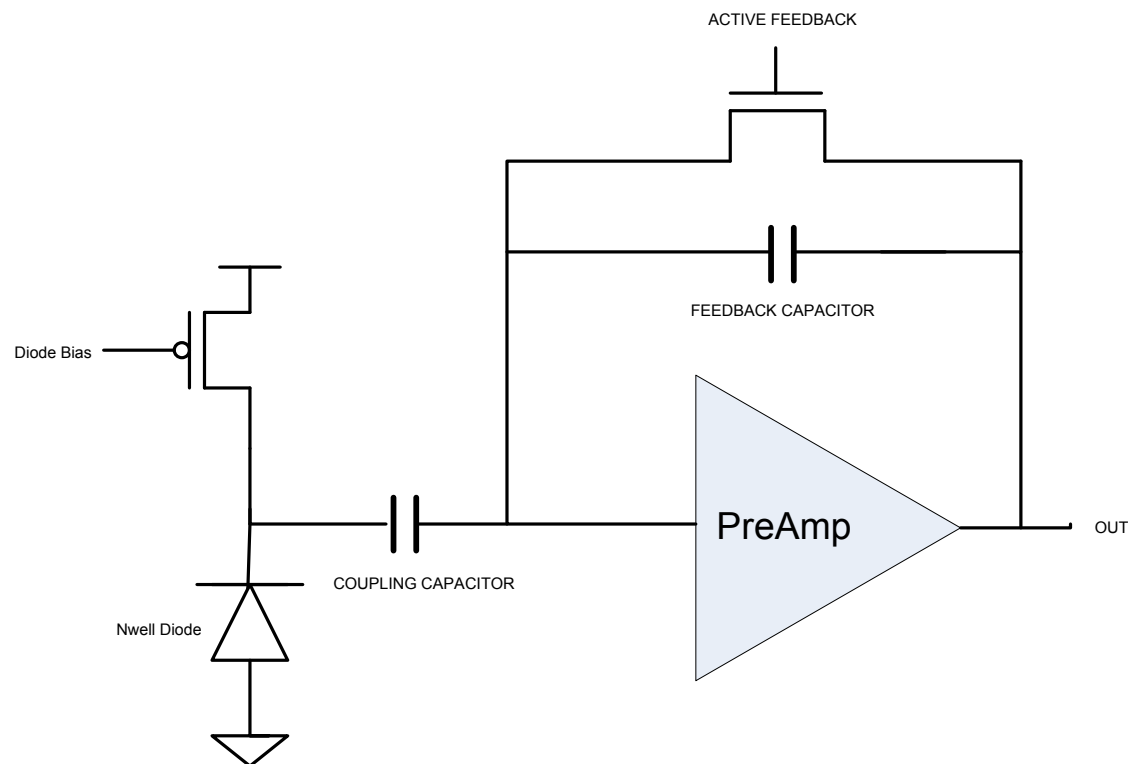
HR-CHESS2 Pre-Amplifier v2 Block Diagram



- AC coupled to block leakage current, MOS device used to bias diode
- Integrated AC coupling capacitor
- Constant current feedback
- Folded cascode architecture with source-follower inside feedback loop



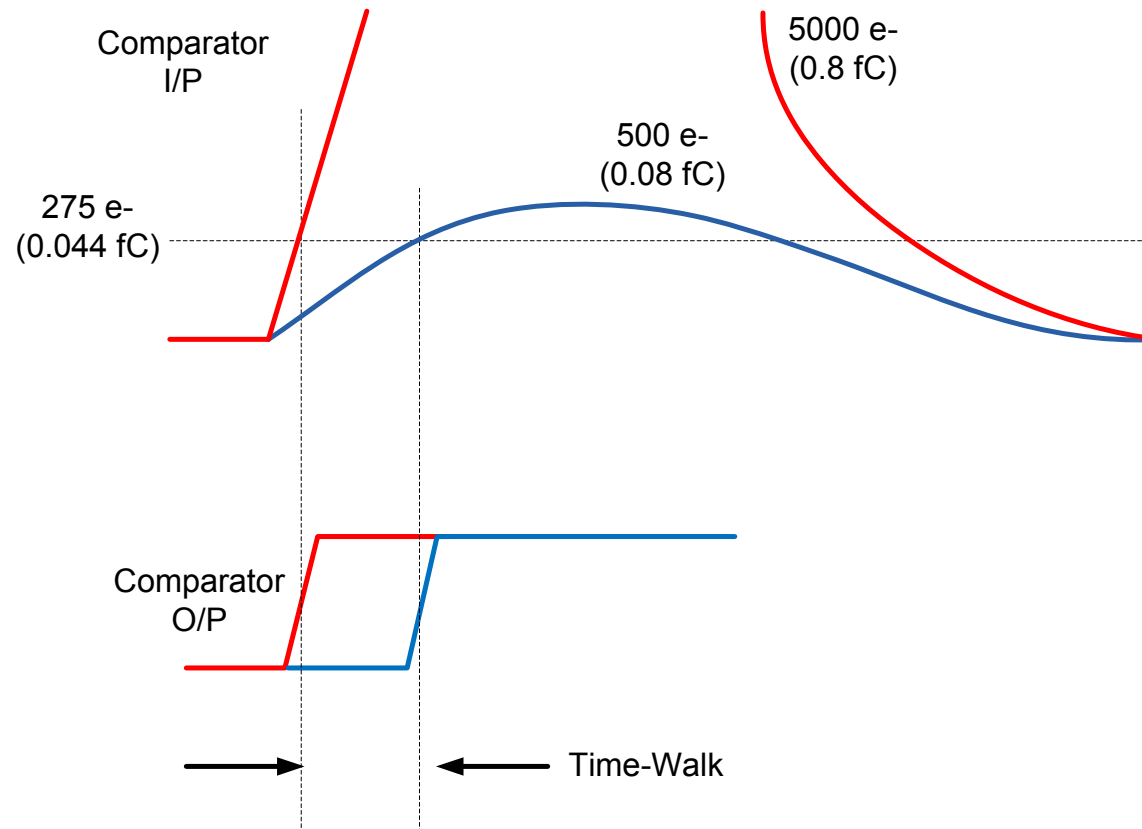
HR-CHESS2 Pre-Amplifier v3 Block Diagram



- Removed source-follower from feedback loop



HR-CHESS2 Time-Walk Specification



Dependence of comparator fire time on signal must be $< 1 \text{ BX}$ i.e. 25 ns

$\leq 16 \text{ ns}$ time difference between comparator leading edges for input signal of size 500 e^- and 5000 e^- with a threshold set at 275 e^-



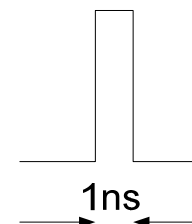
HR-CHESS2 Time-Walk Simulations

Specification < 16ns

Threshold adjusted for each process corner (small differences)

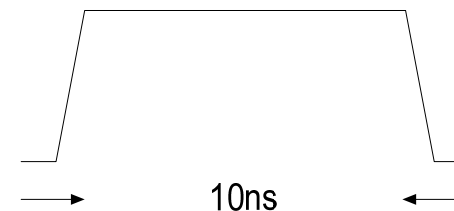
Time-Walk (~1ns charge collection time)

	NOM	FAST	SLOW
+40°C	6.95ns	6.5ns	7.9ns
-40°C	5.32ns	4.9ns	6.2ns



Time-Walk (~10ns charge collection time)

	NOM	FAST	SLOW
+40°C	10.54ns	9.37ns	11.02ns
-40°C	7.5ns	7ns	8ns



Meets specification in all corners



HR-CHESS2 Design Progress Summary

- Modified pre-amplifier design to make it faster & more immune to leakage current
 - Looking into design of pre-amplifier feedback capacitor as it's small $\approx 1\text{fF}$
 - Simulating Trim DAC for comparator offset compensation
 - Preparing for layout of the design
 - Preparing documentation for the first design review of HR-CHESS2 to be held mid to late October
-



3-D structure for leakage current simulation

n697_msh

Pixel Volume = $40\mu\text{m} \times 40\mu\text{m} \times 25\mu\text{m}$

Epi Depth = $25\mu\text{m}$

No. of Pixels = 3

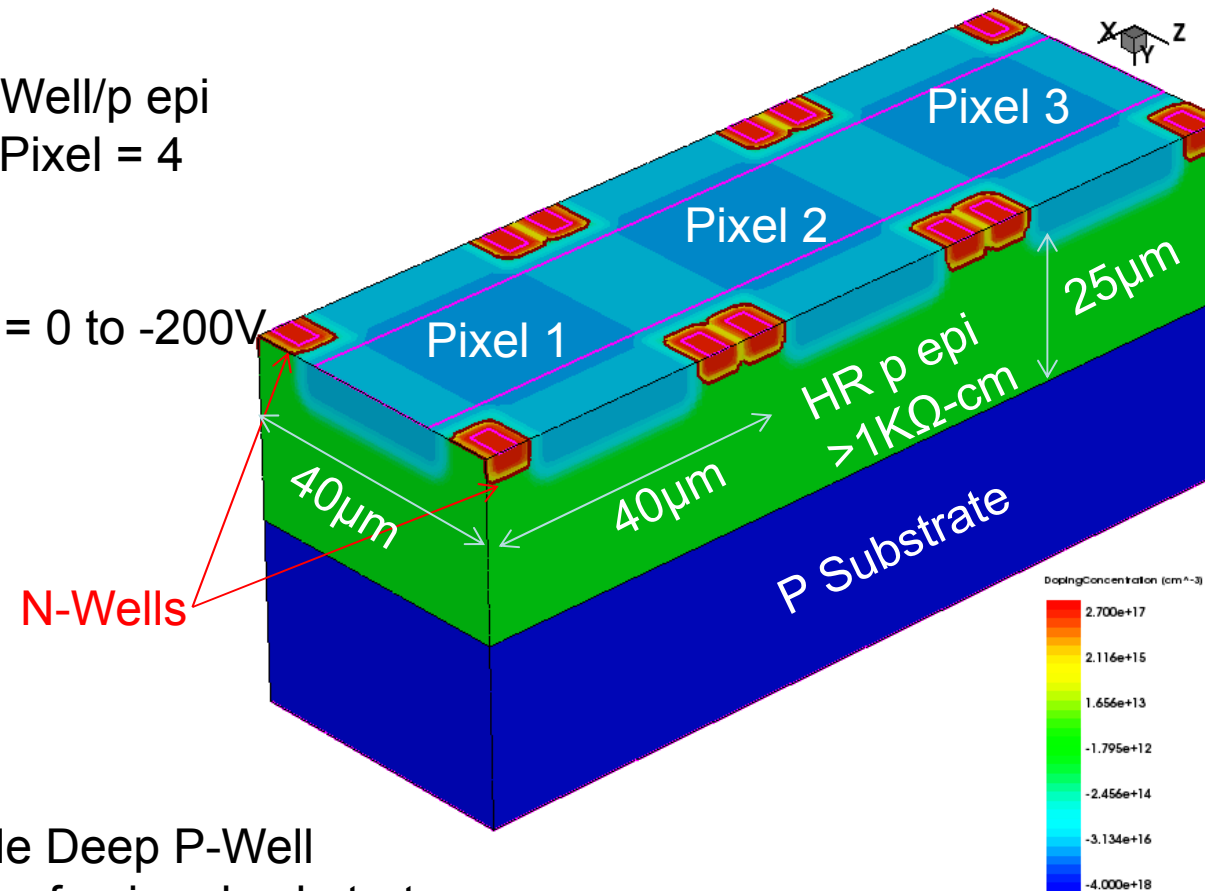
Type of Diode = N-Well/p epi

No. of Diodes per Pixel = 4

N-Well Bias = 1V

P-Well Bias = 0V

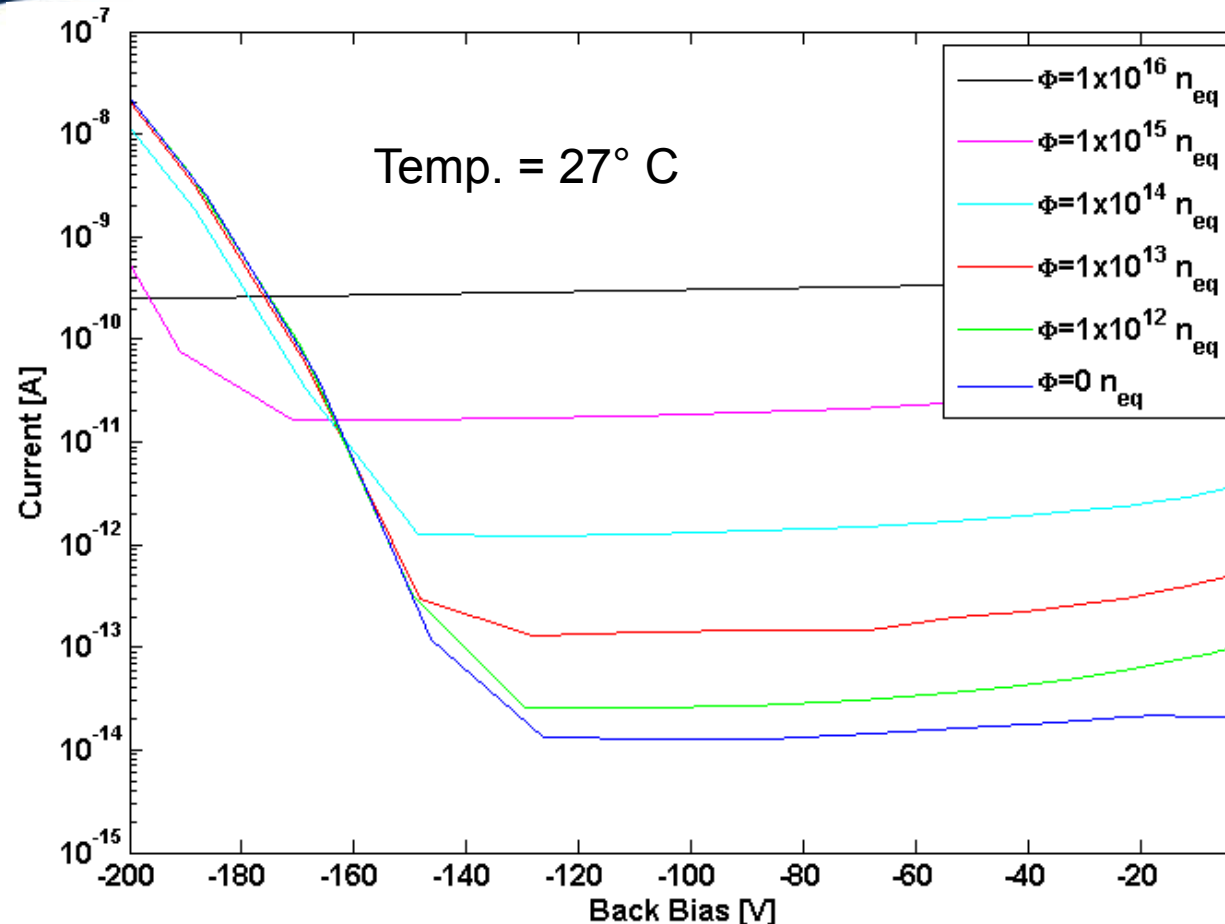
Back Contact Bias = 0 to -200V



- Electronics inside Deep P-Well
- Constant doping of epi and substrate
- N-Well and P-Well has analytical doping profiles



Leakage current vs bias at different fluences



Radiation Damage Model Used:

D. Pennicard et al. / Simulations of radiation damaged 3D detectors for the Super-LHC NIMA 592 (2008) 16–25
IEEE Trans. Nucl. Sci., vol. 53, pp. 2971–2976, 2006
 “Numerical Simulation of Radiation Damage Effects in p-Type and n-Type FZ Silicon Detectors”, M. Petasecca, F. Moscatelli, D. Passeri, and G. U. Pignatelli

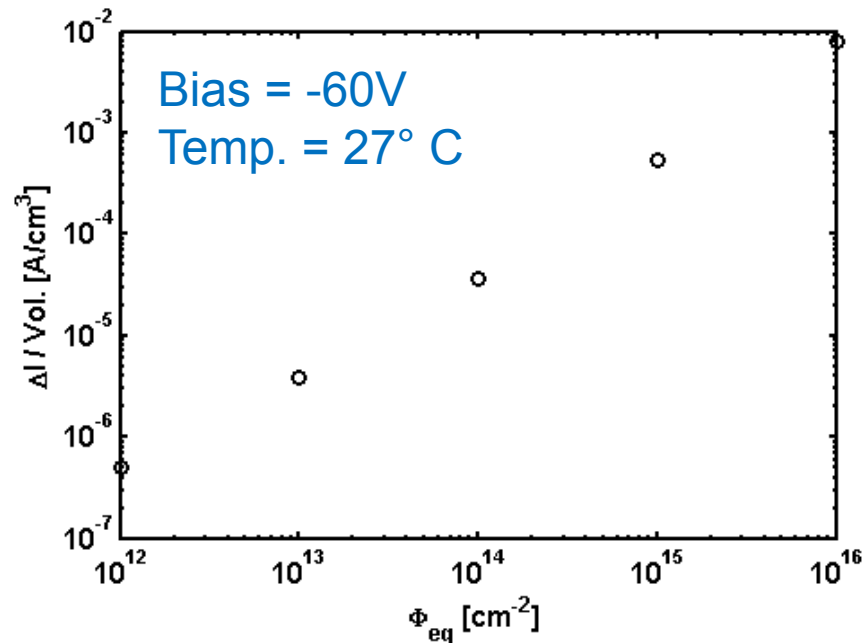
Breakdown voltage increases with fluence because effective doping concentration increases with irradiation!

- Back Bias varied from 0V to -200V (until breakdown)
- Current of Pixel 2 (middle) recorded
- Leakage current **< 500pA** for fluence of $1 \times 10^{16} \text{ n}_{\text{eq}} [\text{cm}^{-2}]$



Leakage current vs geometry

During simulated irradiation dark current increases linearly with fluence:



$$\frac{\Delta I}{V} = \alpha \Phi_{eq}$$

V = volume of sensor

ΔI = increase of total leakage current

Φ_{eq} = equivalent fluence

α = Current related damage rate

Current related damage rate is temperature dependent $\rightarrow \alpha(T)$

Geometry	Leakage Current @ $1 \times 10^{16} n_{eq} [cm^{-2}]$
$40\mu m \times 25\mu m \times 40\mu m$	3.2pA
$40\mu m \times 25\mu m \times 80\mu m$	6.4pA
$40\mu m \times 25\mu m \times 120\mu m$	9.6pA
$40\mu m \times 25\mu m \times 200\mu m$	1.6nA
$40\mu m \times 25\mu m \times 400\mu m$	3.2nA
$40\mu m \times 25\mu m \times 800\mu m$	6.4nA

From simulation results at 27°C:
 $\alpha \approx 80 \times 10^{-18} A/m$