HV-CMOS Options for Stave Layout

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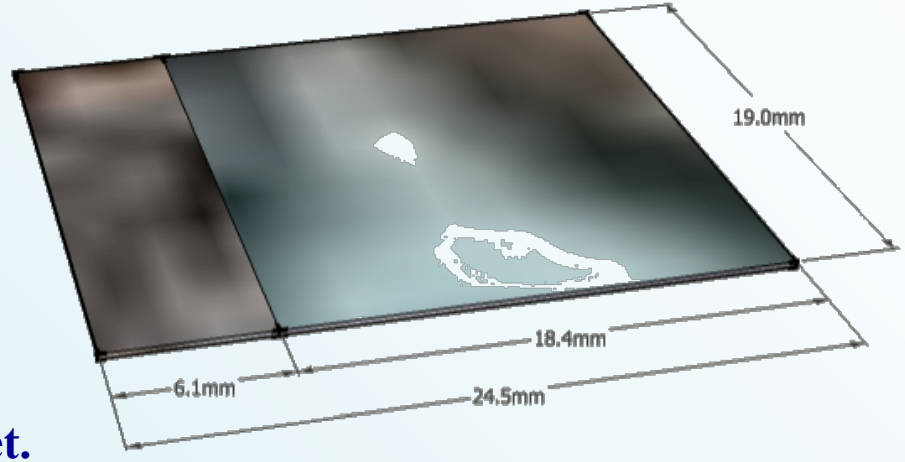
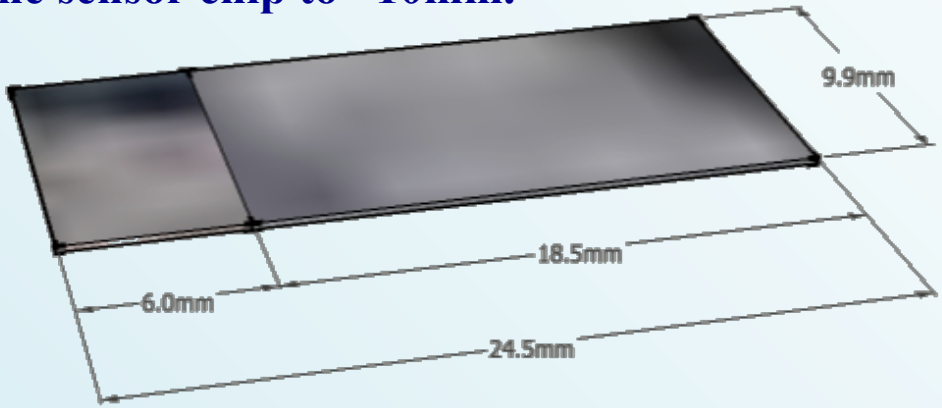
AMS Reticle Size

- The max reticle size for AMS 350 is 24.5 mm x 19.0 mm.
- If we want to keep the ~10 cm wide stave, which is the baseline for the barrel, this 19mm does not fit well.
  - The End-caps may be a different story and I haven't looked at those geometries yet.



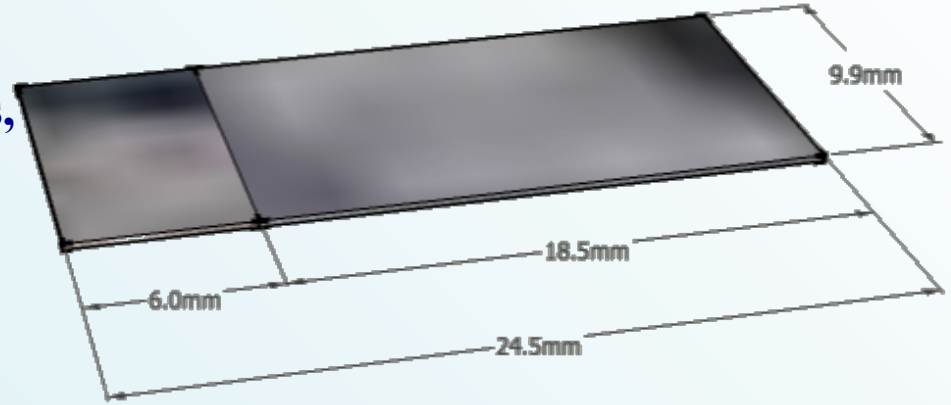
- What will fit better is to reduce the width of the sensor chip to ~10mm.
- Then we would reduce the strip count to 2 groups of 127 strips instead of 4 groups.



- This results in 10 sensor chips across the stave, possibly each serviced by one readout chip.

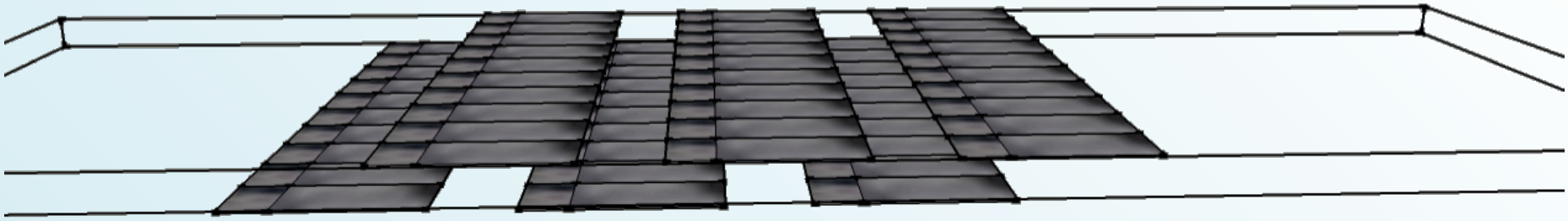
Two Sections of the Sensor Chip

- At the end of the sensor chip, we need an area with peripheral circuitry. (I/O circuits, DACs, encoders, possibly comparators)
- This reduces the length of the strips below the 24.5 mm reticle length.
- We don't yet know how deep this area for peripheral circuitry will be but first guess is about 6 mm.



- This would leave about 18.4 mm for strip length (I'm allowing ~0.05mm as dead region all around the chip and my drawing package seems to cut of at 0.1mm resolution.)
- Given the shorter strip lengths, we may want to consider 16 pixel segments per strip instead of 32.
  - I won't get into that any more for now.

Simplest Arrangement of Sensor Chips on Stave

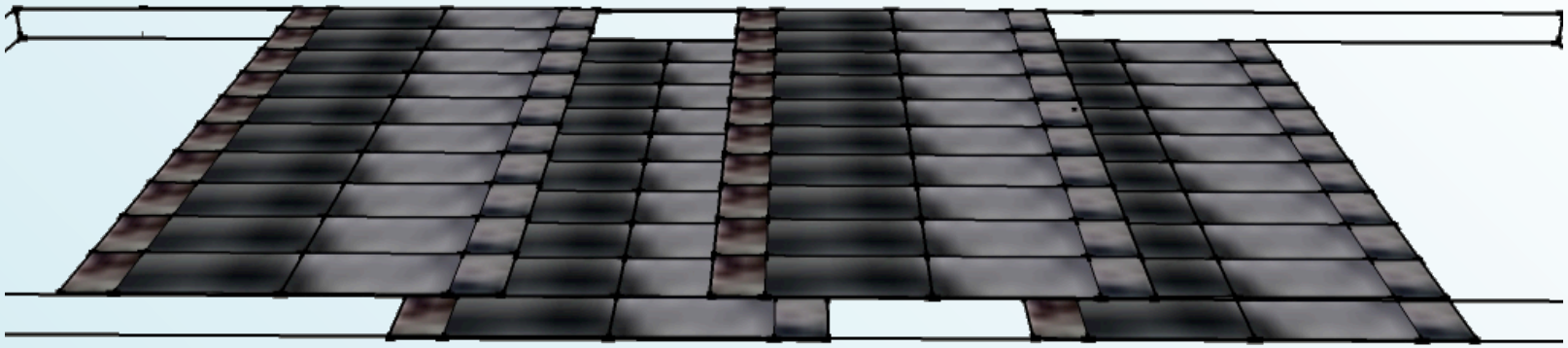


- The picture above shows a row of sensor chips alternating on both sides of the stave.
  - The active strip areas overlap by 1 mm.
  - The areas for peripheral circuitry are covered by the strips on the opposite side.
  - Presumably a hybrid with readout chips would sit above each row of sensor chips and wire bond to pads at the edge of the sensor peripheral area.
- With strip lengths ~ 18.4 mm, this requires ~35 hybrids on each side.
  - Since each hybrid feeds a data uplink, this requires 35 data lines.
  - We currently only have room on the bus tape for 26 data lines.
- To keep the number of data lines $\leq$26, the strip length must be $\geq$25 ($\geq$23.2mm for 28 lines adding just 2).
- The only way to keep the number of data uplinks within bounds is to combine two rows of sensor chips into one uplink, i.e. one HCC.
- Also, with this arrangement we only save ~34% of the silicon area due to the area for peripheral circuitry.
  - This savings will increase if the peripheral area decreases.

One Arrangement to Reduce Data Uplinks

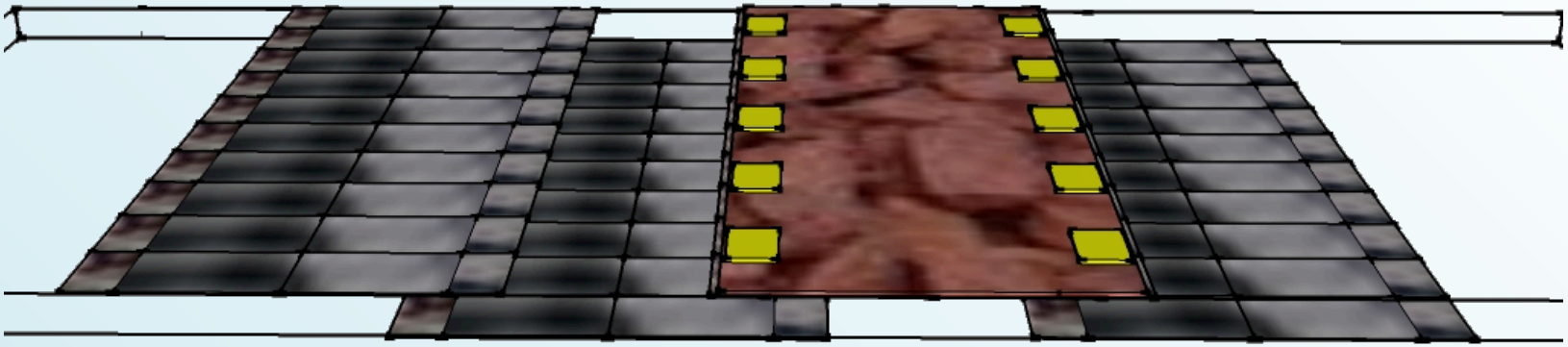
- This was my first idea to reduce the number of hybrids and HCCs.
- Two rows of sensor chips are placed such that their peripheral areas adjoin allowing one hybrid to service both rows.
  - A problem is created, however, because this requires one row of sensor chips on the back side to shadow the double peripheral area on the top and results in the staggered arrangement of a double row followed by a single row on each side.
  - We end up with either two types of modules or one extended module that includes three rows of sensor chips.
- The "modules" are also not mechanically rigid unless one includes some sort of backing underneath the sensor chips, adding more material and possibly reducing thermal contact to the stave.
- This does result in 26 hybrids on both top and bottom sides, half are double row hybrids and half are single rows.

Double Sensor Row Reduces Hybrid/Link Count



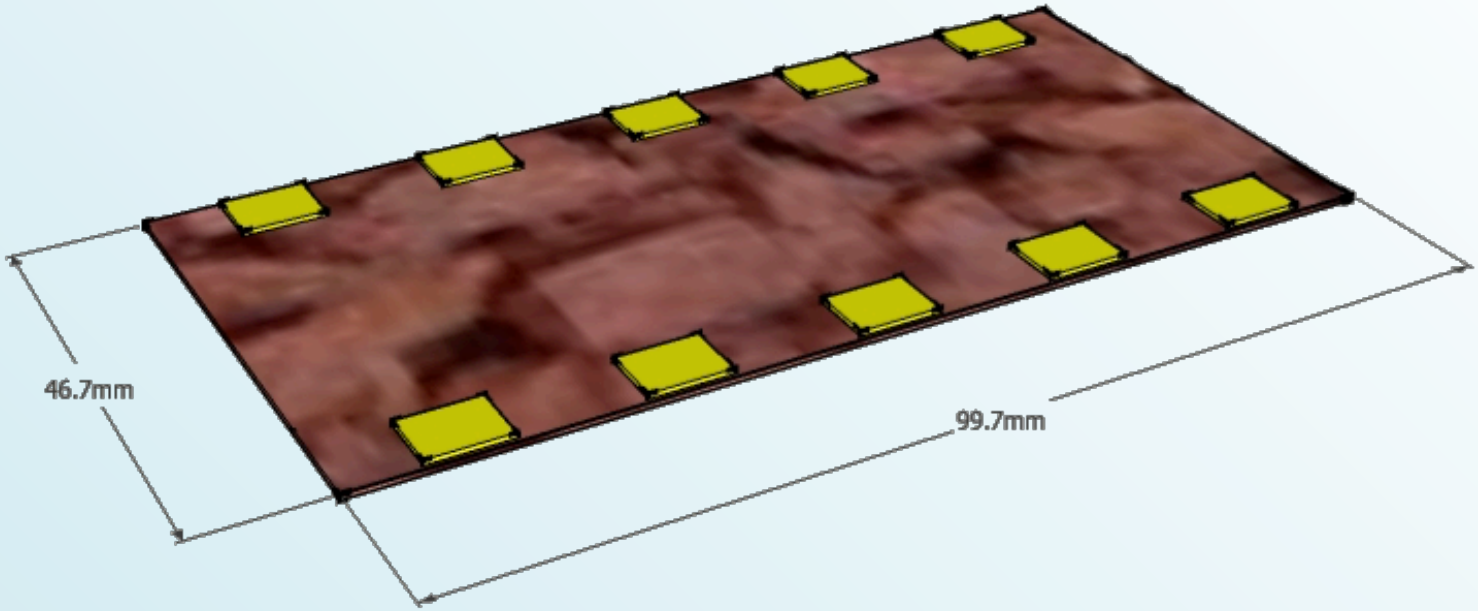
- Richard Nickerson proposed a better double row module arrangement.
- Strip ends butt against each other; peripheral circuitry is on the outer edges.
- Strips on the opposite side shadow the peripheral area.
- Assuming a strip length of 18.55 mm and 1 mm overlap of strips on the opposite side, there are 18 double row modules on each side of the 1300mm stave.
- There will be a dead gap where the strip ends of the sensor chips butt against each other but not any worse than the edges of the baseline planar sensors.
  - And likewise dead gaps where each sensor chip touches an adjacent sensor chip across the width of the stave.

Module = Double Row of Sensor Chips with One Hybrid



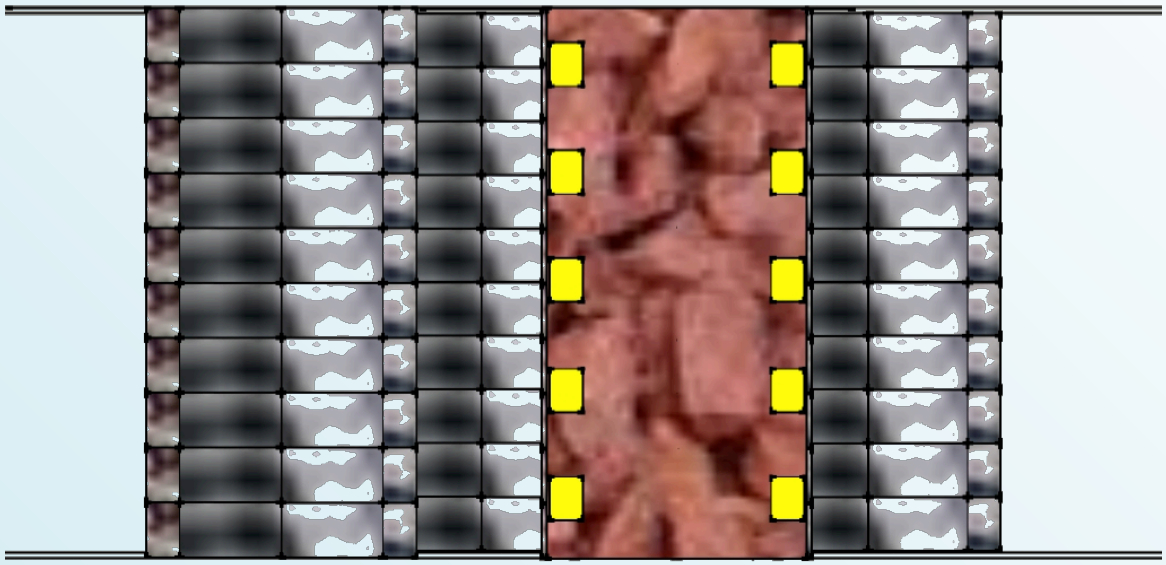
- This picture shows a hybrid on top of one double row of sensor chips along with 10 readout chips.
  - 10 readout chips should be able to handle the occupancy of a double row of sensor chips as this is slightly less area than covered by one 10-chip hybrid in the baseline design.
  - The 10-chip arrangement is consistent with the HCC now in design.

Hybrid



- The hybrid is wider than the baseline hybrid as it covers two full rows of sensor strips.
- However, since it will be difficult to couple one power board (containing DC/DC converter, HV switch, etc.) to two hybrids, propose to place one power board circuitry in the middle of each hybrid.
  - This may be useful to provide the extra power needed for the HV-CMOS circuitry.
- Need to investigate stiffening material for the hybrid so that it becomes the structural support for the array of sensor chips prior to mounting on the stave.
- Nearly the full top side face of each sensor chip would be glued to the hybrid on top.

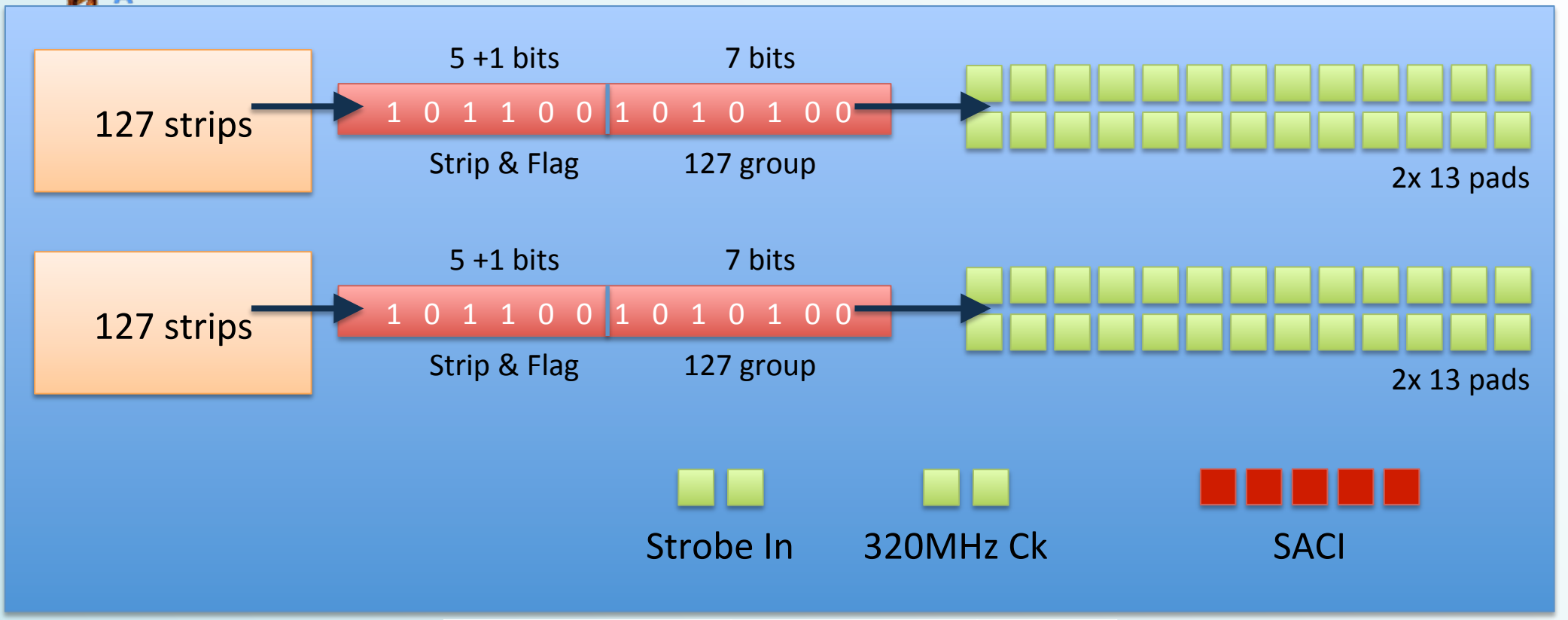
Wire Bonding Issue to Resolve



- This picture shows the hybrid covering one double row of sensor chips on the top side and the back side of the sensor chips on the bottom side of the stave. (The stave structure is transparent.
- This points out an issue with the bonding pads.
  - One readout chip services two sensor chips but the present ABC is only 7.9 mm wide.
  - Even though we expect fewer bond wires, can we fit the needed number in the edge of the sensor chip lined up with the readout chip.
  - A possibly bigger issue is that the opposite corner of the two sensor chips lines up with the readout chip.
    - How can this work?
    - Can the sensor chip include two copies of each bond pad at opposite corners?

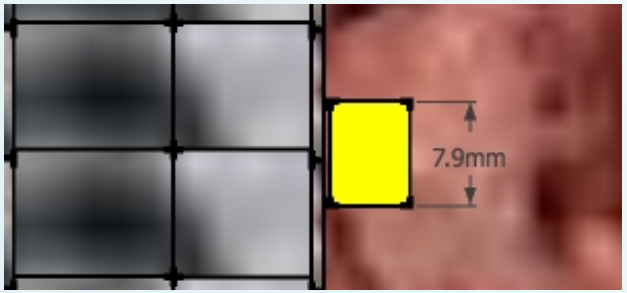
Interface to ABC

from Hervé



	Nb of pads	
2x 127 strips	2x26	52
Strobe in	2	2
SACI	5	5
320MHZ Ck	2	2
Total		61

Wire Bonding Issue to Resolve



- The designers are looking into having two sets of pads on each sensor chip at opposite corners of the back of the peripheral area.
- But can all the pads fit?
- The present ABC130 is 7.9mm wide – assume ~0.050mm gap between pad and chip edge, the pad area at the front-end would be about 7.8mm wide.
- From the previous slide, each sensor chip requires 61 pads (66 if the SACI interface must also be differential).
  - This implies 2 rows with up to 31 pads (33 pads for 66 total).
- Using only half the ABC front edge (3.9mm) yields a pad pitch of ~0.126mm (~118mm for 66 pads) in each row, which is comparable to the present ABC which has 4 rows.
  - This reduces the number of wire bonds from ~256/ABC to ~122. (~132).
- I assume for now that power and ground can be supplied directly from the hybrid and not from the ABC.