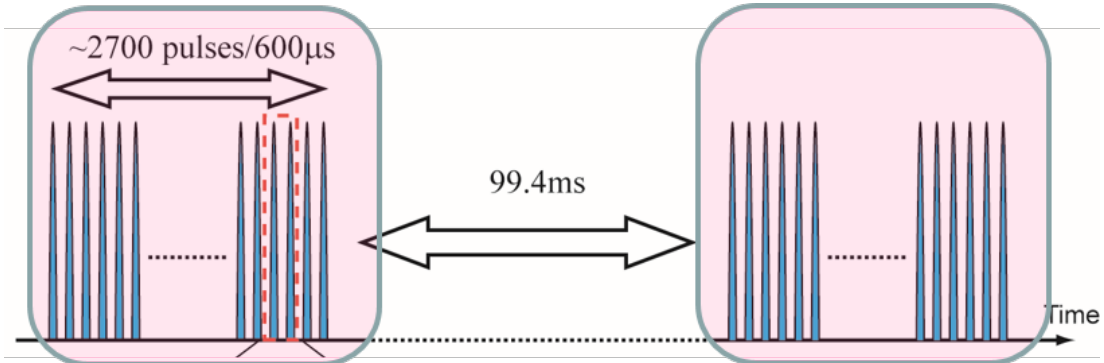
Status of the DSSC Project

Matteo Porro

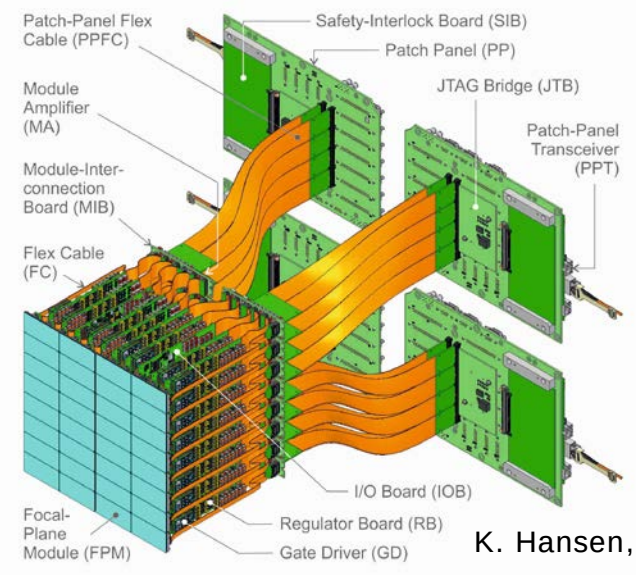
For the DSSC Collaboration

Sensor and focal plane architecture

- Non Linear DEPFET
  - Intrinsic low noise
  - Intrinsic signal compression
- Mini SDD array
  - Linear response
  - Simplified technology
- Readout concept
  - Full parallel readout
  - Analog shaping
  - **8-9 bit digitization in pixel**
  - **In-pixel SRAM (800 frames/bunch)**
- Power cycling
  - 10.7 kW peak power
  - 240 W average power



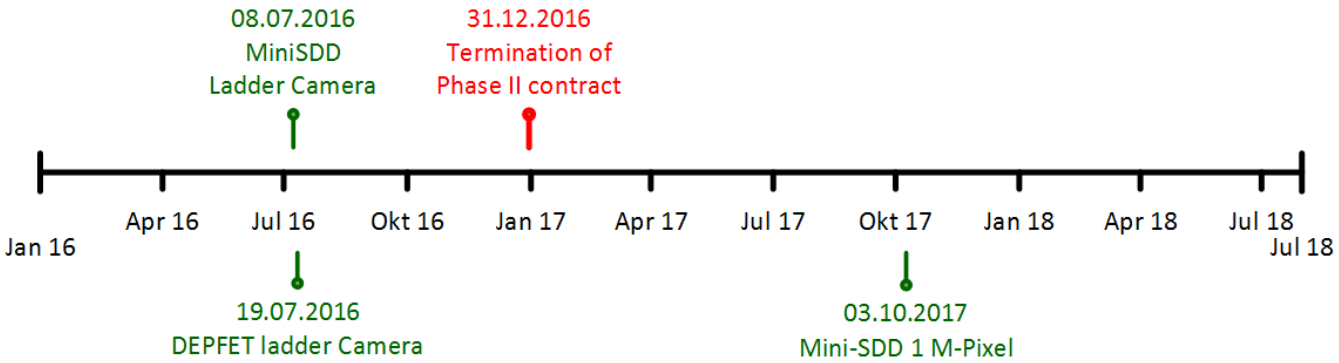
- Focal Plane composition
  - 1024x 1024 pixels
  - **16 ladders (512 x 128)**
  - 32 monolithic sensors 128x256
  - 256 Readout ASICS 64 x64

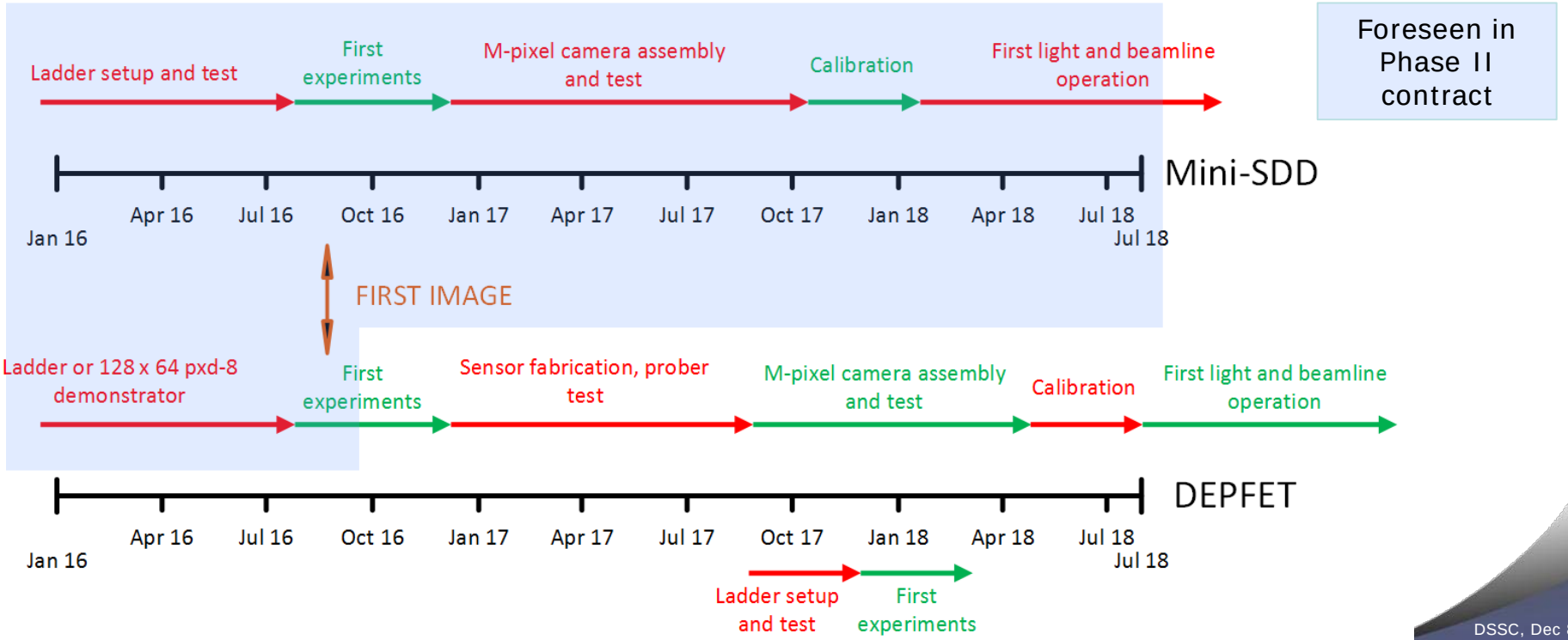


K. Hansen, DESY

- Mini-SDD camera by end 2017
- **Two ladder cameras (Mini-SDD and DEPFET) by middle of 2016**
- DEPFET camera to follow

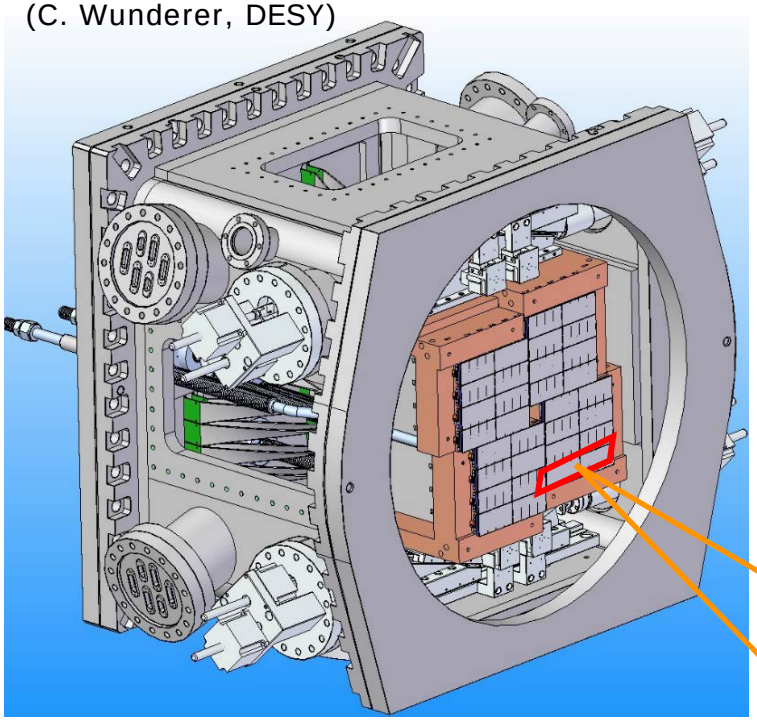
Time plan - overview



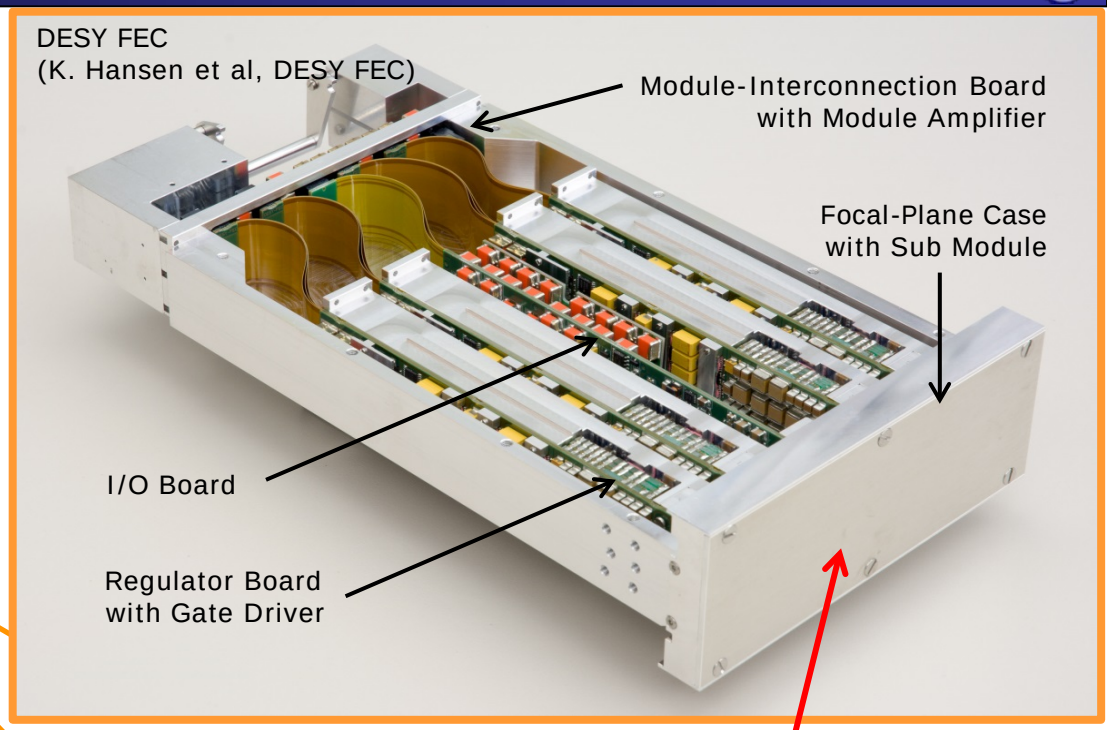


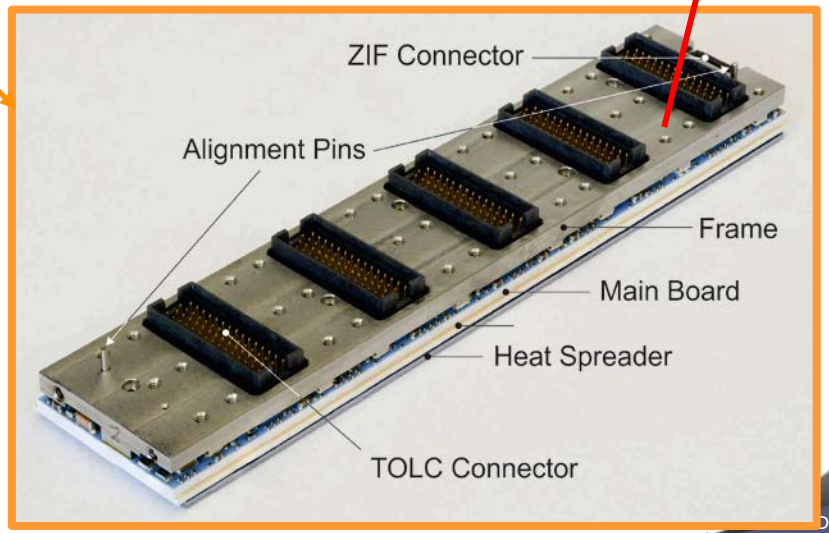
DSSC ladder camera

(C. Wunderer, DESY)



DESY FEC
(K. Hansen et al, DESY FEC)



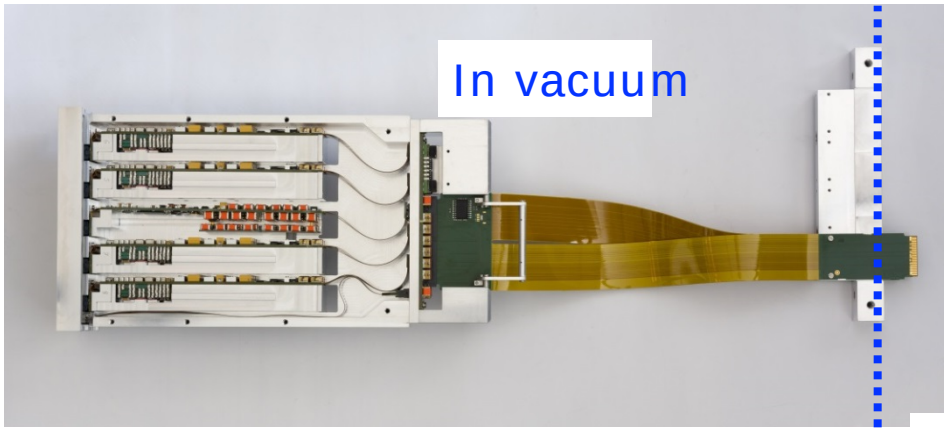


Mini-SDD and DEPFET based systems (512x128)

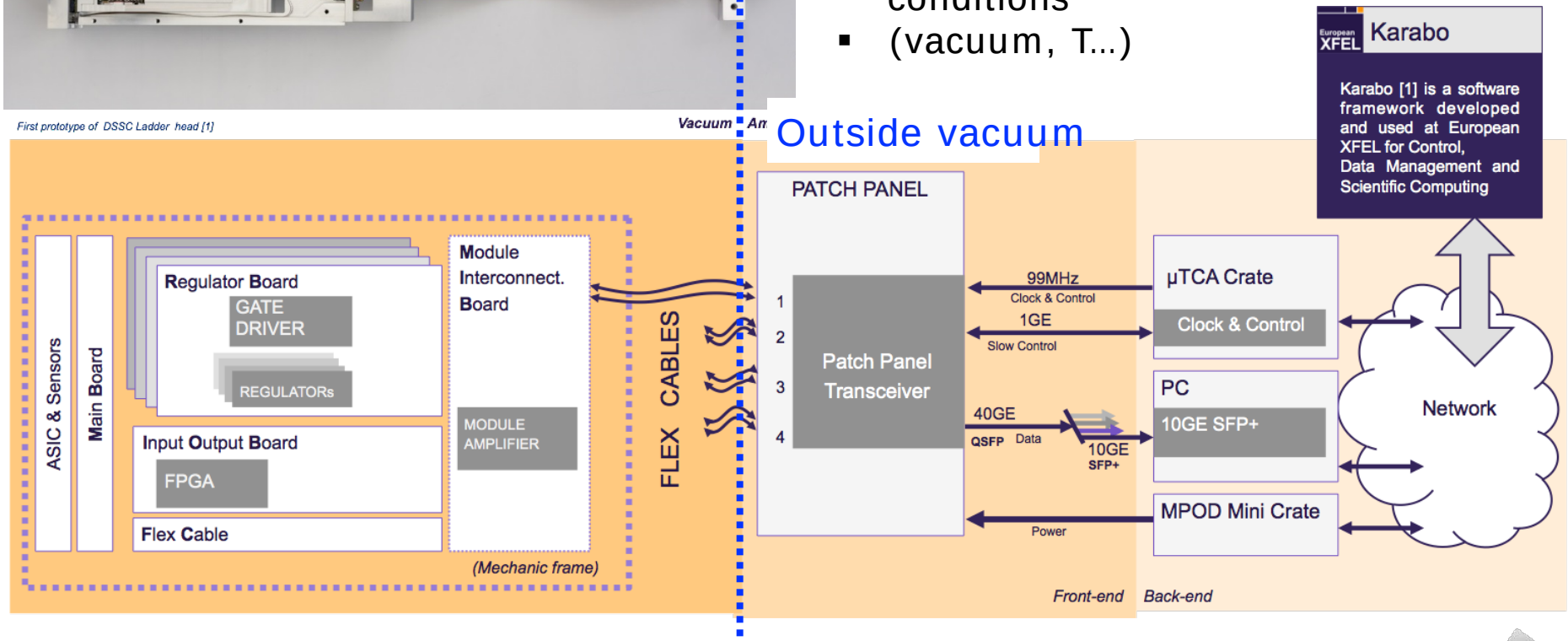
⇒ ladder test-stand

⇒ ladder cameras

Ladder prototype and backend electronics

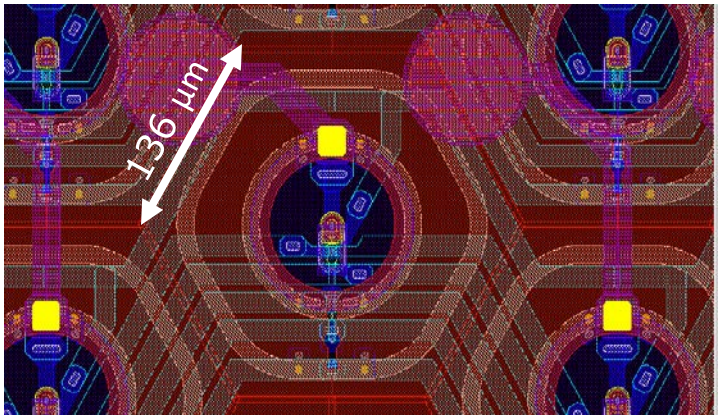


- 128x512 pixels
- Full electronic chain as in final camera
- Full integration into the XFEL.EU software frame
- To be operated in the same conditions
- (vacuum, T…)

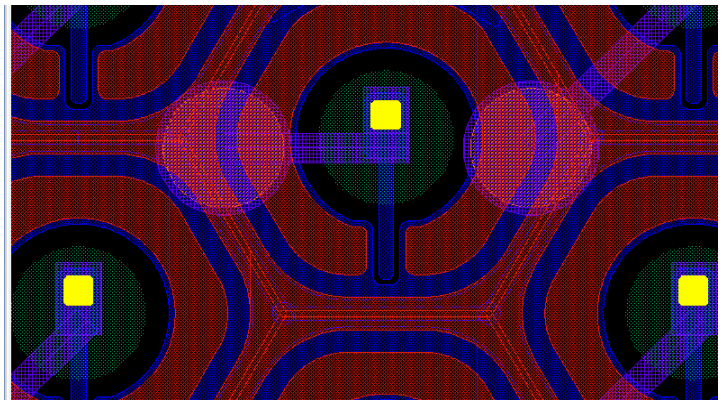


(M. Donato - XFEL.EU, K. Hansen – DESY FEC, A. Kugel, M. Kirchgessner – Heidelberg)

Mini-SDD sensor motivations and main characteristics



DEPFET (PNSensor, MPG HLL)
- 2x poly, 2x Al, 1x Cu
- 11 implantations



Mini-SDD (MPG HLL)
- 1x Al, 1x Cu
- 2(3) implantations

- **Large area DEPFET arrays will be used to build detector ladder cameras** (512 x 128 pixels)
- For the full camera an additional DEPFET production is needed
- We need an increase of availability of DEPFET sensors with reduced production time establishing an industrial fabrication process (accomplished by PNSensor)
- **A simplified sensor has been produced**
  - mini-SDDs with passive collecting anode
  - Same geometry of DEPFET devices
  - Linear response
- the mini-SDD sensor has reduced performance but it will allow one to:
  - Test the full-system in advance
  - perform a large fraction of the foreseen experiments at low energy

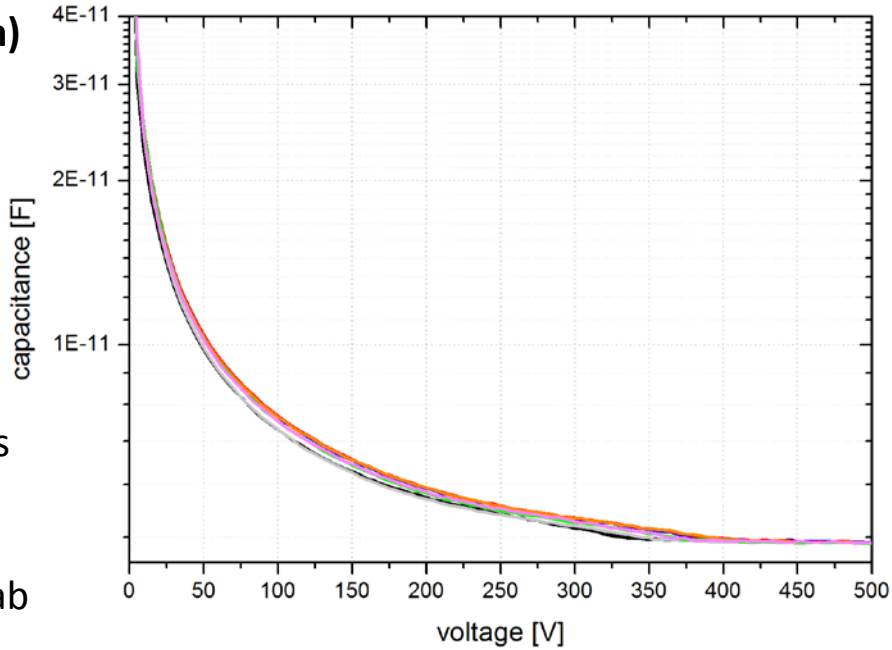
DEPFETs in Industrial-Scale CMOS Fab

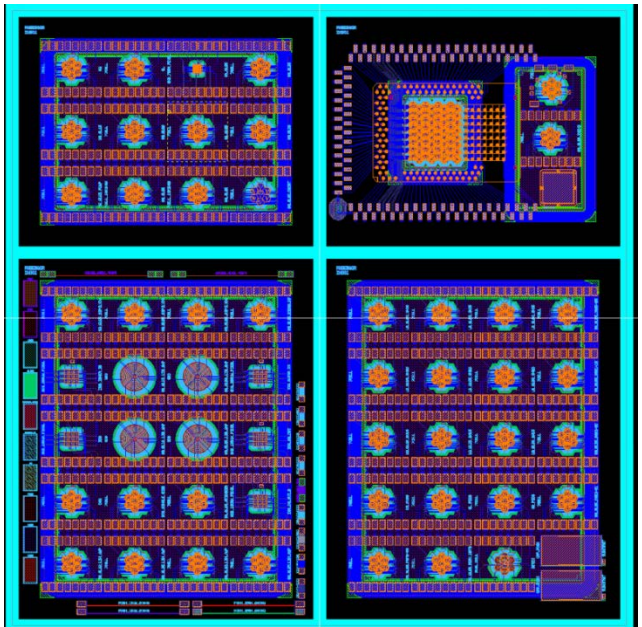
First production of diode test structures (12 wafers 8 inch)

- Large Diodes 5x5 mm^2
- Small Diodes 1x1 mm^2
- Technology test structures

Test results

- Depletion voltage is below 400 V
- Leakage current is typ. < 1 nA /cm2 at full depletion
- Distribution of leakage current is homogeneous across the wafer
- Double sided processing of DEPFET devices with very sensitive entrance windows is possible in the CMOS Fab

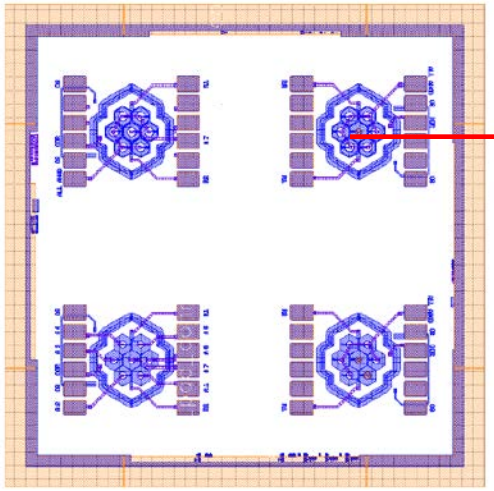




- First DEPFETs will be available in **April**
  - 7-cell clusters
  - Macropixels
  - 3x3 matrix (smaller pixels)
  - 8x8 matrix (UBM required)

Verification of MiniSDD functionality

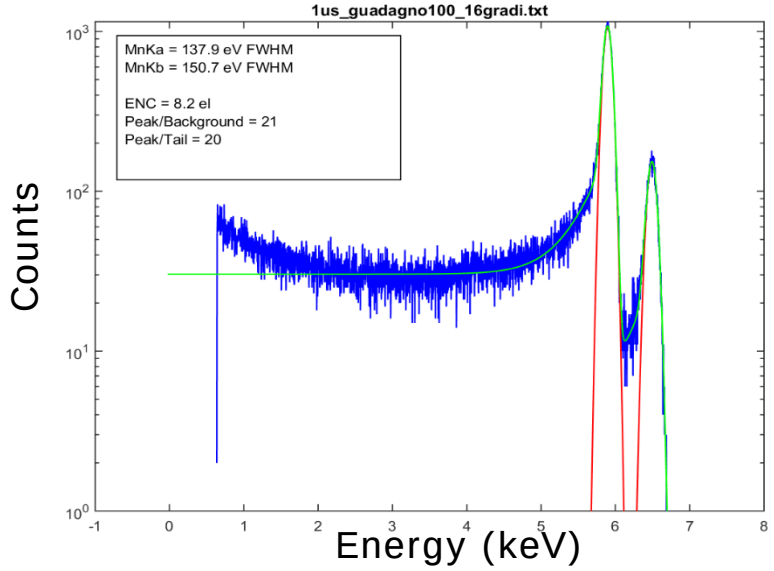
The functionality of the MiniSDD pixel has been verified with CUBE external charge preamplifier:



- Test made with four shaping times: 1 us, 500 ns,375ns and 250 ns
- Two different temperatures : 16° C and -10° C
- Test leaving floating the Ring1 at 16° C

ENC summary

Shaping time (ns)	T=16° C	T=-10° C	R1 floating (T=16° C)
1000	8.2	7.3	8.2
500	8.6	8	9.1
375	9.2	8.4	9.8
250	9.7	9.4	10.4



ASIC - Reminder: DEPFET vs. Mini-SDD

- Originally **DEPFET** sensors + Low impedance **current mode input FE** were chosen by DSSC because this combination solves several challenges:
  - low noise (low input cap, internal amplification)
  - high compression (increasing cap. of internal gate with fill level)
  - low crosstalk (primary charge confined to internal gate, low Z_{in})
  - power supply rejection

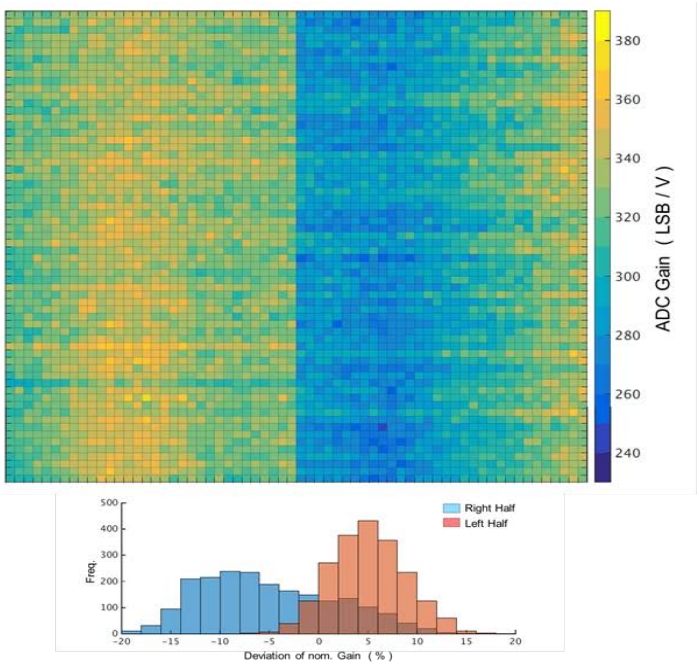
- After withdrawal of MPE / HLL from DSSC, we **had to** move to Mini-SDD
- All above challenges **must now be handled in the FE**, which puts additional burden on the FE.
- This challenging FE had to be implemented in fairly short time.
- The FE version in F1 was only a first shot

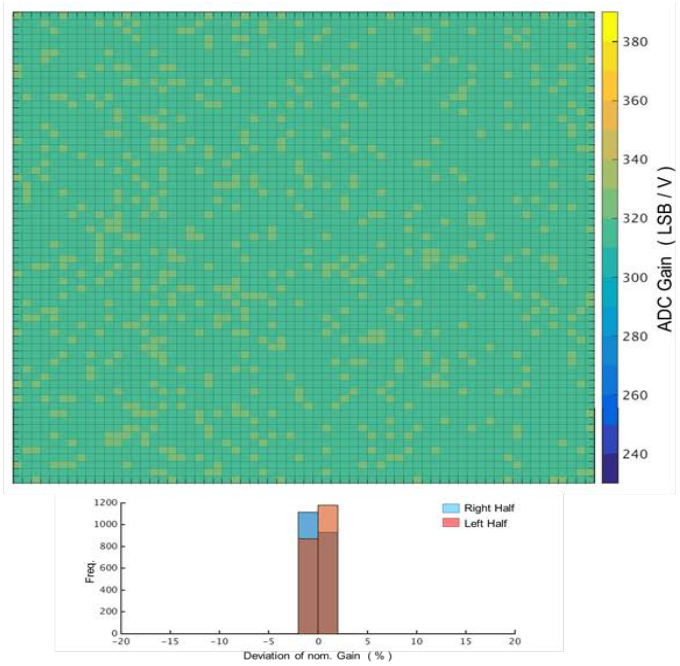
- F1 (containing both FE types) has still sub-optimal performance for Day-0
- It will be used for the first focal ladder cameras (128 x 512)
- We are working on a better Day-0 FE for the planned F2 chip

- As new DEPFET are planned for the future, we need to go in parallel…

F1 (64 x 64) ASIC - ADC Operation

- ADC can be operated on FULL chip in parallel.
- Gains can be trimmed to nominal value:



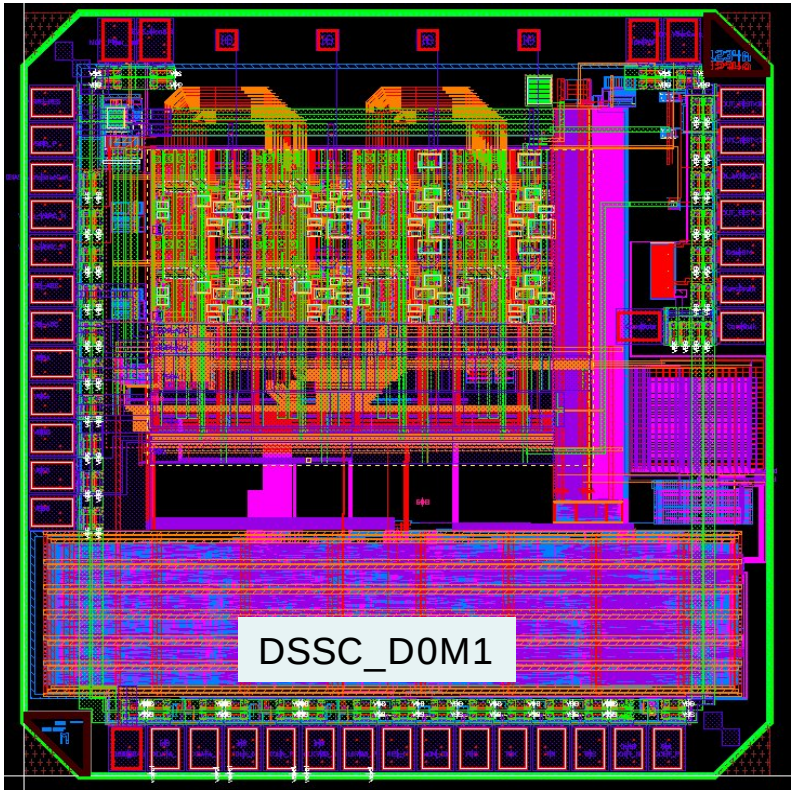


- Gain variations are well understood by simulations including voltage drops
- 99% pixels have DNL (in range of 20 bins) < 0.5 LSB
- 25% trim range is required for this. If nominal gain is trimmed, required trim bins are not centred, so that low contingency is left on 'one side'

ASIC - New Designs

- New design ideas have been invented to address the problems of
  - power supply sensitivity
  - Matching
  - (compression)

- A test chip DSSC_**D0M1** with 2 x 4 pixels has been submitted in August
  - It will be back in Mannheim 7.12
  - It contains 3 types of FE



- A test setup is very similar to previous test chips & ready

- A MM7 8 x 16 ASIC with the pixel electronics foreseen for the final large format ASIC will be submitted in February 2016

- The final F2 64 x 64 ASIC will be submitted in July 2016

Module WP - assembly

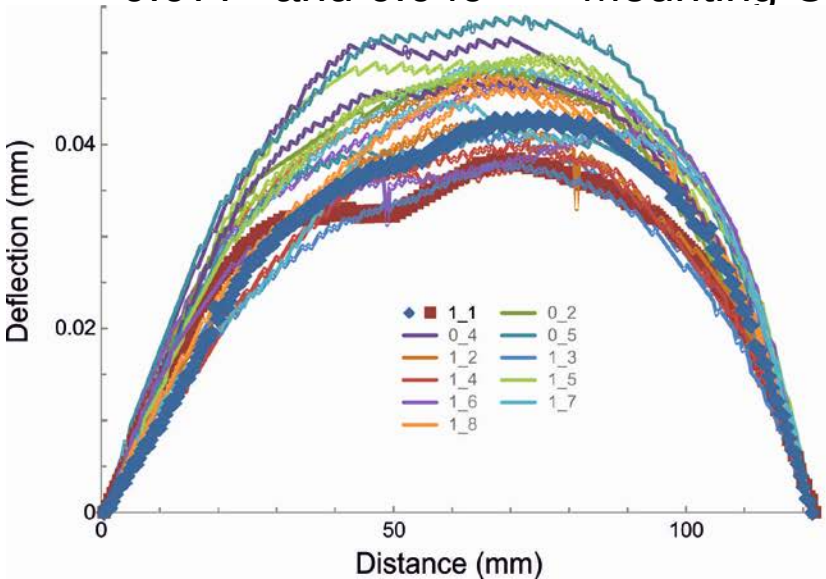
Bare Module Assembly – Flip Chip

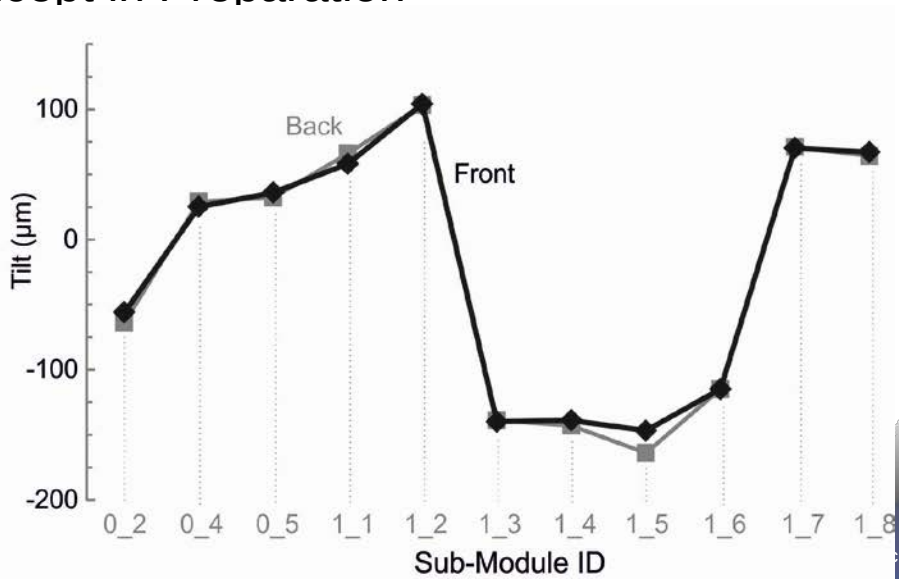
- The Flip-chip process development has started and it is still in progress. Cu UBM Quality is a Problem for both Productions, PXD-8 & mini-SDD

- We successfully flipped 2 samples of 64 x64 MiniSDD sensors and the backside protection has been verified.

Sub-Module

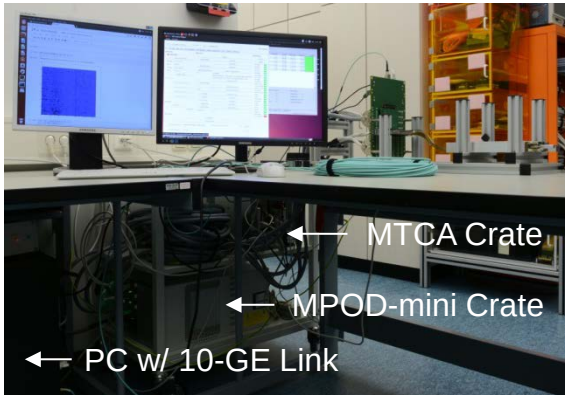
- Sub Modules shows Deflections around 46 µm & Tilting Angles between -0.077° and 0.049° → Mounting Concept in Preparation



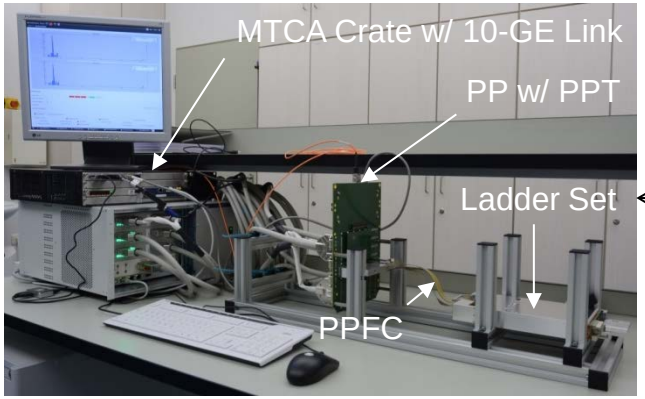


Ladder Systems

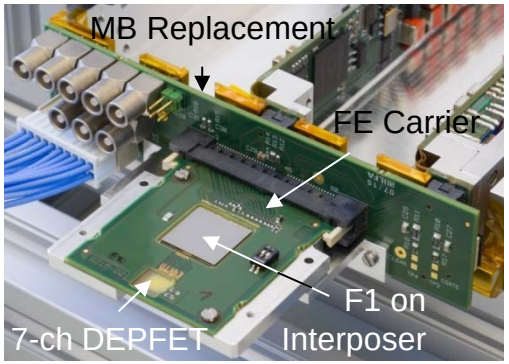
Lab-Test System



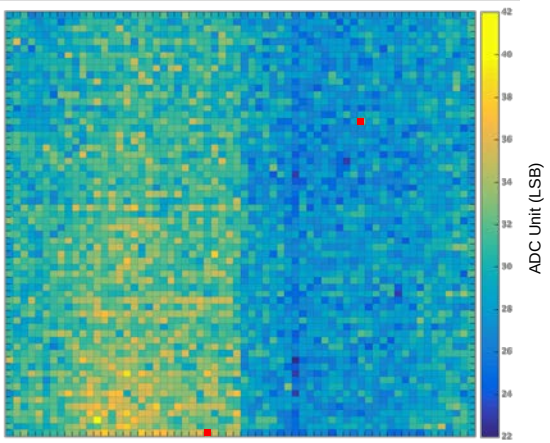
Ladder Camera

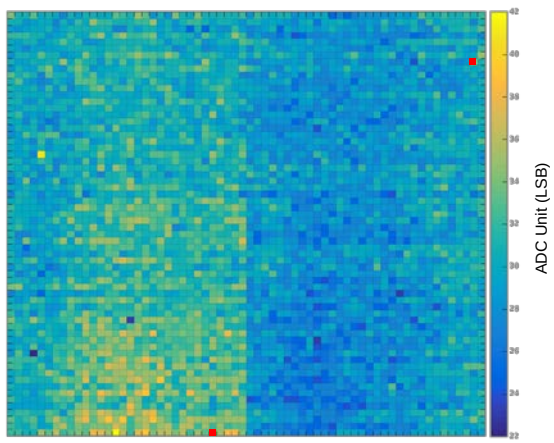


DUT



Dark Images





Current Sink: Off
FE: Buffer Mode
I_{ramp} Setting: 13

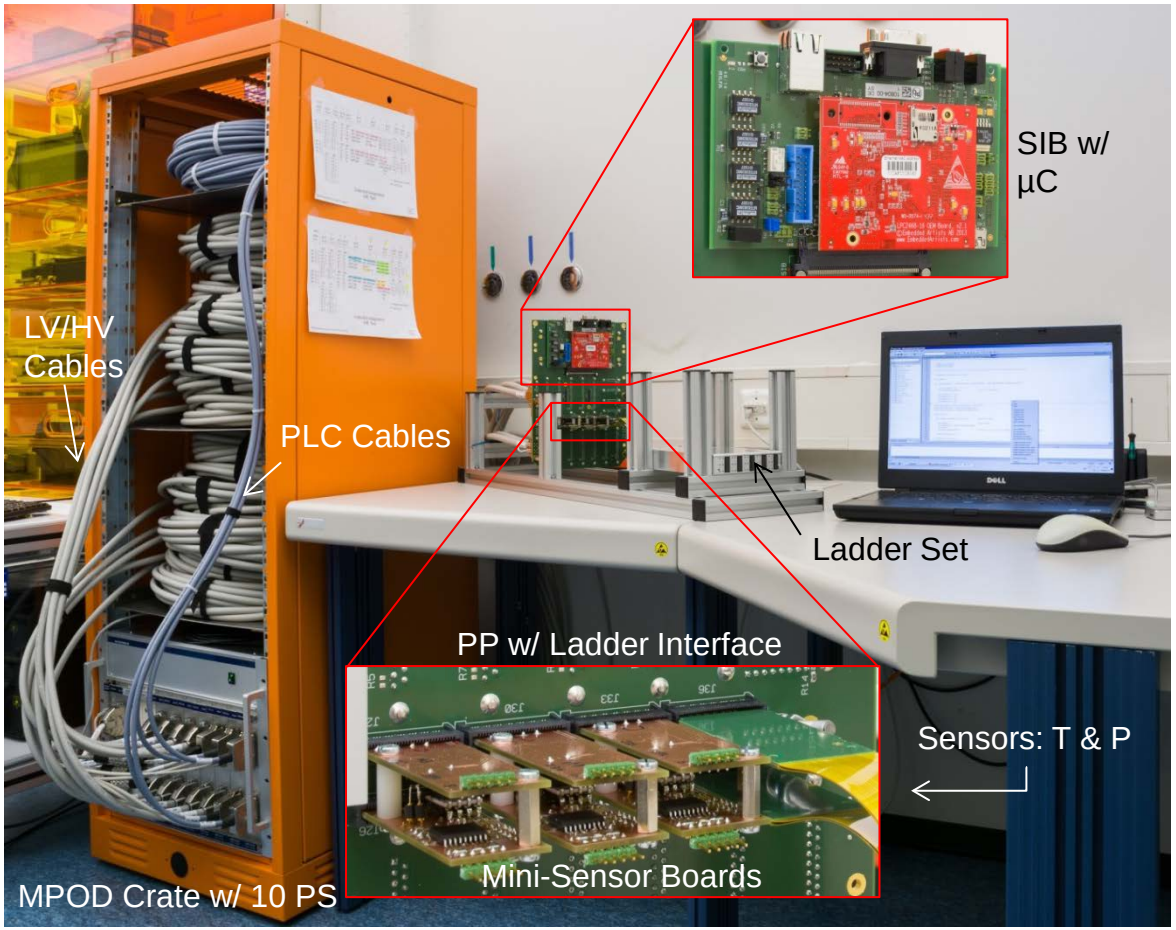
■ *defect Pixel*

Next Steps

- *Tests with 7-ch DEPFETs*
- *wait for FE Carrier for Baby-Bare Modules*
- *Tests with Baby-Bare Modules*

- *whole Signal Chain from ASIC Filter to Back-End Computing works*
- *two F1-Chips show 2 defect Pixel each, one F1 Chip without defect Pixel*

Quadrant-Test Stand



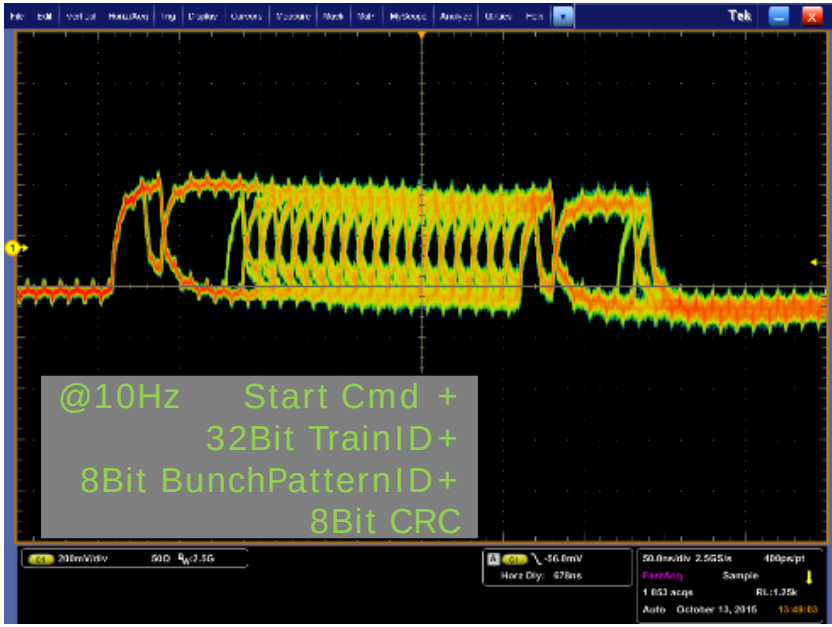
- *whole Power/Signal Chain from Crate to Camera-Head Interface works*
- *SIB's Main Functions successfully tested*

Next Steps

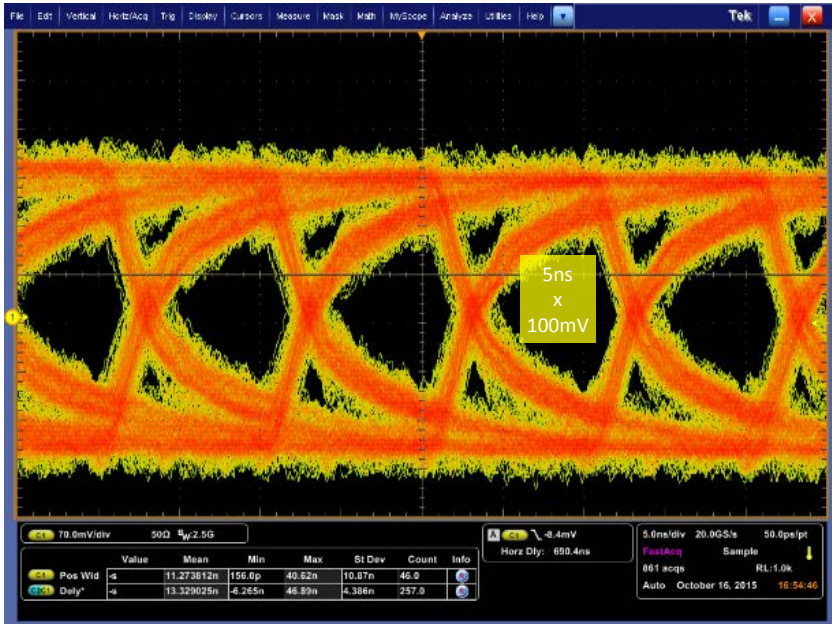
- *Implementation of PPT & IOB*
- *Temperature-dependent Measurement with SIB's Sensors*

DAQ

- 3 out of 10 PPTv2 boards have been produced
  - ➢ One minor termination bug was solved by a small patch board mounted on the bottom side of the PPT
  - ➢ This patch will be integrated in the bottom layer of the PCB for the remaining 7 PPTv2 boards (change of one mask only)



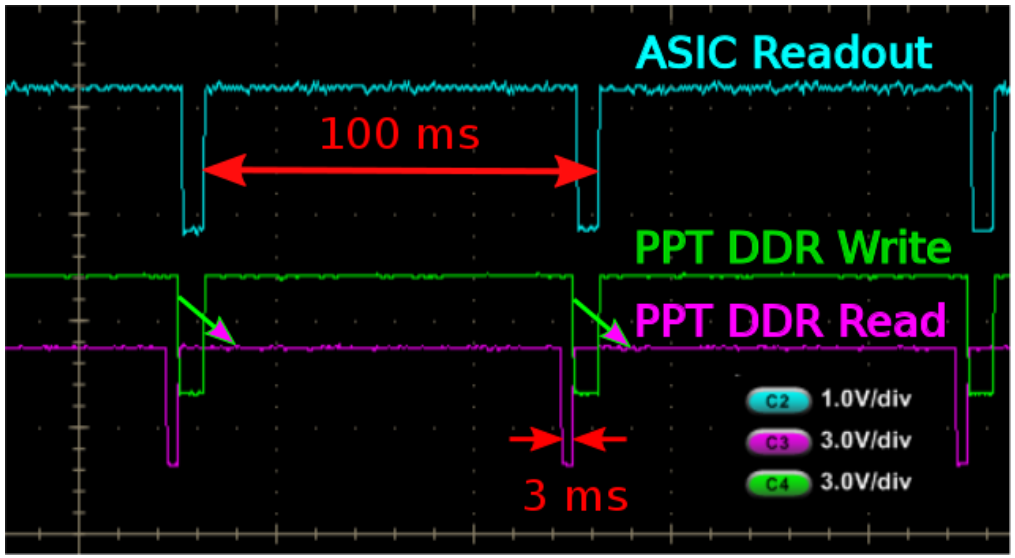
- C&C signal quality has been successfully verified (with patch board) @ 100 MHz operation:
  - ➢ 30m cable (CAT6, CAT7 same)
  - ➢ Eye-opening fits LVDS spec. of 100mV
  - ➢ Bit Error Rate Test (Random pattern) ~ 5.35E-12



DAQ - 10 Hz Operation Mode

- All burst and readout state machines in ASIC, IOB and PPT have to run synchronously
- All Fifos and SRAMs have to be reset/initialized before each burst
- Readout chain must have finished before next burst
  - Per 10Gbit Link: 16 chips x 4096 pixels x 800 words x 16 bit = 838.860.800 bit

    Link capacity in 94 ms (no headers…): 940.000.000 bit



10 Hz operation with C&C signals **runs stable**

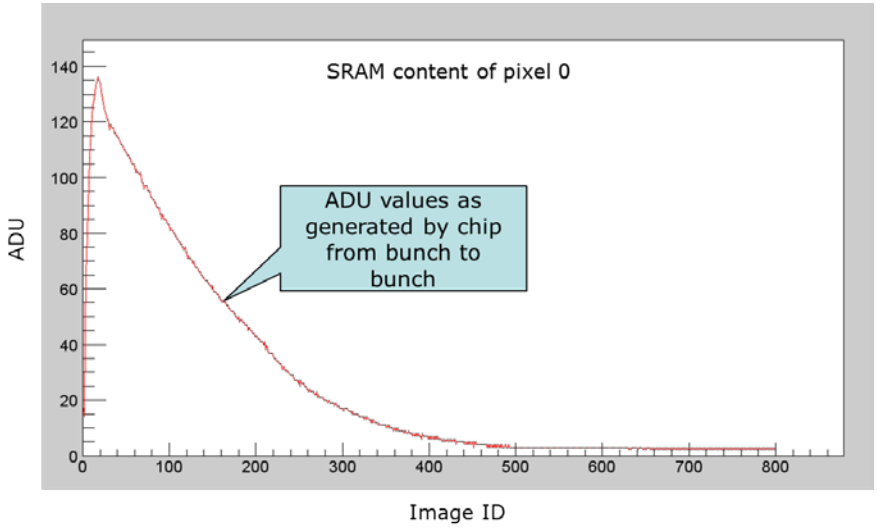
green: PPT receives data from ASIC and writes it to DDR3 buffer

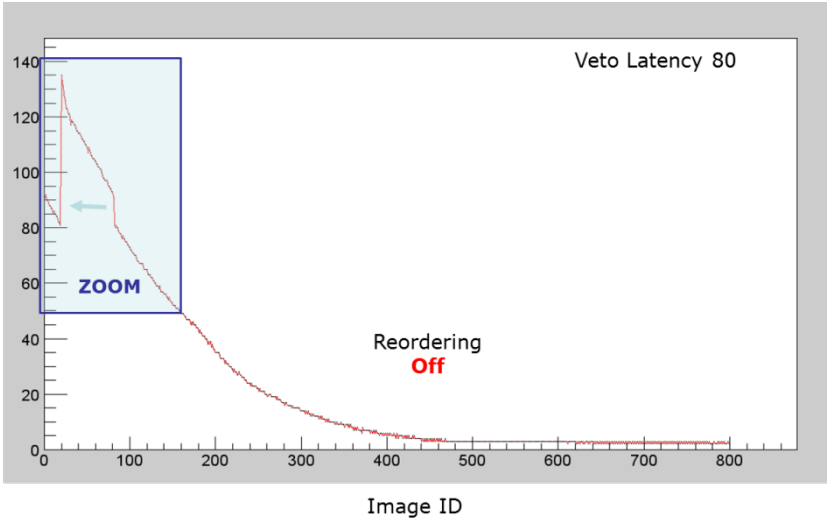
purple: PPT sends (reordered) train data from DDR3 to train builder

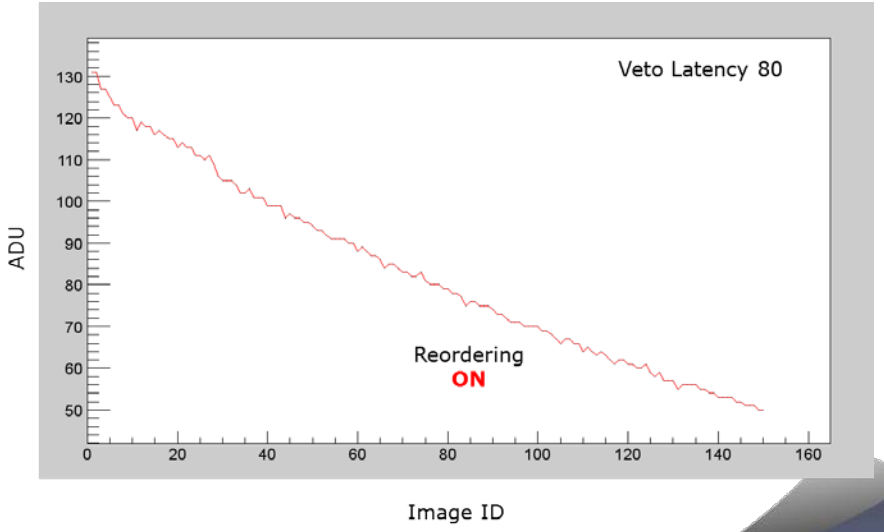
DAQ - Veto & reordering

Real hardware has been used to test Veto Mechanism in detail:

- Full readout chain including the readout ASIC is included
- Start triggers have been received in 10 Hz rate
- F1 ASIC operated with rapidly changing ADC values to visualize the veto correction
- Veto signals generated
  - internally (in ppt, at the beginning of a burst)
  - from C&C via veto command

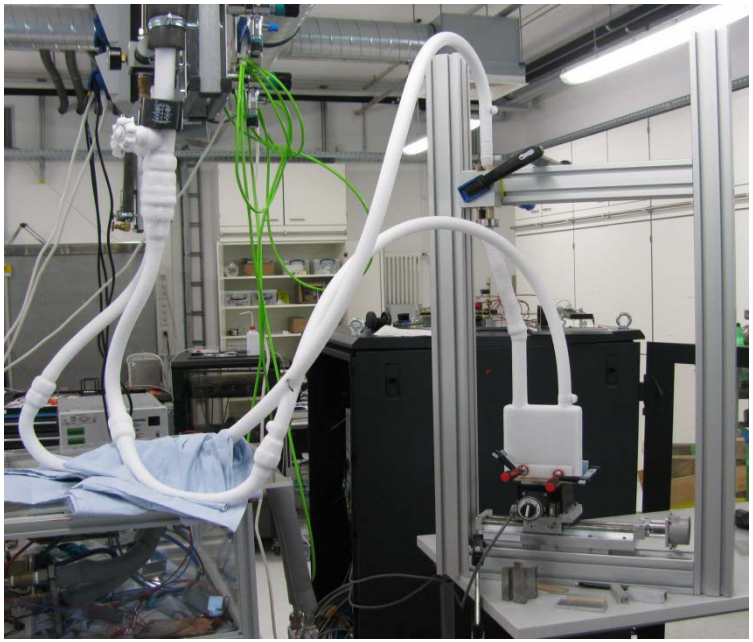




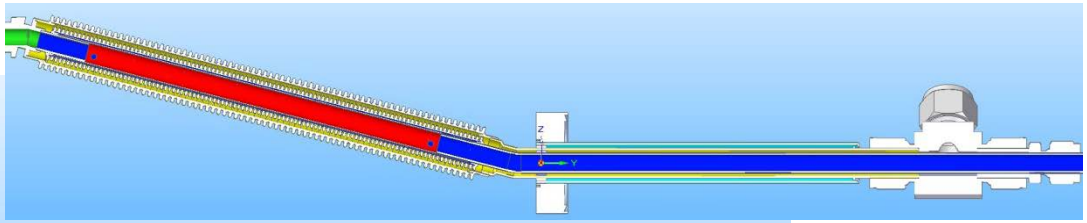


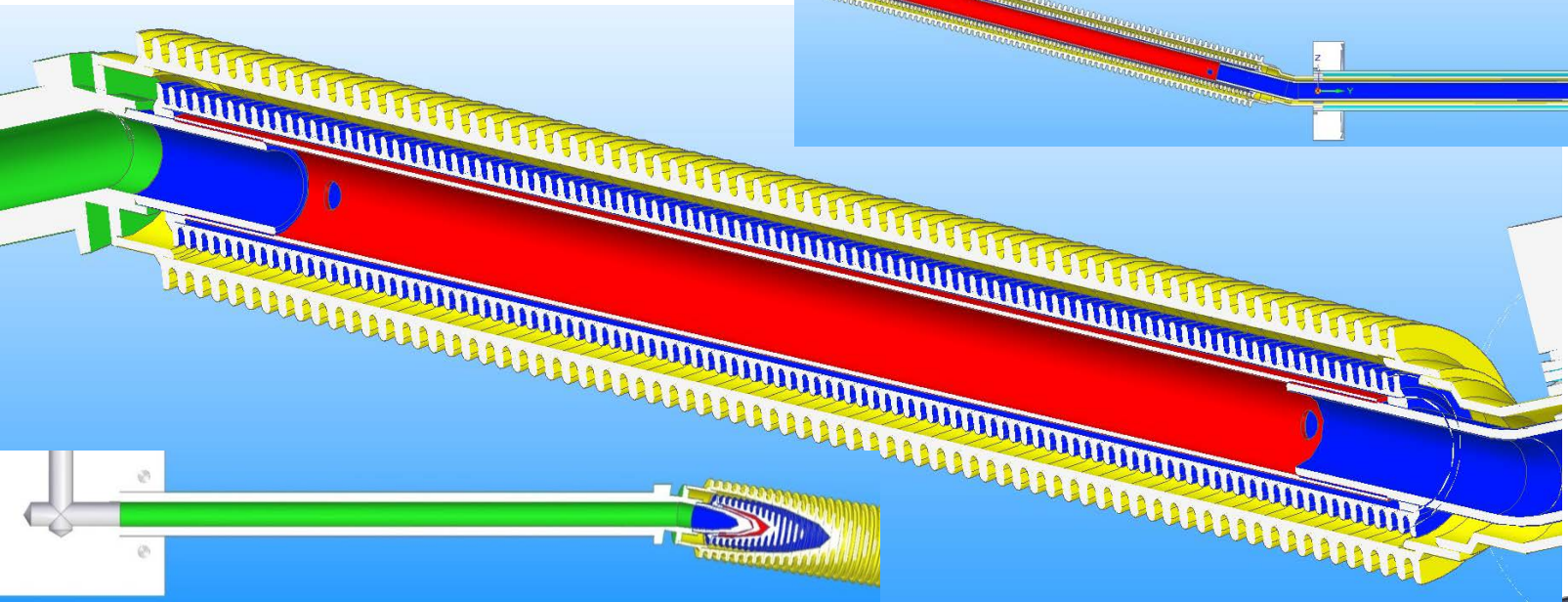
Veto-reordering was also verified in digital simulation.

Thermal/Mechanics 1/2



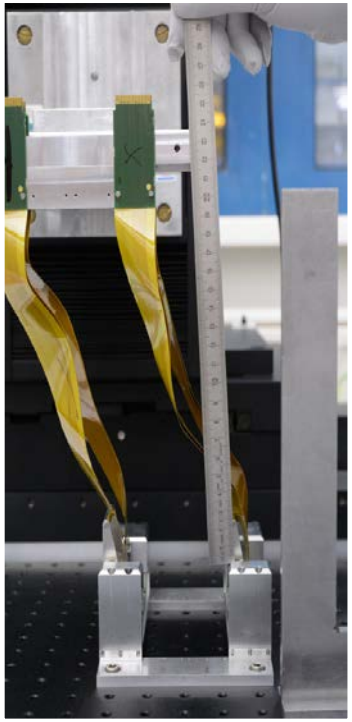
- The coolant pipe architecture is fully qualified
  - 100 cycles warm => passed vacuum check afterwards
  - 2000 cycles moving along outer edges of a 14×14mm^2 square with coolant (-60°C at outset) circulating inside => again passed vacuum check afterwards





Thermal/Mechanics 2/2

- 1:1 Mock-up used for verifications
- In June 2015, attempts to place the Patch Panel Flex Cables (PPFC) revealed mismatch between PPFC and chamber design length
  - ➢ Flex cables will be made longer (~5.5 cm)
  - ➢ No need to change the vacuum chamber design
  - ➢ No need to move cooling pipes



Next Steps:

- ➢ finalize fabrication drawings & order cooling blocks
- ➢ finalize “Pflichtenheft” for the vacuum vessel & get that ordered
- ➢ (XY motion stage has already been ordered)

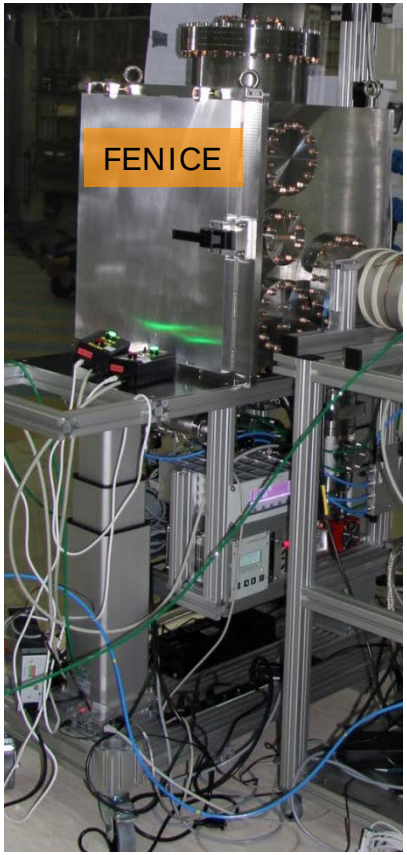
- ➢ We try to learn as much as possible from AGIPD mechanics implementation before placing orders for DSSC components

DSSC ladder vacuum test stand, FENICE

FENICE installed, vacuum system working (best reached pressure ~ 5 x 10^{-7} mbar).

Cooling system ready to be switched on

First tests on PLC performed, stages move.



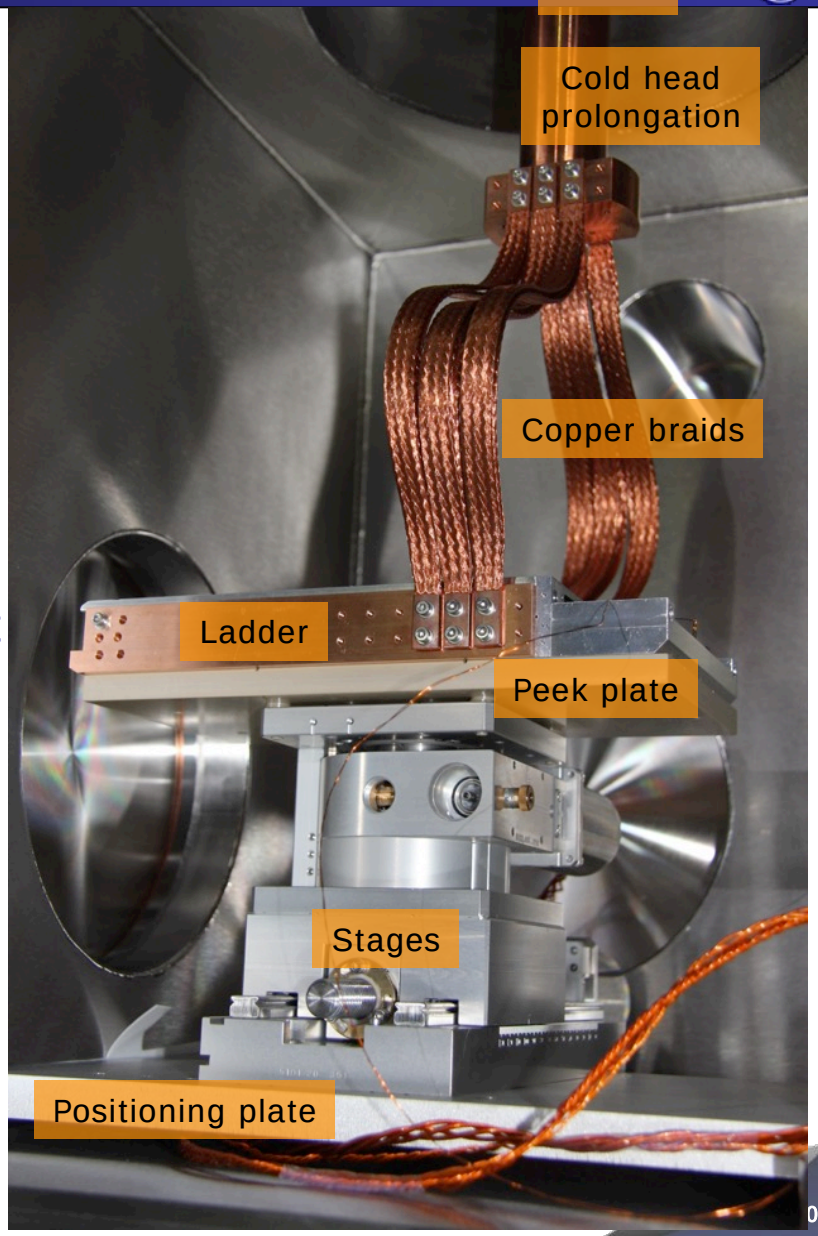
Inside FENICE:

Stages, insulating plate,

ladder mechanics (from FeC)

copper braids to the chiller

Flange with electronic feedthrough assembled with FeC



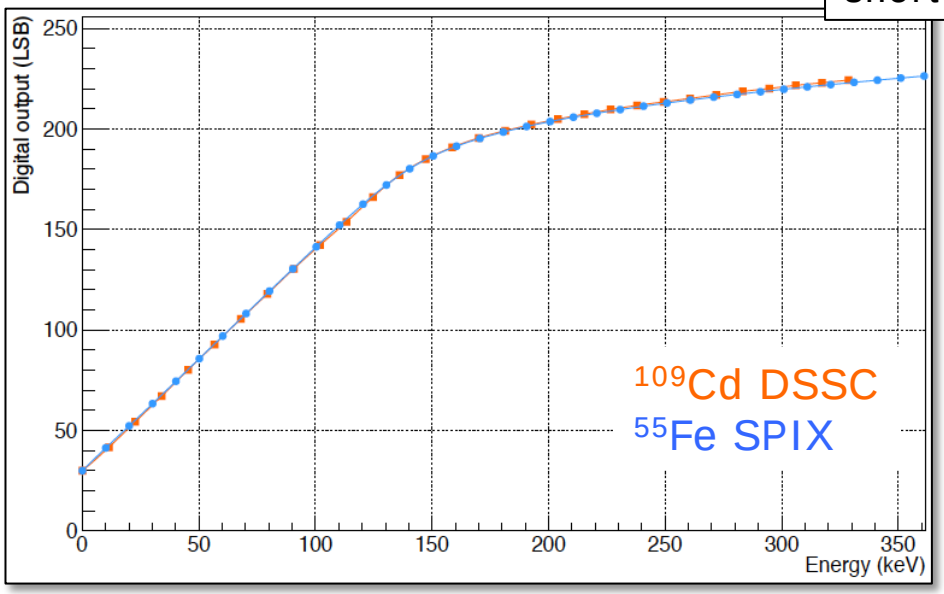
Experimental Calibration of Non-linear System Characteristic II

NLSC: non-linear relation between signal charge collected in DEPFET pixel and corresponding digital output

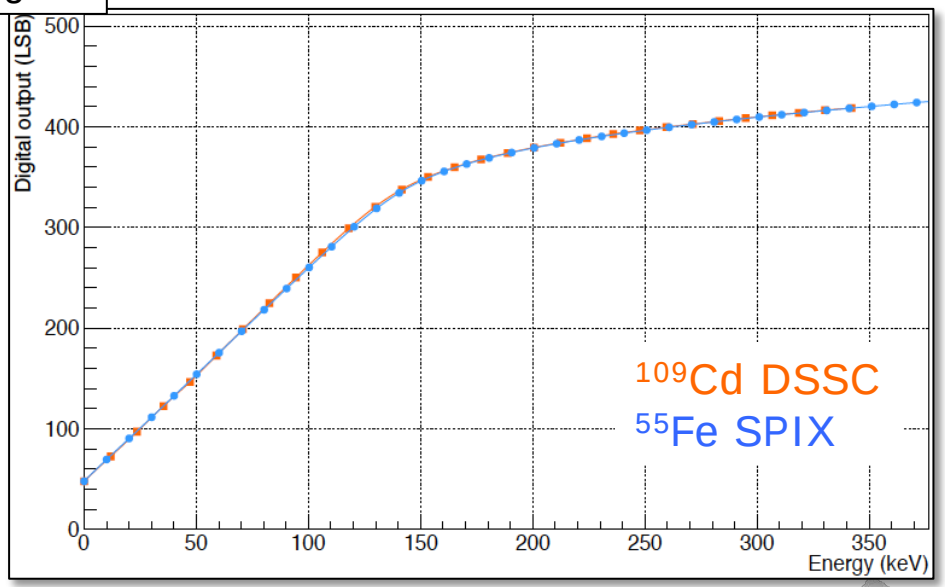
- Verification of DSSC prototype (8-bit read-out) NLSC: comparison to independent SPIX NLSC (14-bit read-out)
- Agreement within statistical and systematic uncertainties

pxd-7
short gate

1 keV/LSB



½ keV/LSB



Summary

SENSOR
- MiniSDD sensors are available and will be used for ladder camera and 1 Mpixel camera
- Pxd-8 DEPFETs will be used for the ladder camera.
- A new DEPFET production in industrial scale CMOS fab has started

ASIC
- F1 ASIC has been characterized in depth. Measurements with sensors was not yet possible
- Optimization of the design of the front-end for MiniSDD is ongoing for the F2 ASIC

CAMERA HEAD
- The flip-chip has started. 2 MiniSDD 64 x 64 sensors have been flipped to F1 ASICs
- Deflections of the sub module have been measured and macro assembly concept is in preparation
- The full electronics readout chain is complete and in operation

LADDER CAMERA
- FENICE installed, vacuum system working (best reached pressure ~ 5 x 10-7 mbar).
- Cooling system ready to be switched on
- First tests on PLC performed

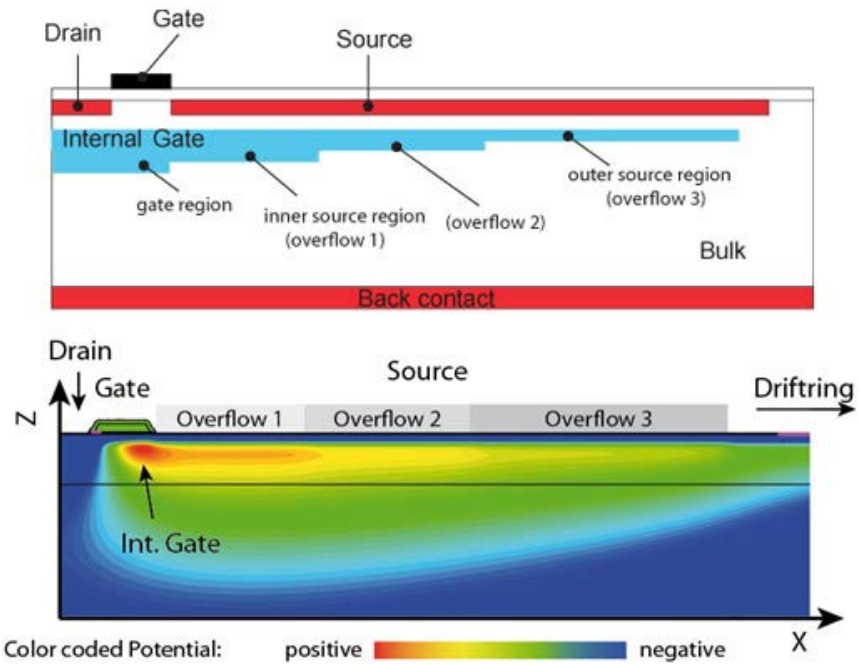
MECHANICS
- Double-walled coolant pipe architecture is fully qualified
- 1:1 Mock-up used for verifications

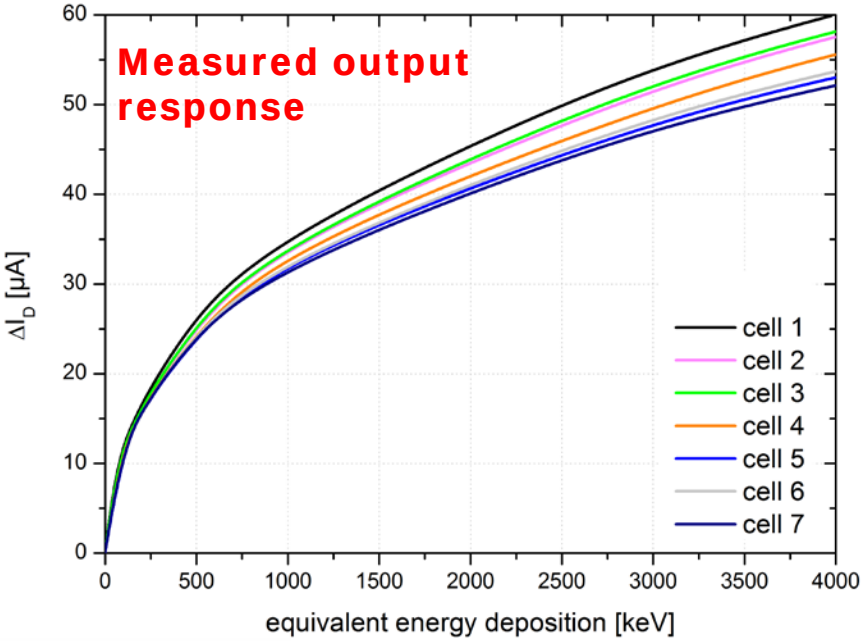
DAQ
- 3 PPTs have been produced and the C&C signal quality at 100 MHz has been verified
- 10 Hz operation with C&C signals runs stable
- The VETO and reordering mechanism has been successfully tested in hardware and simulation

CALIBRATION
- Calibration for 1 keV/LSB and ½ keV/LSB with 55Fe. Calibration with DSSC 8-bit resolution has been compared with calibration obtained with the 14 bit SPIX setup
- The path to scale the calibration procedure to 1 M pixels is under study.

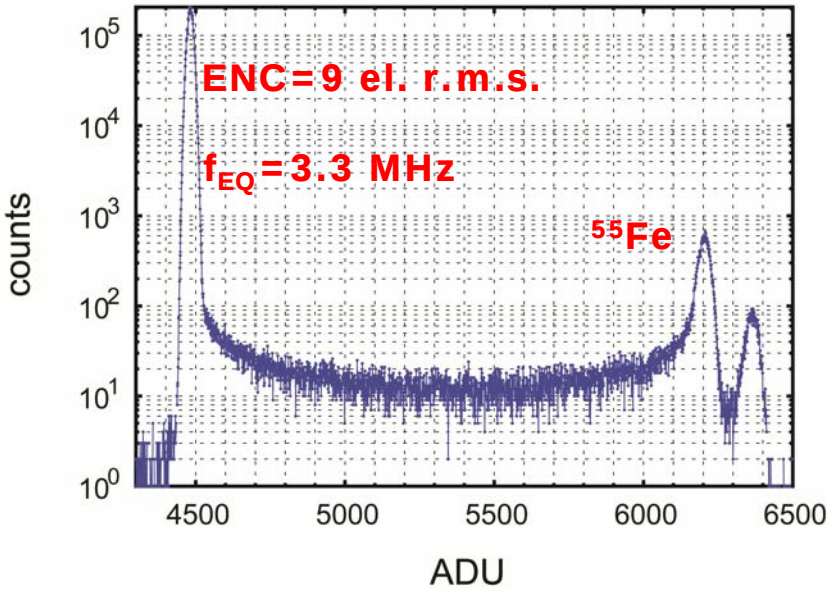
BACKUP

Non Linear DEPFET reminder





(Porro et al., "Development of the DEPFET Sensor With Signal Compression … ", IEEE TNS, Oct. 2012)

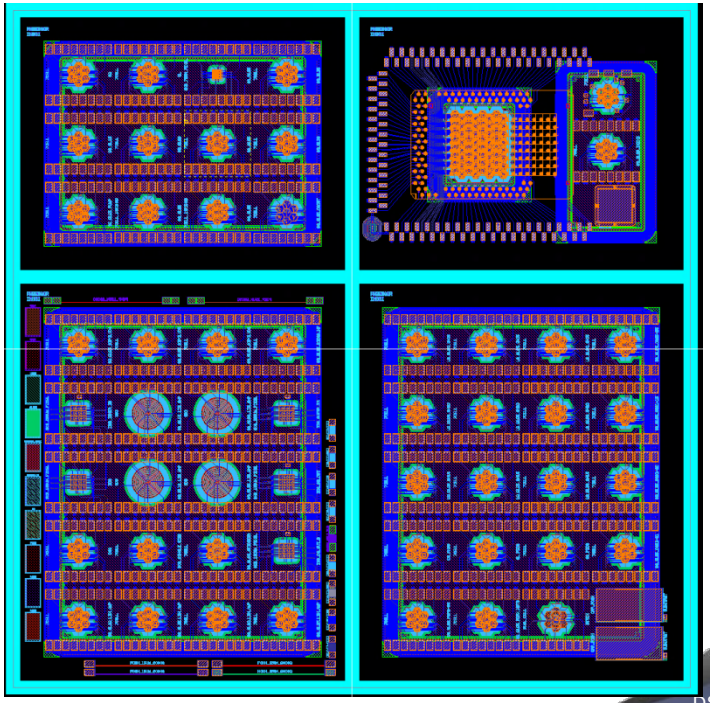


DEPFETs in Industrial-Scale CMOS Fab

- New 8 inch wafers show a very high quality
  - Depletion voltage is below 400 V
  - Leakage current is typ. < 1 nA /cm^2 at full depletion (150 diodes measured)
  - Not a single voltage breakdown occurred on reverse biased diodes
  - Distribution of leakage current is homogeneous across the wafer

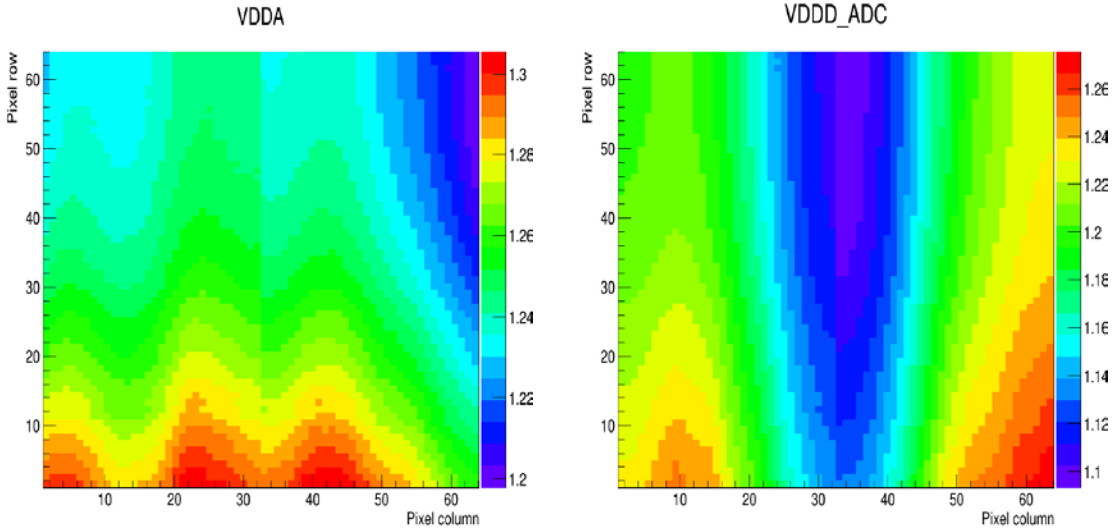
- Double sided processing of DEPFET devices with very sensitive entrance windows is possible in the CMOS Fab

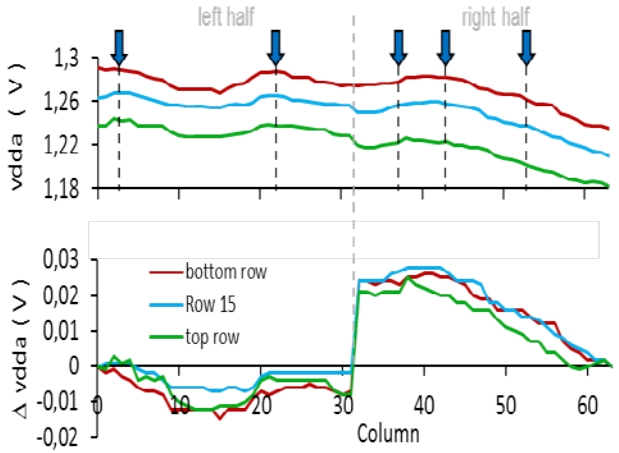
- First DEPFETs will be available in **April**
  - 7-cell clusters
  - Macropixels
  - 3x3 matrix (smaller pixels)
  - 8x8 matrix (UBM required)



ASIC - Measured Voltage Drops

- A nice monitoring feature allows for measuring of all voltages in each pixel:





- Measurements by HD (left) and DESY (right) are consistent
- Vertical drops are as expected
- A large horizontal component is a bad surprise. *Total* drops are 110 / 180mV
- Shape can be reproduced by careful (a posteriori) simulation of extracted power nets, taking into account bump positions
- Optimal bump position should reduce the hor. drop from 50mV to ~20mV. We therefore foresee to change the pad assignment in F2

Vacuum qualification infrastructure

Vacuum qualification of the ladder components and of the full ladder performed

REHA vacuum and heating system working, PLC under test

BigPipe upgraded and routinely used for vacuum qualification tests

RHEA: Residual gas analysis and thermal qualification chamber