# the built-in amplifier performance in HV-CMOS CHESS1

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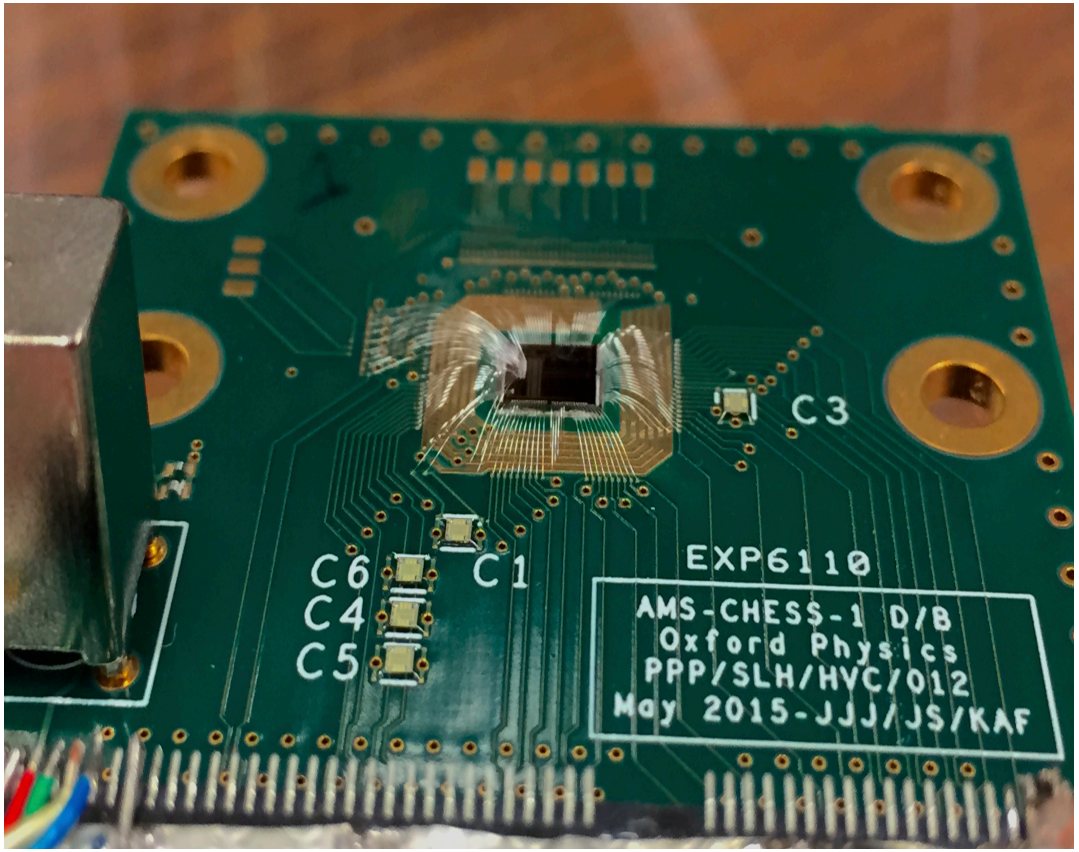
# CHESS1 bonded for testing

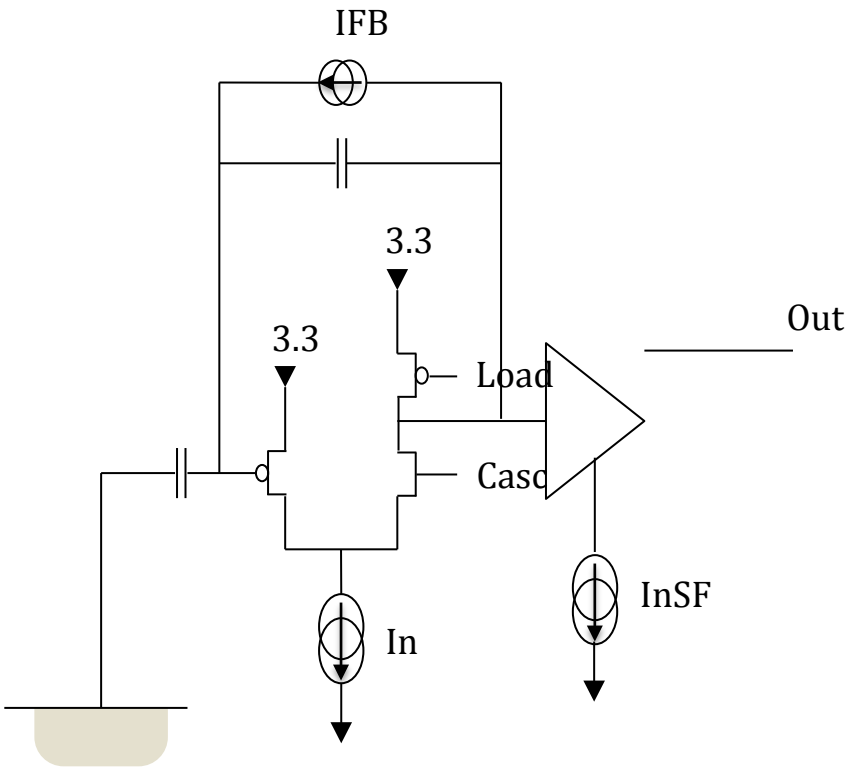
CHESS1 chip Mount on daughter board




Thanks to Jaya John and Oxford group to design daughter board for CHESS1 chip

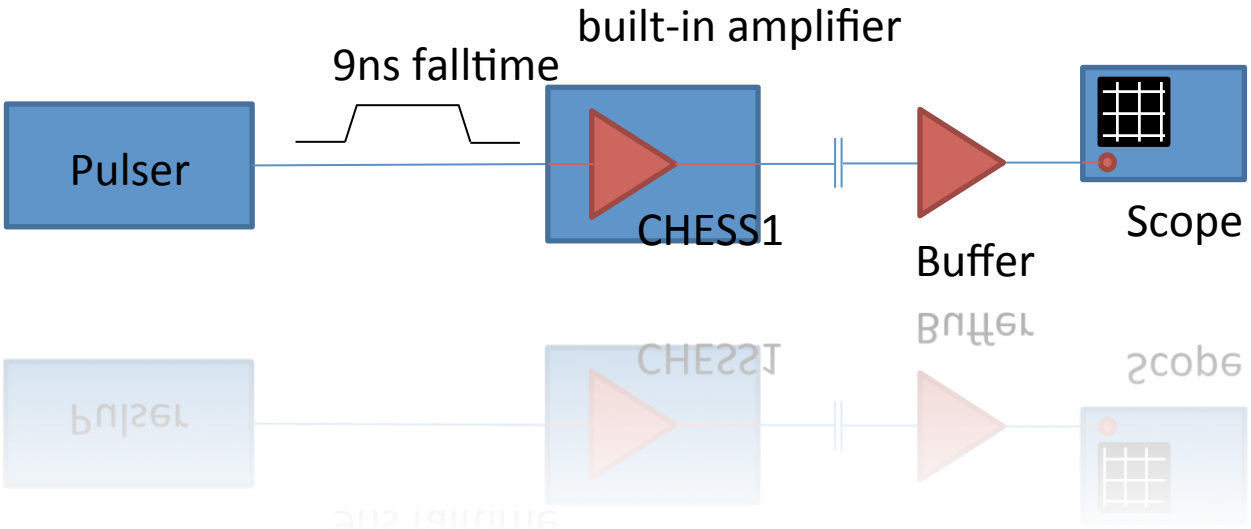
# CHESS1 amplifier

A low noise built-in amplifier **into** the CHESS1 chip to improve the signal to noise ratio.



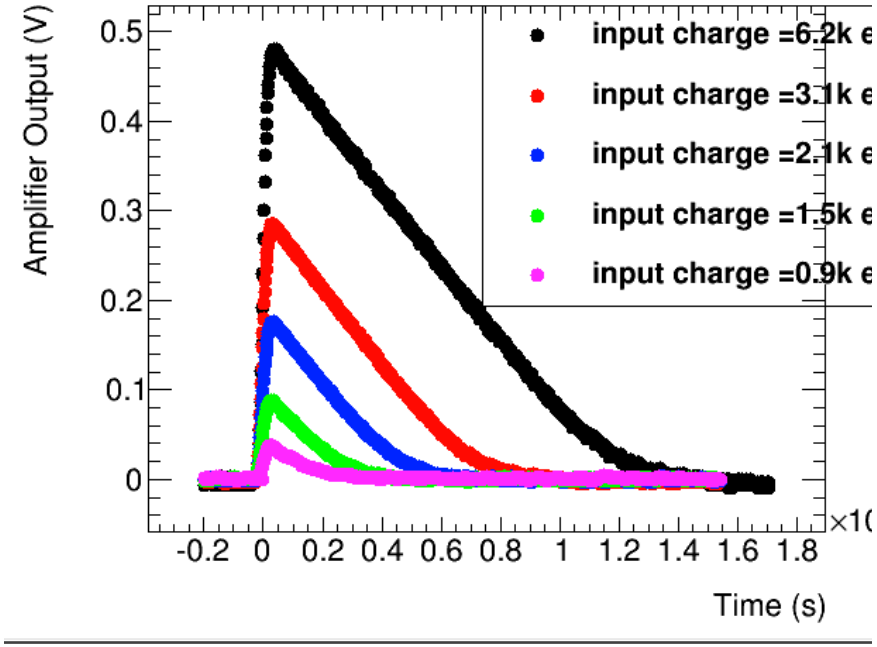

| Bias | Description | Config (V) |
|---|---|---|
| VNBias | Bias for the NWELL | 0.4 |
| Casc | Cascode voltage | 2.6 |
| VPLoad | Pmos Load voltage | 2.1 |
| iN | Amplifier bias current | 1.0 |
| iNSF | Source Follower Bias | 0.49 |
| iFB | Feedback current | 2.664 |

# Isolated amplifier  test Setup

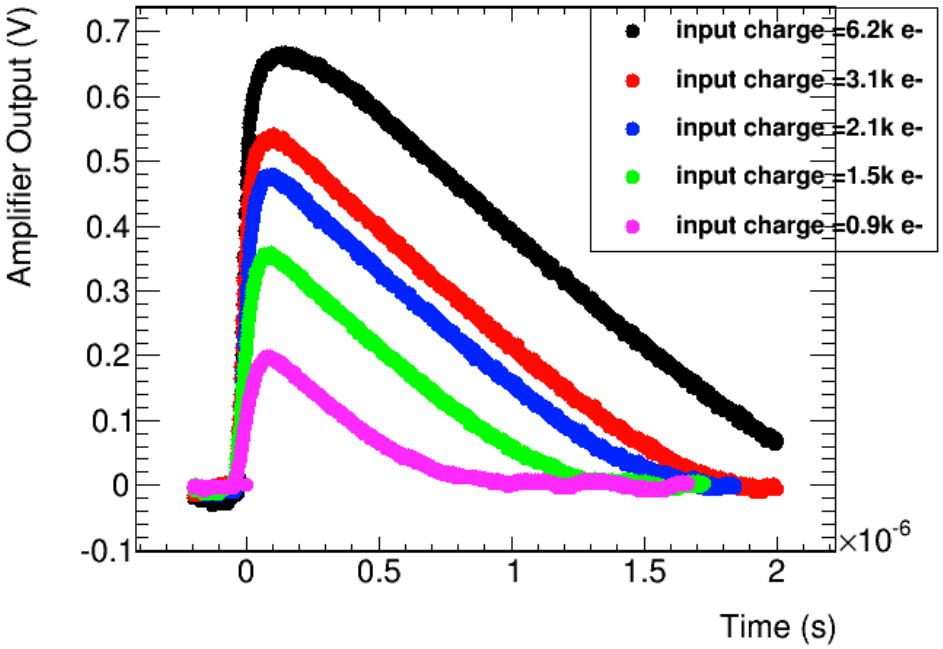


# Pulse shape

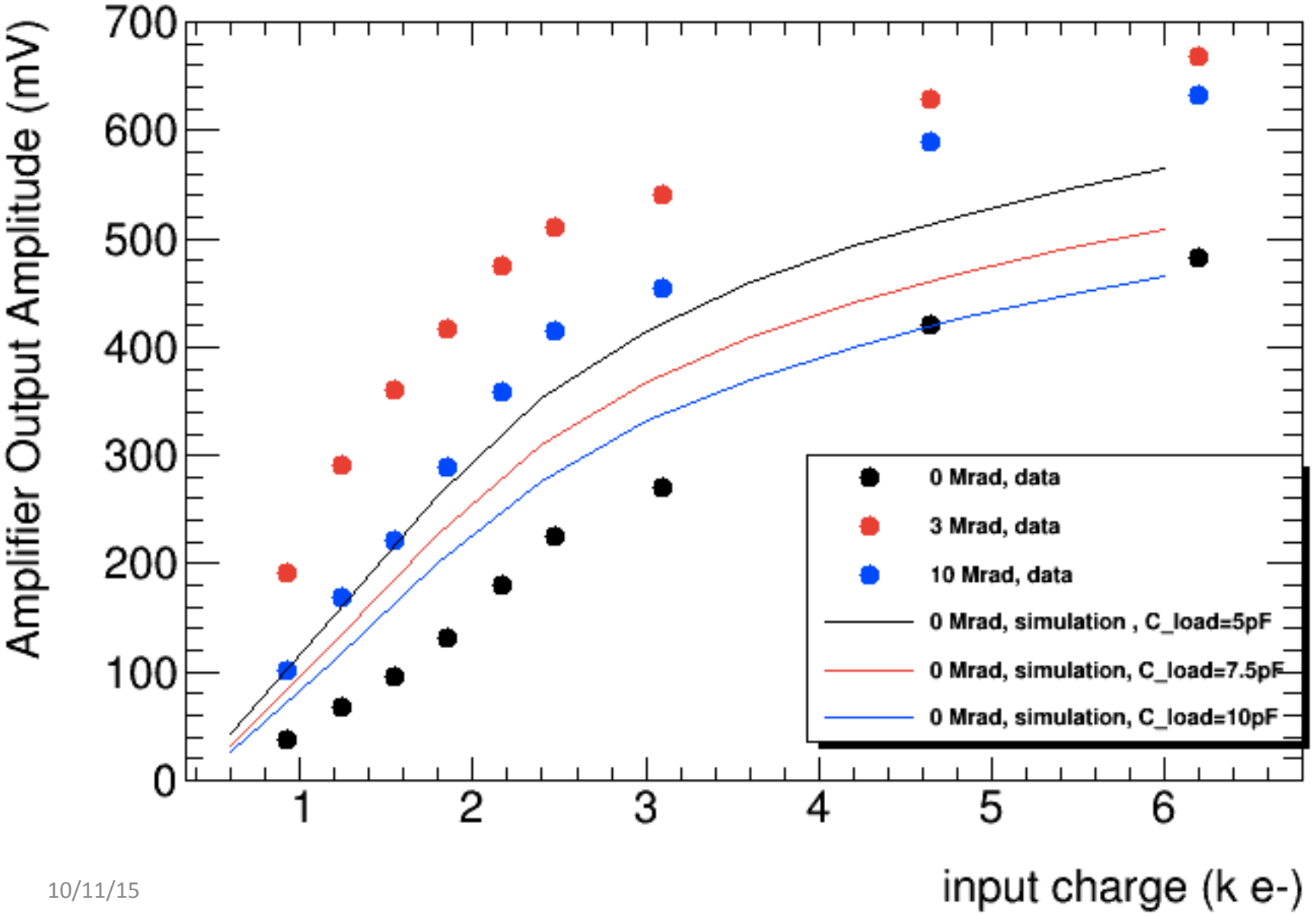
Before irradiation



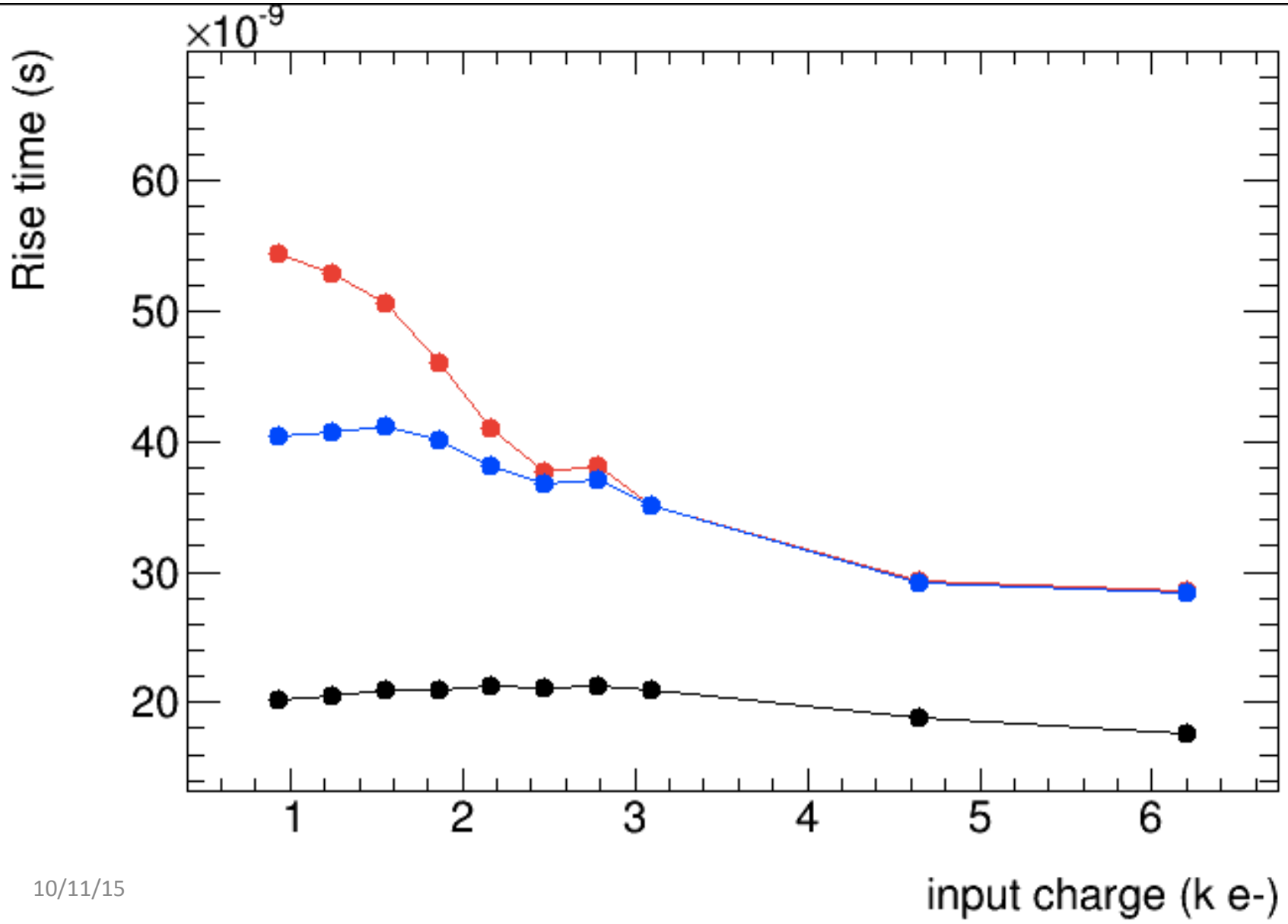

After 3Mrad gamma irradiation



# Response curve



# Rise time



# Summary

- The gain increased after radiation
- Rise time and deadtime(pulse width) increased after radiation