HR-CHESS2-TJ Update

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HR-CHESS2-TJ Chip Block Diagram Updated

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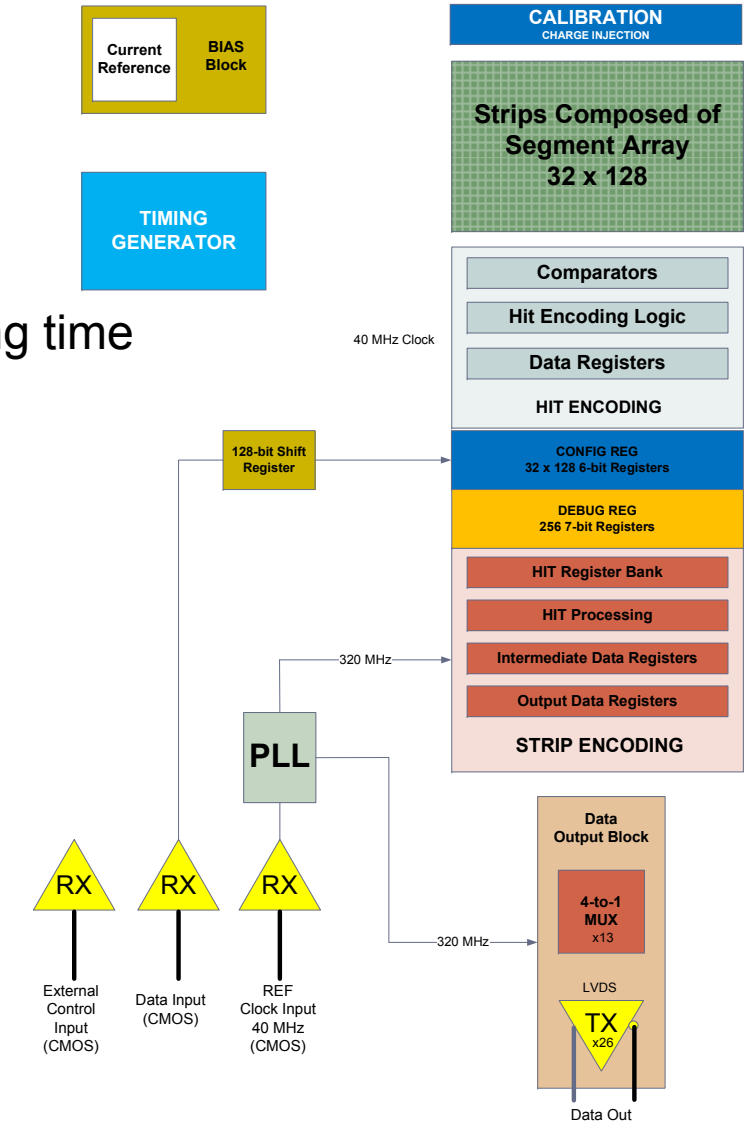
Main Functional Blocks:

- Fast Pre-Amplifier <10ns peaking time
- Comparator with threshold trim
- HIT Encoding
- Strip Encoding
- Data Output
- Calibration
- PLL
- LVDS TX/RX
- *Bias**
- *Timing generation**
- *CONFIG & DEBUG Register**
- *1 Strip dedicated for testing**

*Added & simulated recently



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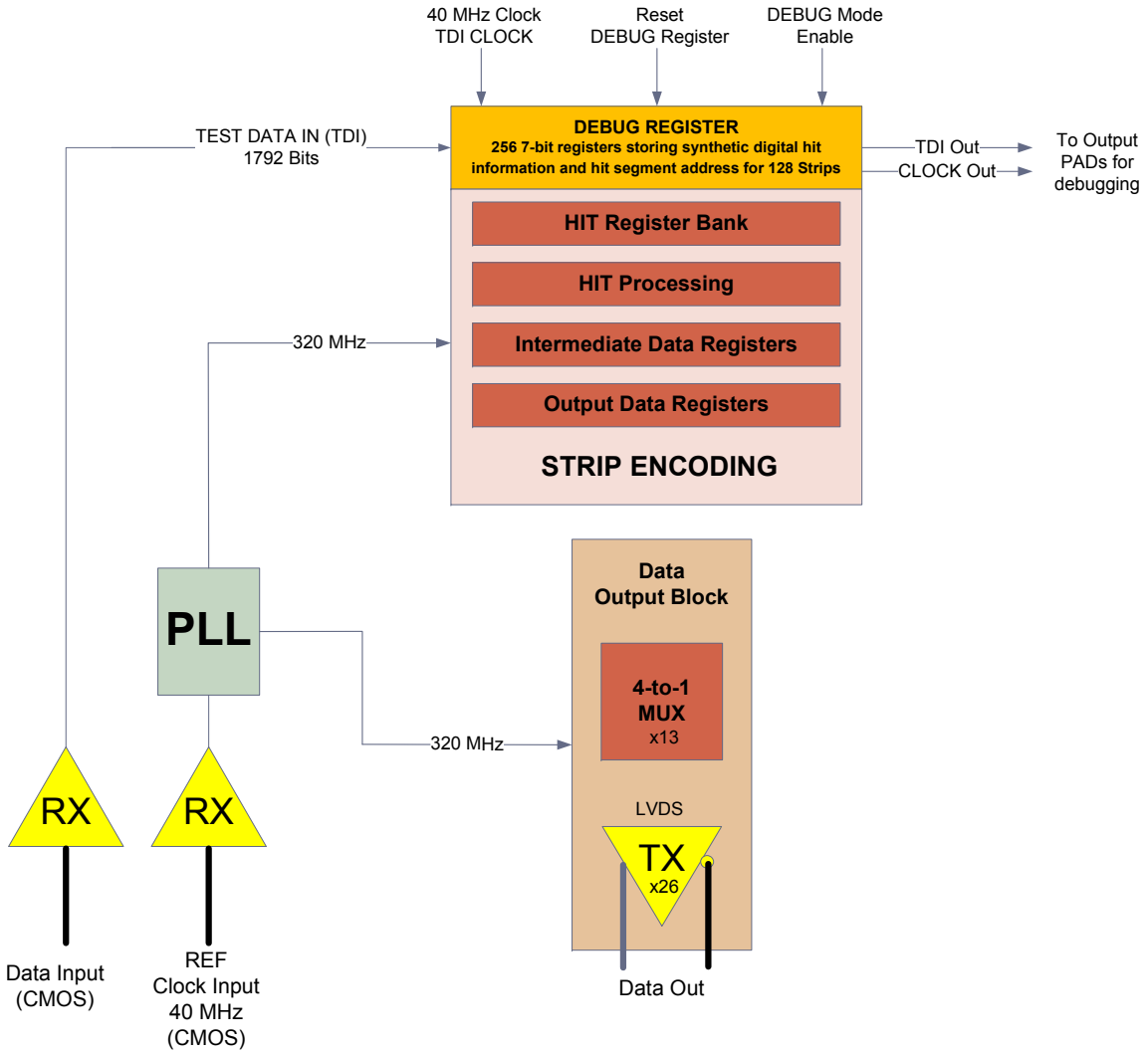
DEBUG register to test digital back-end



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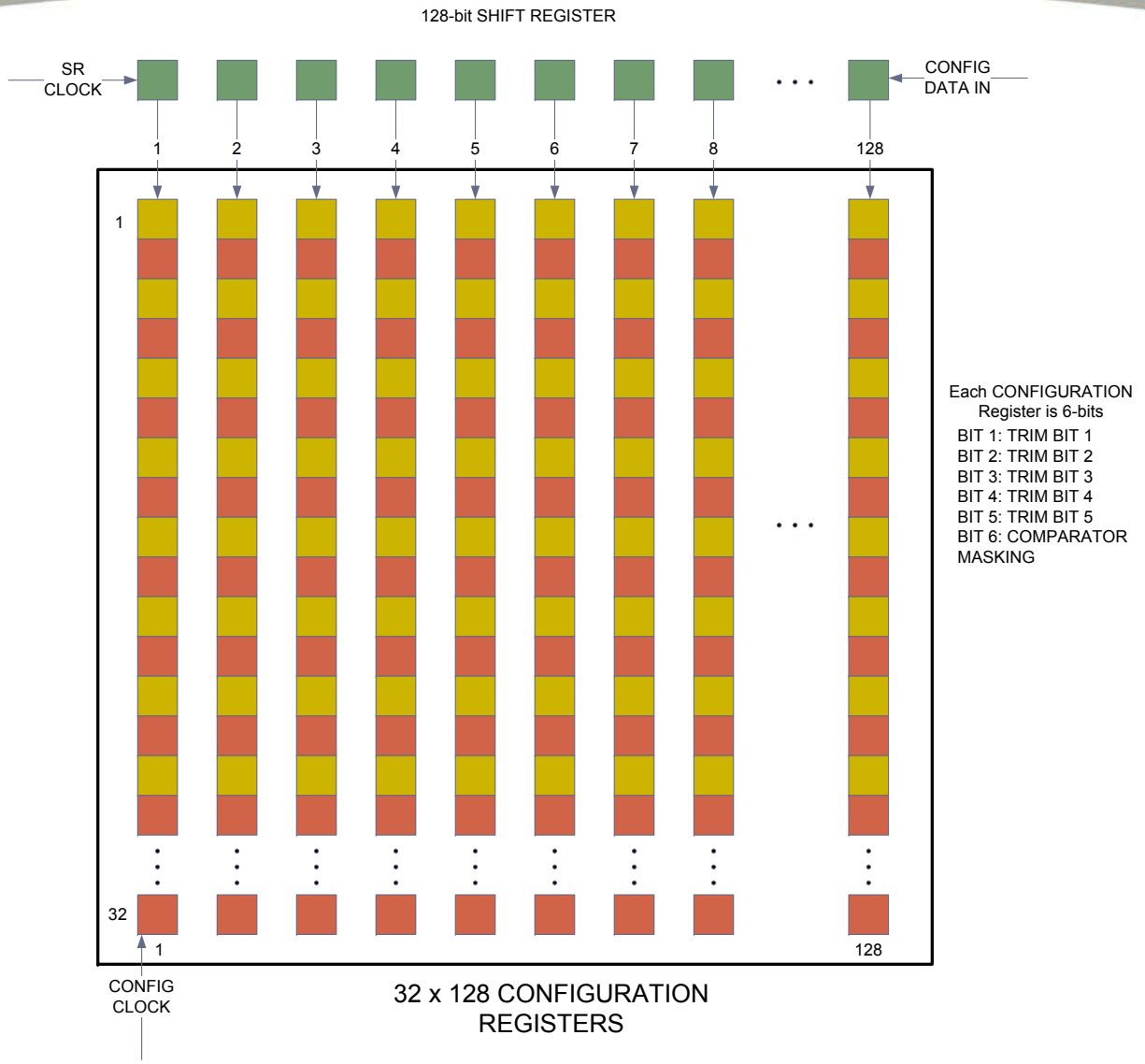
CONFIG register for calibration and masking



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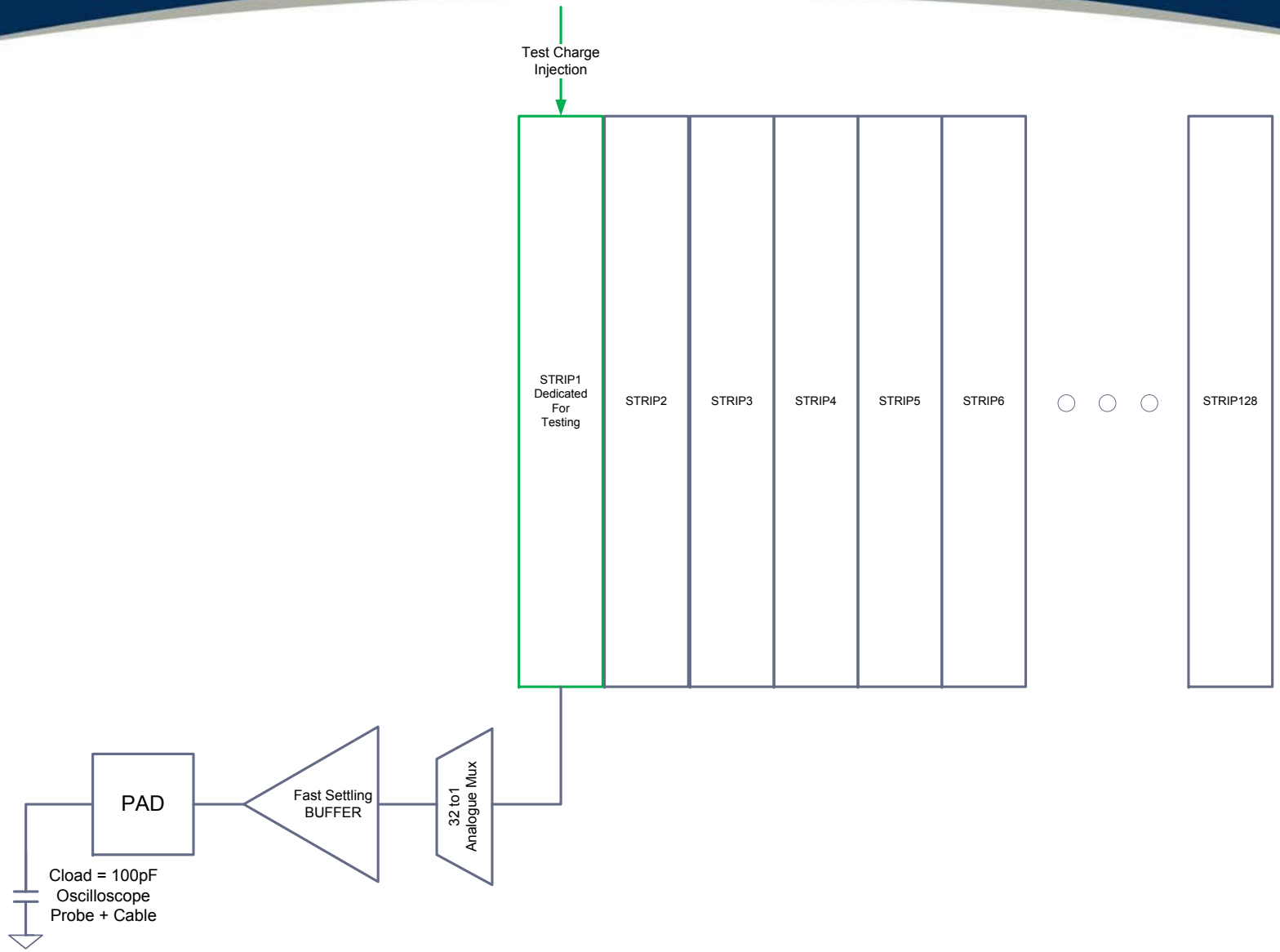
Test/debug channel From STRIP1



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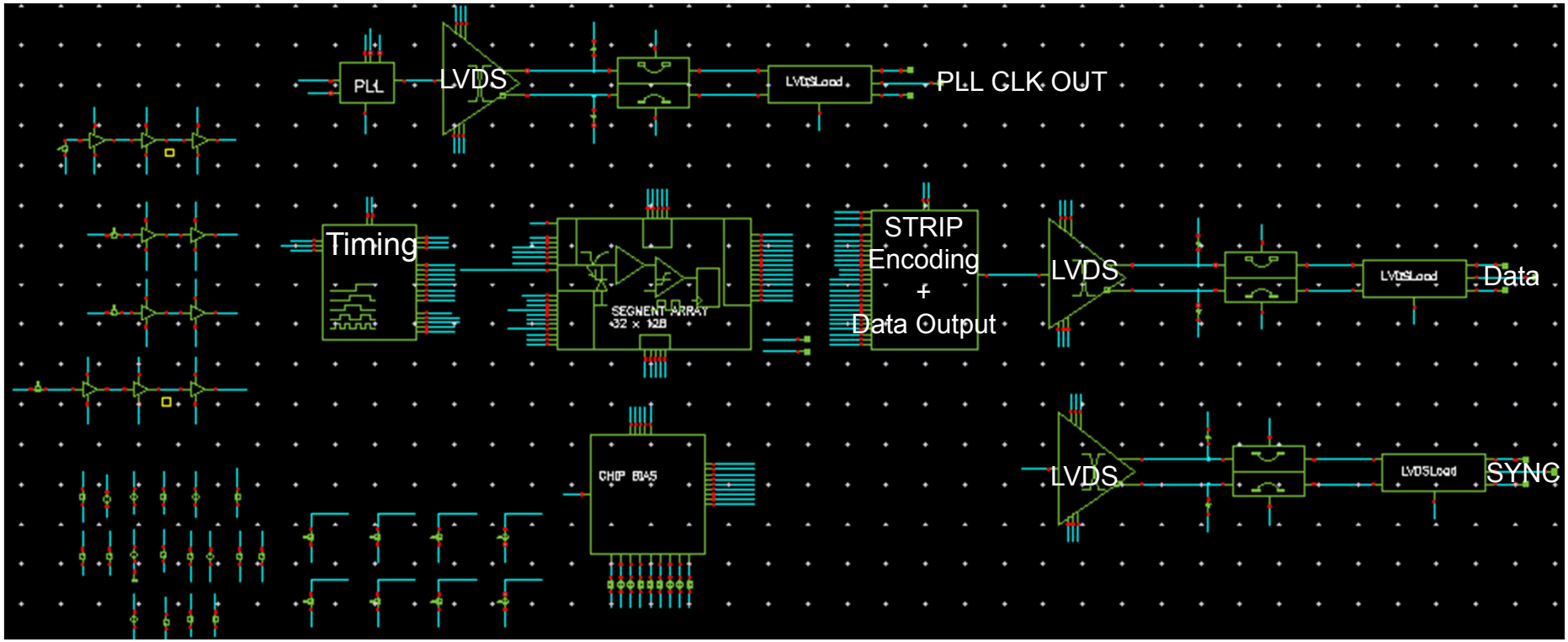
Top-level Simulation
Test bench

Full-chip simulation; added PLL, timing generation block, BIAS block, and LVDS stages to the existing top-level simulation



NOT simulated in this top-level test bench:

- Configuration and Debug registers
- Test debug column circuitry

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Top-level simulation setup

- We simulate 7 Strips being hit in 2 adjacent bunch crossings
- 3 hits in BX1 and 4 hits in BX2
- For each strip that was hit the last Segment/Pixel was hit
- 7-bit Strip address is binary coded
- Goal is to detect and read out these hits for each BX and output their address inside 2 BX periods or 50 ns
- Clock period used in simulation is 320 MHz
- The Hit addresses corresponding to each bunch crossing are then stored and readout through LVDS stages every 25 ns.
- Table below shows the Hit locations and corresponding 7-bit Strip address (binary coded).

Valid Addresses
Segment: 0 to 31
Strip: 1 to 127

Hits	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0	Strips	BX
1	0	0	0	0	1	0	0	4	1
2	0	0	0	1	0	0	1	9	1
3	0	1	0	0	0	1	0	34	1
4	0	1	1	0	1	1	1	55	2
5	1	0	0	0	1	1	0	70	2
6	1	0	1	1	1	1	0	94	2
7	1	1	1	1	1	1	1	127	2

Data 4	Data 3	Data 2	Data 1	Data 0	Segment
1	1	1	1	1	31

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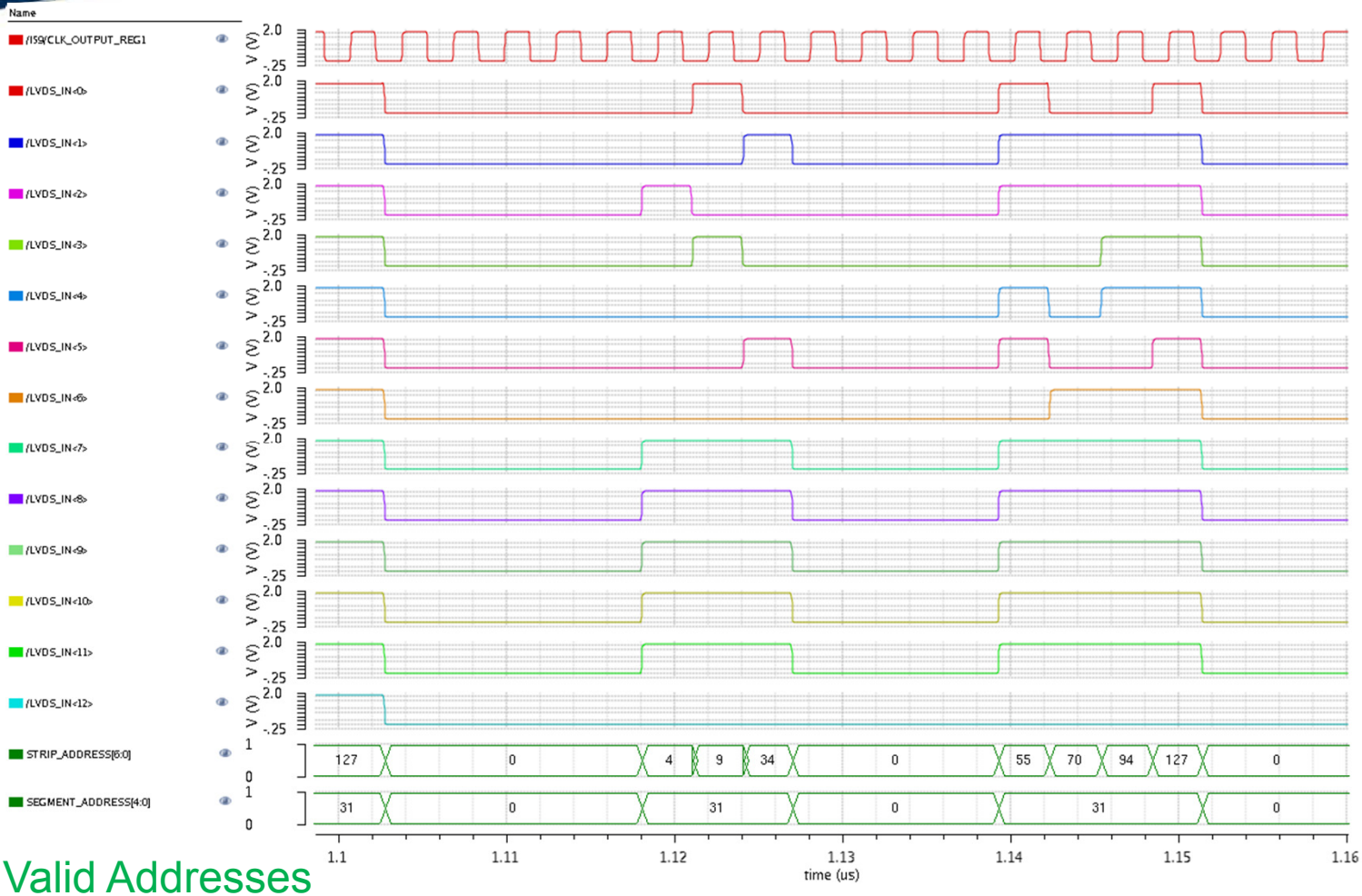
Top-Level simulation data in CMOS logic level



Temp=27C
Nominal corner
Clock=320MHz

Hits	Strips	BX
1	4	1
2	9	1
3	34	1
4	55	2
5	70	2
6	94	2
7	127	2

Valid Addresses
Segment: 0 to 31
Strip: 1 to 127

Data 4	Data 3	Data 2	Data 1	Data 0	Segment
1	1	1	1	1	**31**

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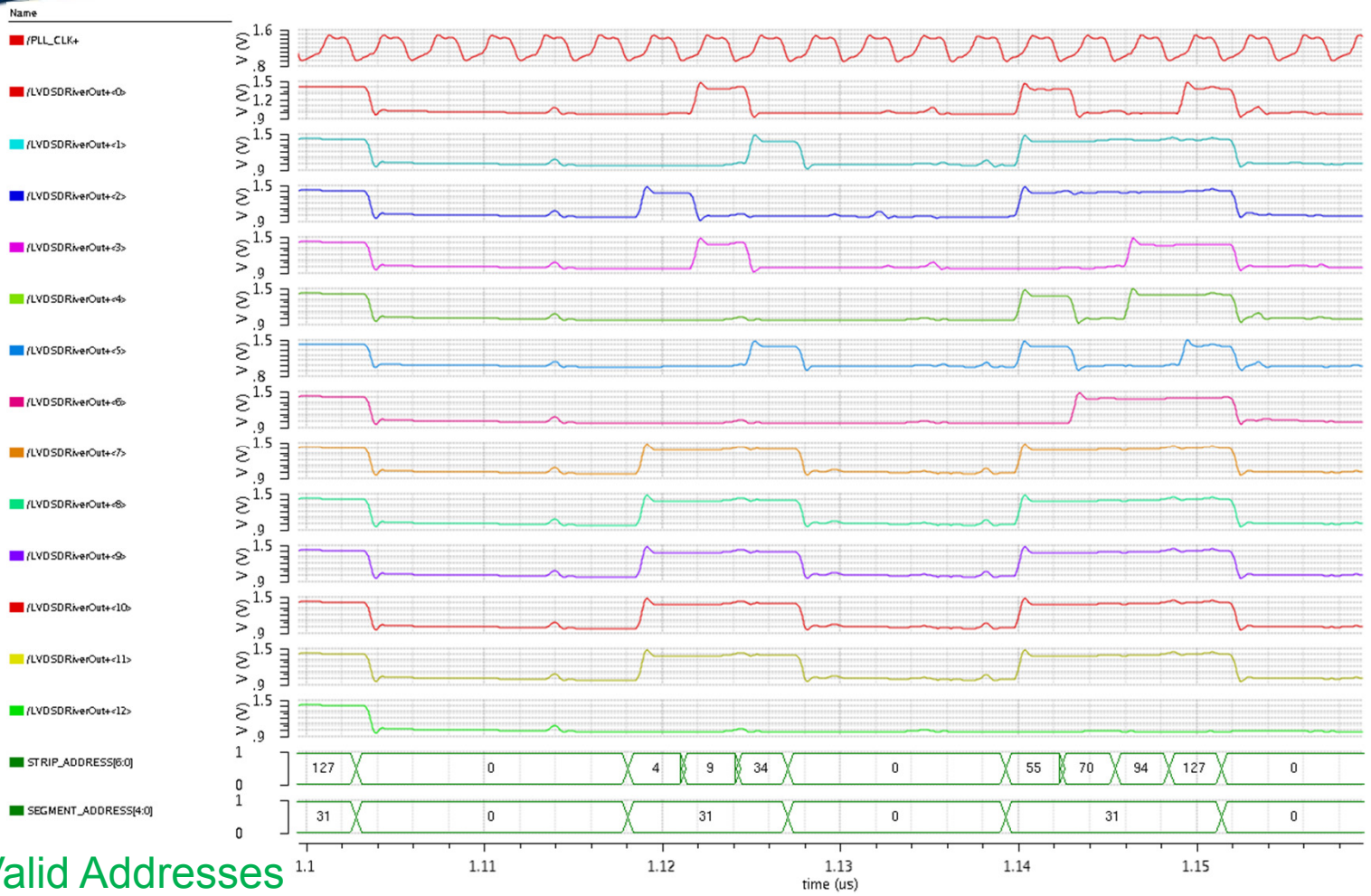
Top-Level simulation
Data at the output of LVDS drivers



LVDS drivers have load equivalent of 75 cm cable

Hits	Strips	BX
1	4	1
2	9	1
3	34	1
4	55	2
5	70	2
6	94	2
7	127	2

Valid Addresses
Segment: 0 to 31
Strip: 1 to 127

Data 4	Data 3	Data 2	Data 1	Data 0	Segment
1	1	1	1	1	**31**

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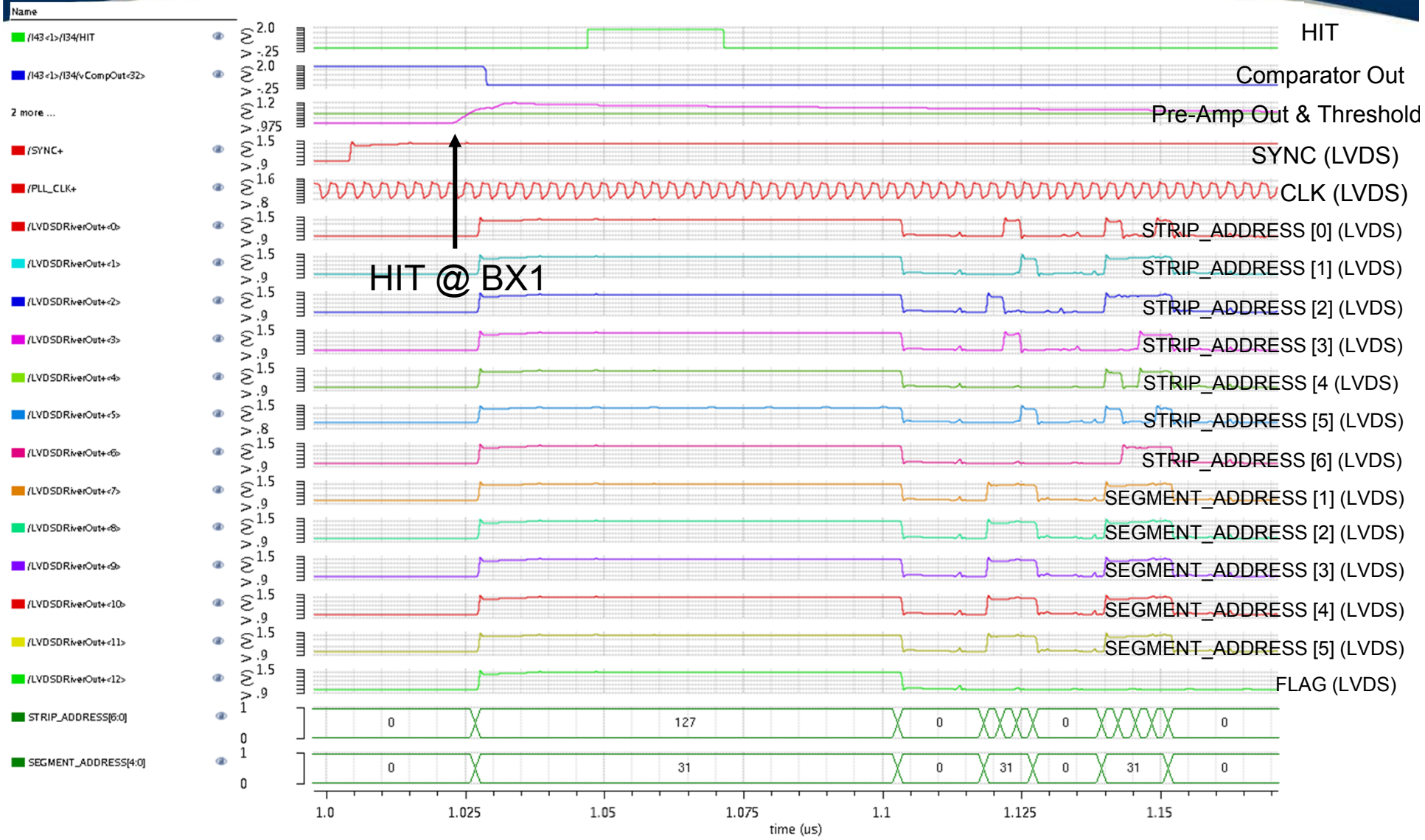
Top-Level simulation
Detail view



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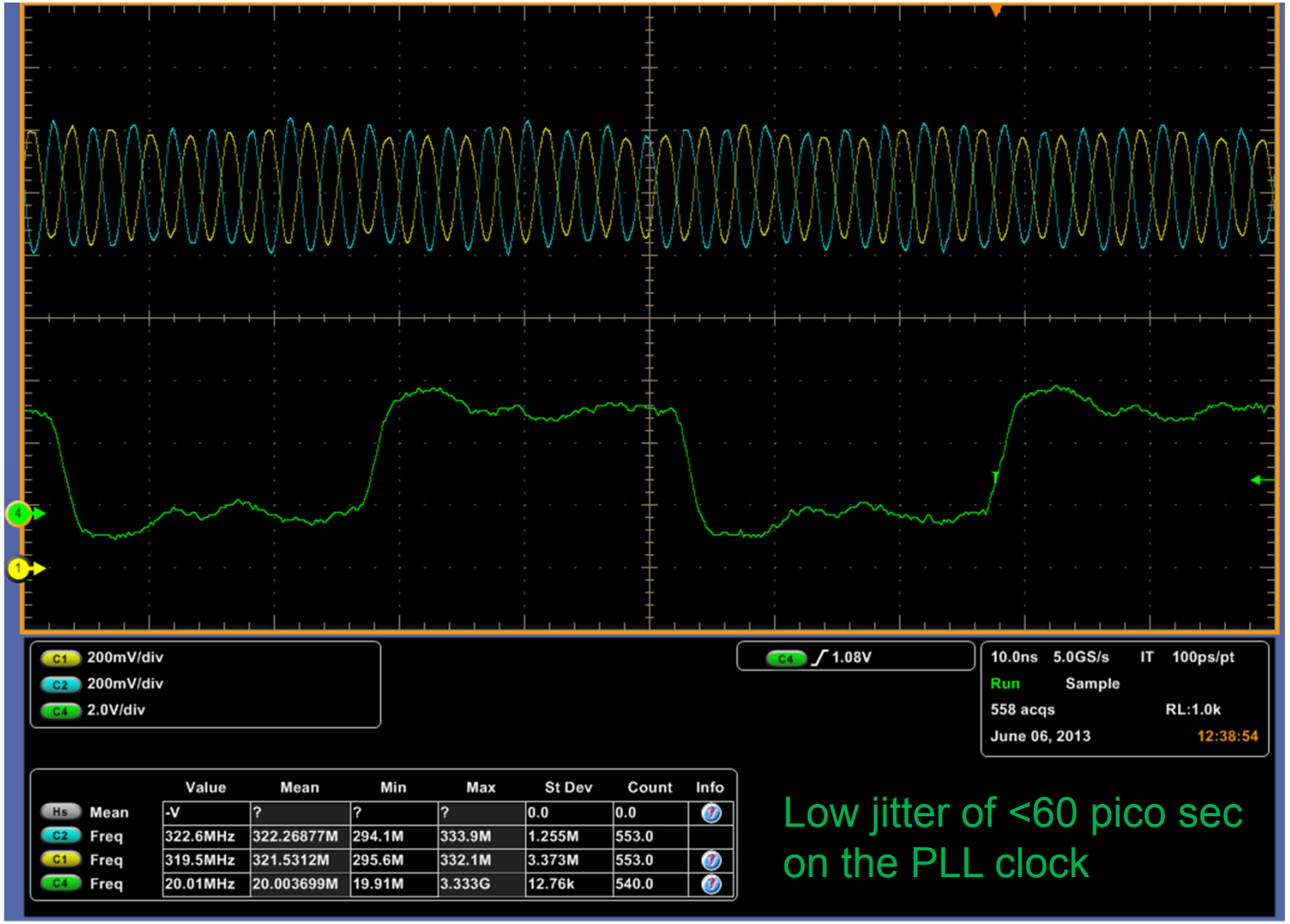
PLL 320MHz CLOCK
Measured Results from PLL+LVDS Driver



PLL 320MHz Clock from LVDS Output

REF: 20MHz Clock seen at CMOS Output