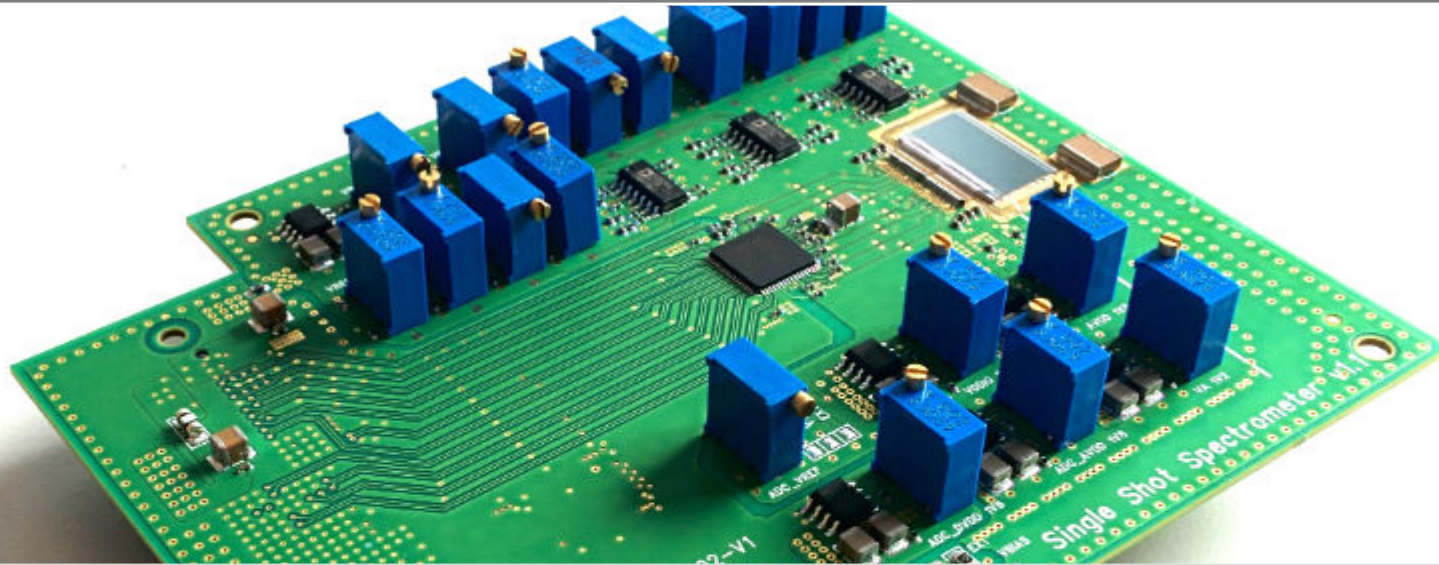


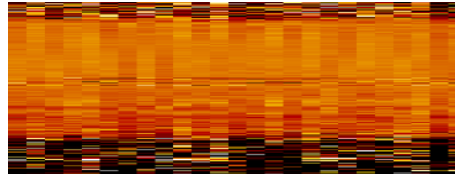
KALYPSO: Karlsruhe Linear array detector for MHz-repetition rate Spectroscopy

L. Rota (lorenzo.rota@kit.edu), M. Caselle, A. Mozzanica, N. Hiller, P. Schönfeldt, S. Walther,
G. Niehues, M. J. Nasse, M. Balzer, M. Weber

KIT, Institute for Data Processing and Electronics (IPE)

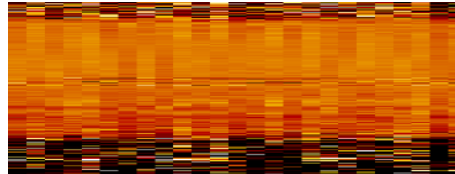


KALYPSO Motivation

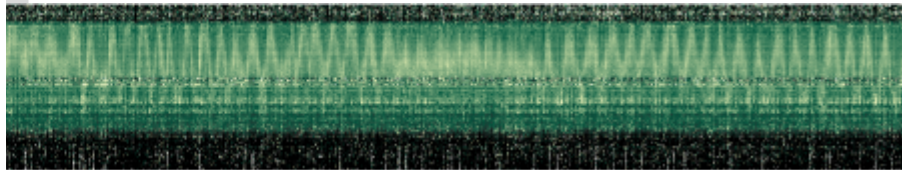
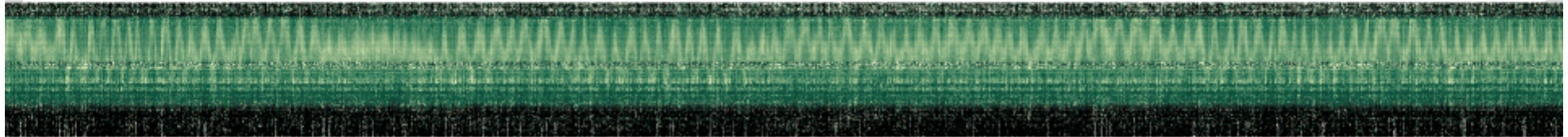
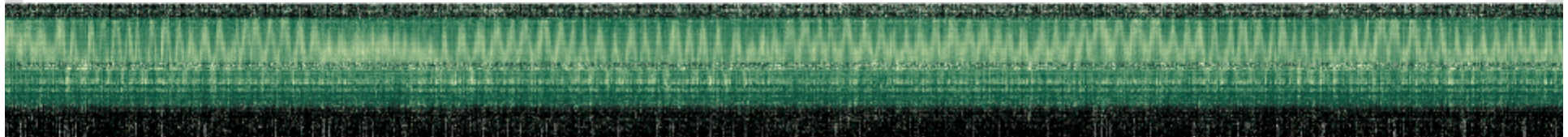
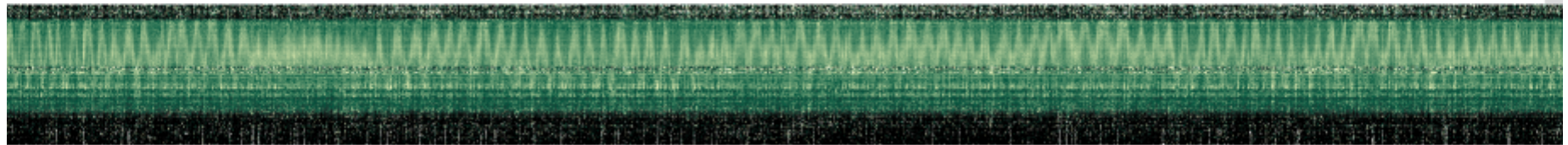


Commercial solutions

KALYPSO Motivation



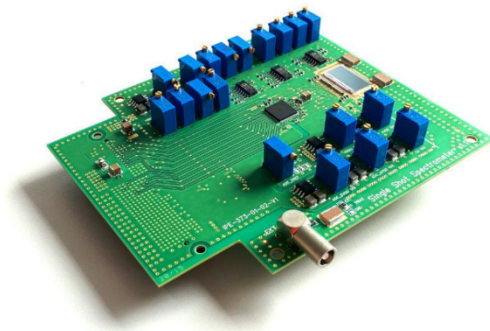
Commercial solutions



KALYPSO

... limited only by PC memory

KALYPSO v2.0 vs KALYPSO v1.1



2x GOTTHARD v1.4:

- Charge-sensitive amplifier
- 3 different Gain settings
- Inputs: 128
- Outputs: 4 outputs
- Max line-rate= 900 kHz
- Designed by A. Mozzanica (PSI)

InGaAs sensor (Xenics):

- 256 pixels, 50 μ m pitch

Si sensor (PSI):

- 256 pixels (diced), 50 μ m pitch

AD9252:

- Channels: 8
- Resolution: 14 bits
- Sampling rate: 50 MSps

KALYPSO detector board

Xilinx ML605:

- FPGA: Virtex6, speedgrade -1
- Connectors: 1 FMC fully populated, 1 partially
- PCI-Express link: x4 Gen2 or x8 Gen1
- KIT-DMA engine for Xilinx PCI-Express Core 2.0 (up to 12/24 Gbit/s)

PCI-Express
x4 Gen2
(3.6 Gbit/s)

RF Clock (62.5 MHz)
Fast trigger (900 kHz)
Slow trigger (0.1 Hz)

KALYPSO DAQ system at KIT

1 MHz

2x GOTTHARD 'KIT-version':

- 3 different Gain settings
- Inputs: 128
- Outputs: 8 outputs
- Max line-rate: 2.7 MHz
- Designed by A. Mozzanica (PSI)

AD9249:

- Channels: 16
- Resolution: 14 bits
- Sampling rate: 65 MSps

LMK03001C:

- Outputs: 3 LVDS, 5 LVPECL
- VCO RMS Jitter: 400 fs
- VCO Tuning Range: 1470 - 1570 MHz

KALYPSO detector board

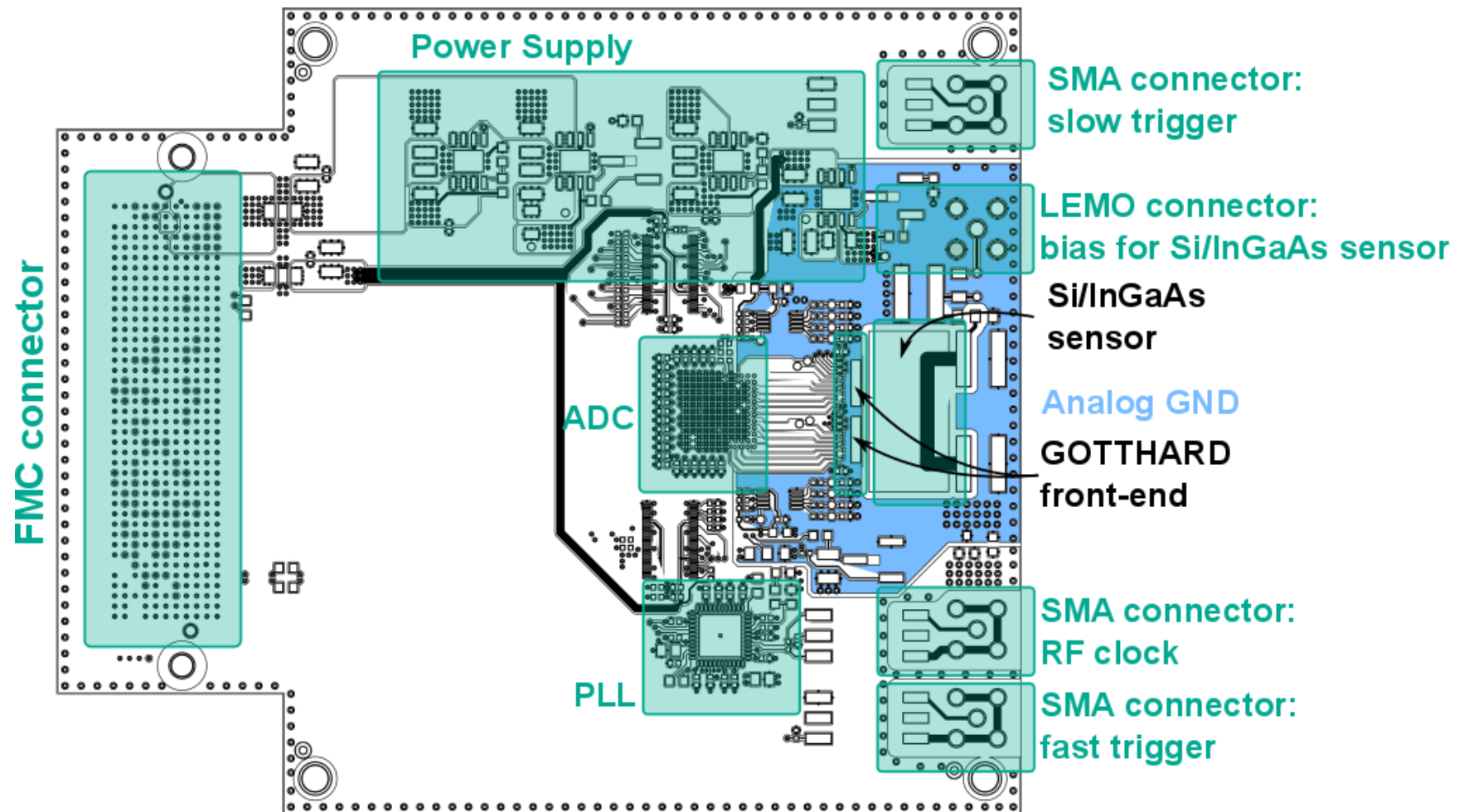
PCI-Express
x8 Gen3
(10 Gbit/s)

RF Clock (62.5 MHz)
Fast trigger (2.7 MHz)
Slow trigger (0.1 Hz)

KALYPSO DAQ system at KIT

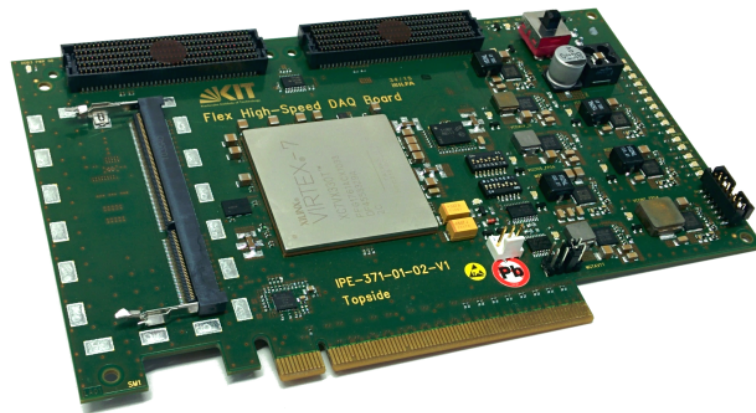
2.7 MHz

KALYPSO v2.0: preview of PCB layout



High-performance readout electronics

Hi-Flex: custom FPGA board

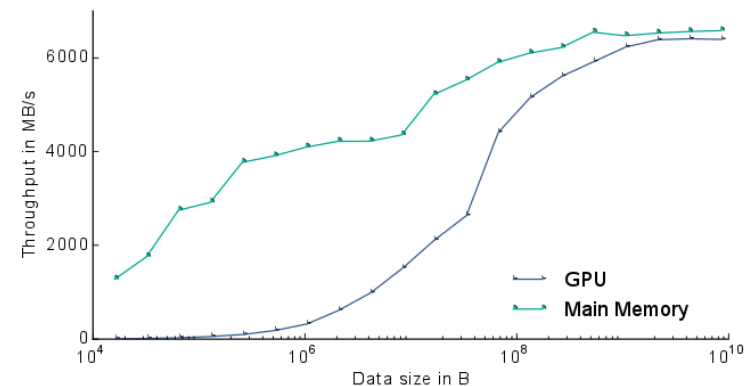


- Virtex 7, Speedgrade -2
- PCI-Express Gen3 x16 Lanes (net data throughput of up to 13 GB/s)
- 2 FMC Connectors, fully populated
- 119 Gbit/s DDR Memory

... currently under test at IPE!

High-throughput readout architecture based on PCI-Express 3.0 and AMD's DirectGMA

The architecture consists of a Direct Memory Access (DMA) engine compatible with the Xilinx PCI-Express 3.0 core, a Linux driver for register access, and high-level software to manage direct memory transfers using AMD's DirectGMA technology.



- Throughput: 6.4 GB/s to GPU memory and 6.6 GB/s to system memory
- Real-time data analysis on GPU based on OpenCL code
- Integration with custom framework for high-performance GPU computing