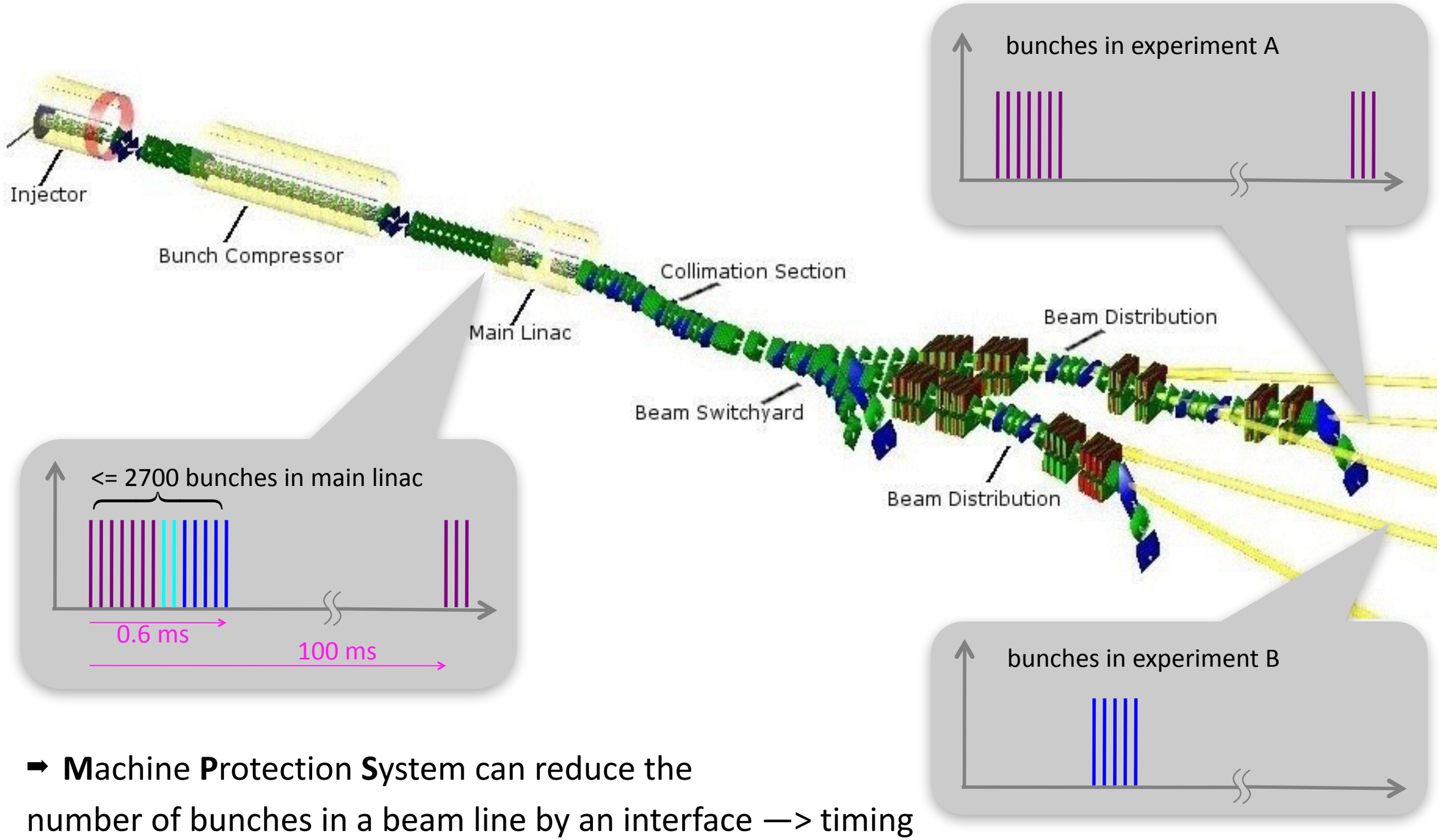
The XFEL Timing System

Kay Rehlich, DESY MCS4

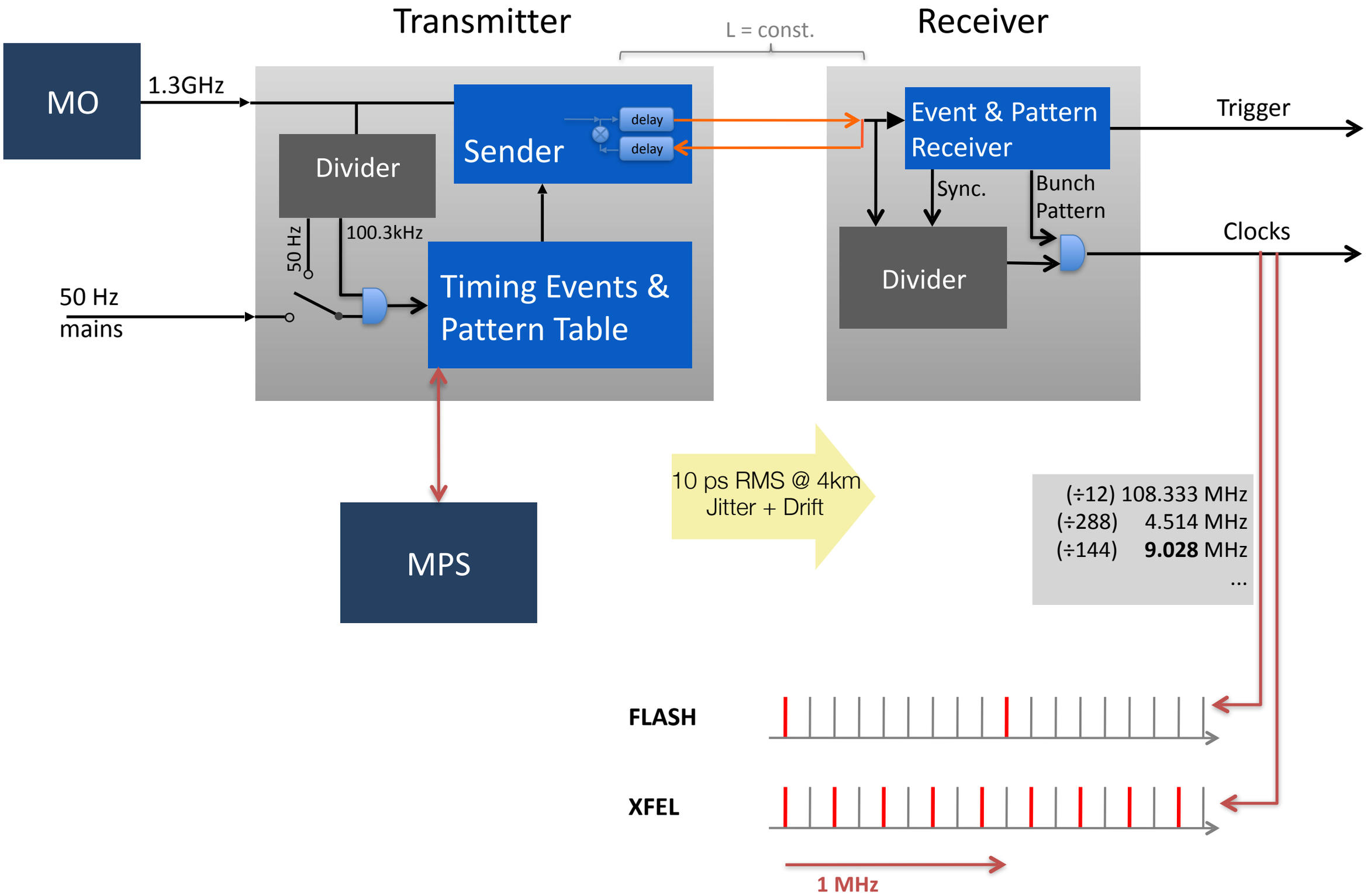
Introduction

- The XFEL can produce 27 000 bunches per second

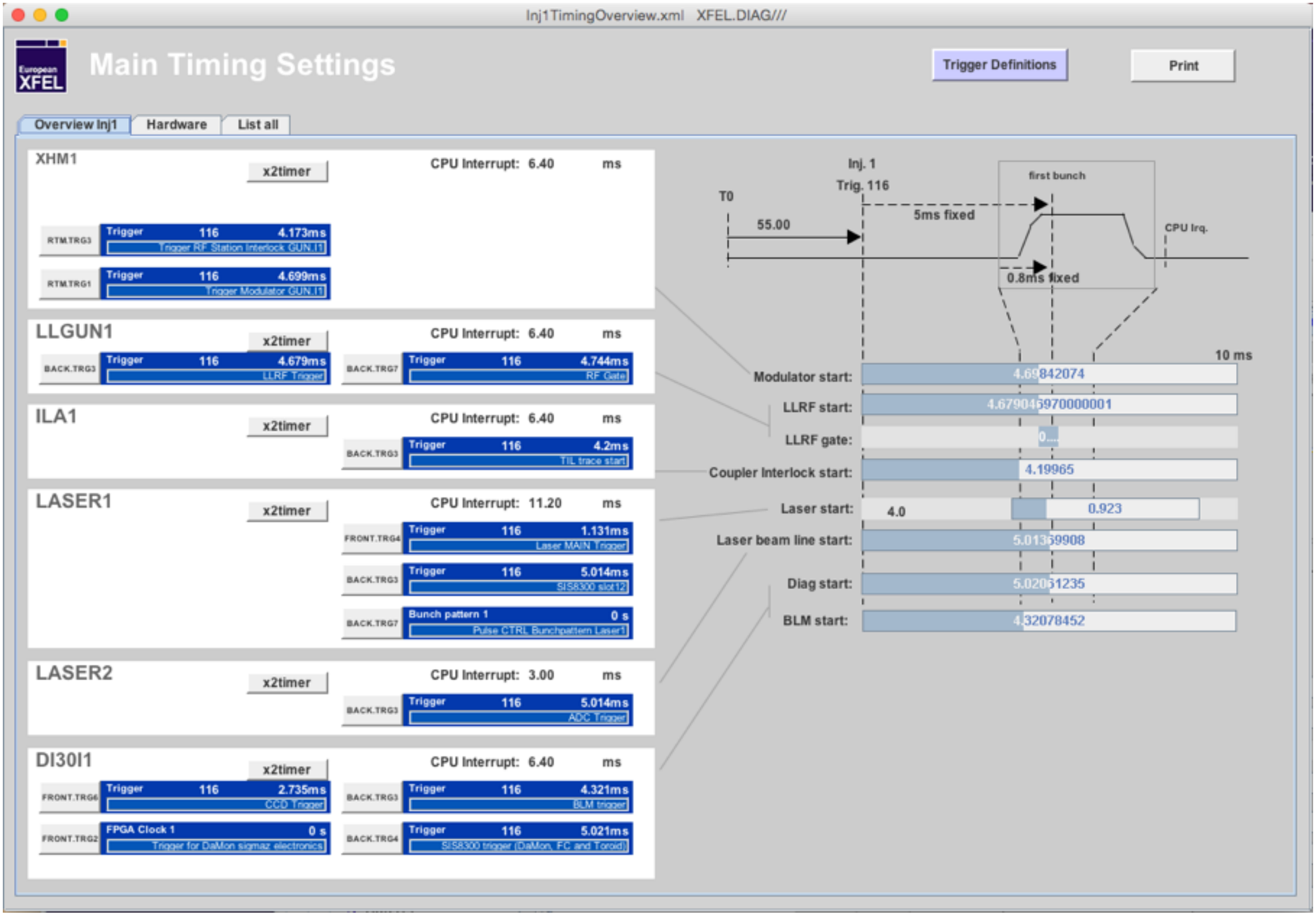


➡ **M**achine **P**rotection **S**ystem can reduce the number of bunches in a beam line by an interface —> timing

The Basics


Transmitter
L = const.
Receiver
MO
1.3GHz
Divider
Sender
delay
delay
50 Hz
100.3kHz
50 Hz
mains
Timing Events &
Pattern Table
Event & Pattern
Receiver
Trigger
Sync.
Bunch
Pattern
Clocks
Divider
MPS
10 ps RMS @ 4km
Jitter + Drift
(÷12) 108.333 MHz
(÷288) 4.514 MHz
(÷144) 9.028 MHz
...
FLASH
XFEL
1 MHz

Triggers

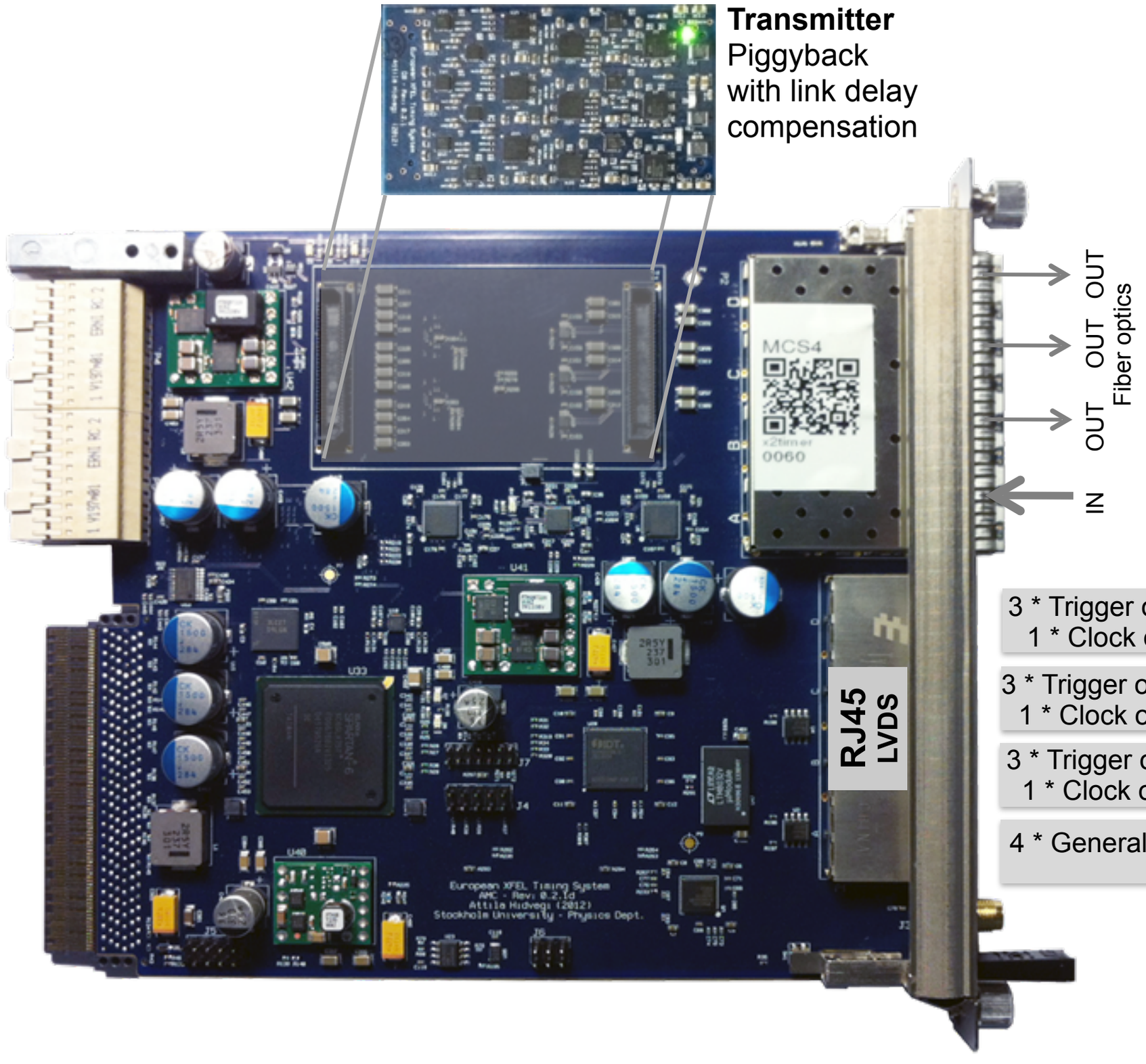

Inj1TimingOverview.xml XFEL.DIAG///
Main Timing Settings
Trigger Definitions
Print
Overview Inj1
Hardware
List all
XHM1
x2timer
CPU Interrupt: 6.40 ms
RTM.TRG3 Trigger 116 4.173ms Trigger RF Station Interlock GUN.I1
RTM.TRG1 Trigger 116 4.699ms Trigger Modulator GUN.I1
LLGUN1
x2timer
CPU Interrupt: 6.40 ms
BACK.TRG3 Trigger 116 4.679ms LLRF Trigger
BACK.TRG7 Trigger 116 4.744ms RF Gate
ILA1
x2timer
CPU Interrupt: 6.40 ms
BACK.TRG3 Trigger 116 4.2ms TIL trace start
LASER1
x2timer
CPU Interrupt: 11.20 ms
FRONT.TRG4 Trigger 116 1.131ms Laser MAIN Trigger
BACK.TRG3 Trigger 116 5.014ms SIS8300 slot12
BACK.TRG7 Bunch pattern 1 0 s Pulse CTRL Bunchpattern Laser1
LASER2
x2timer
CPU Interrupt: 3.00 ms
BACK.TRG3 Trigger 116 5.014ms ADC Trigger
DI30I1
x2timer
CPU Interrupt: 6.40 ms
FRONT.TRG6 Trigger 116 2.735ms CCD Trigger
FRONT.TRG2 FPGA Clock 1 0 s Trigger for DaMon sigmaz electronics
BACK.TRG3 Trigger 116 4.321ms BLM trigger
BACK.TRG4 Trigger 116 5.021ms SIS8300 trigger (DaMon, FC and Toroid)
Inj. 1
Trig. 116
T0
55.00
5ms fixed
first bunch
CPU Irq.
0.8ms fixed
10 ms
Modulator start: 4.69842074
LLRF start: 4.6790469700000001
LLRF gate: 0...
Coupler Interlock start: 4.19965
Laser start: 4.0 0.923
Laser beam line start: 5.01359908
Diag start: 5.02031235
BLM start: 4.32078452

MicroTCA.4 Timing Receiver / Transmitter

Can be used as a timing **receiver** or **transmitter**

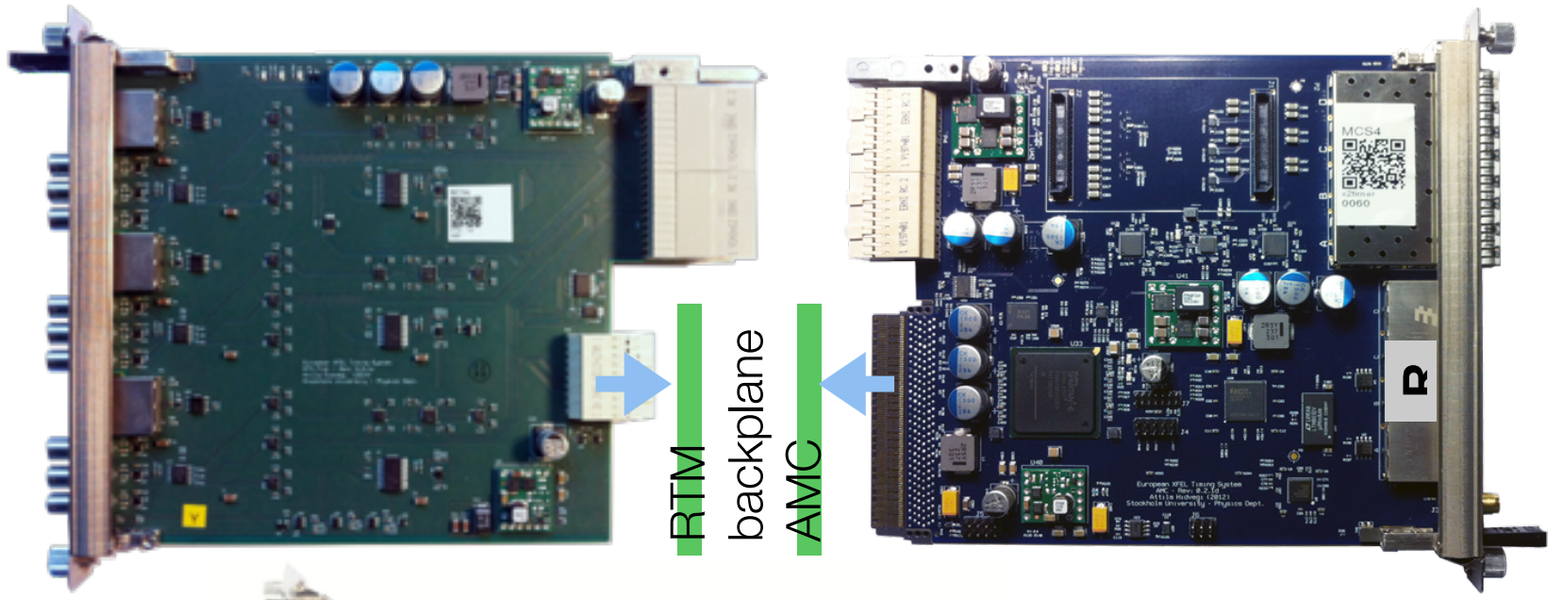
Optional **RTM**:
9 transmitters,
Further triggers or clocks

MicroTCA **backplane**:
TCLKA and TCLKB,
8 * M-LVDS

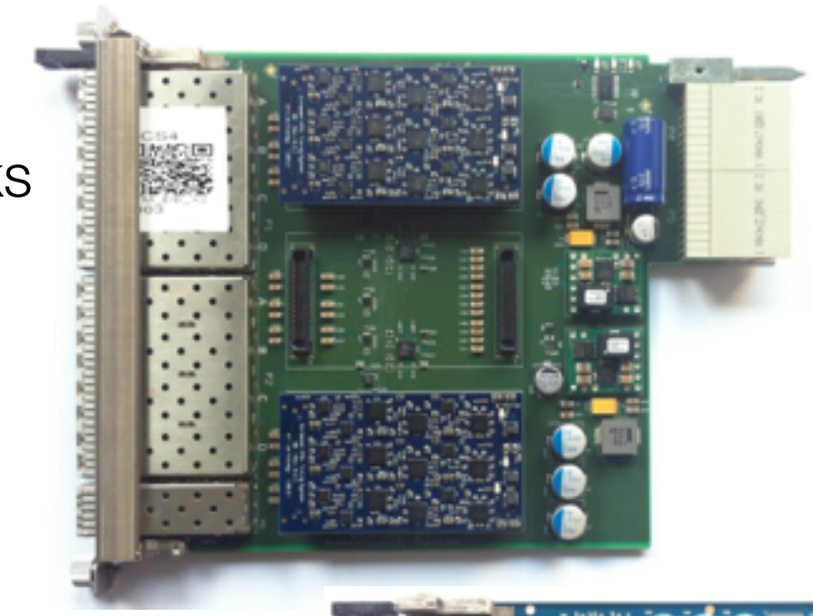


RTM Timing Extension Modules

9 Lemo outputs (50 Ohm):
- Triggers, Clocks, Data
- 3 channels with 5ps resolution



9 SFP outputs:
- length compensated fiber links



9 Fiber outputs (ST):
- Triggers, Clocks, Data
- used for modulators

Timing in a MicroTCA.4 Crate

Common modules

Application modules

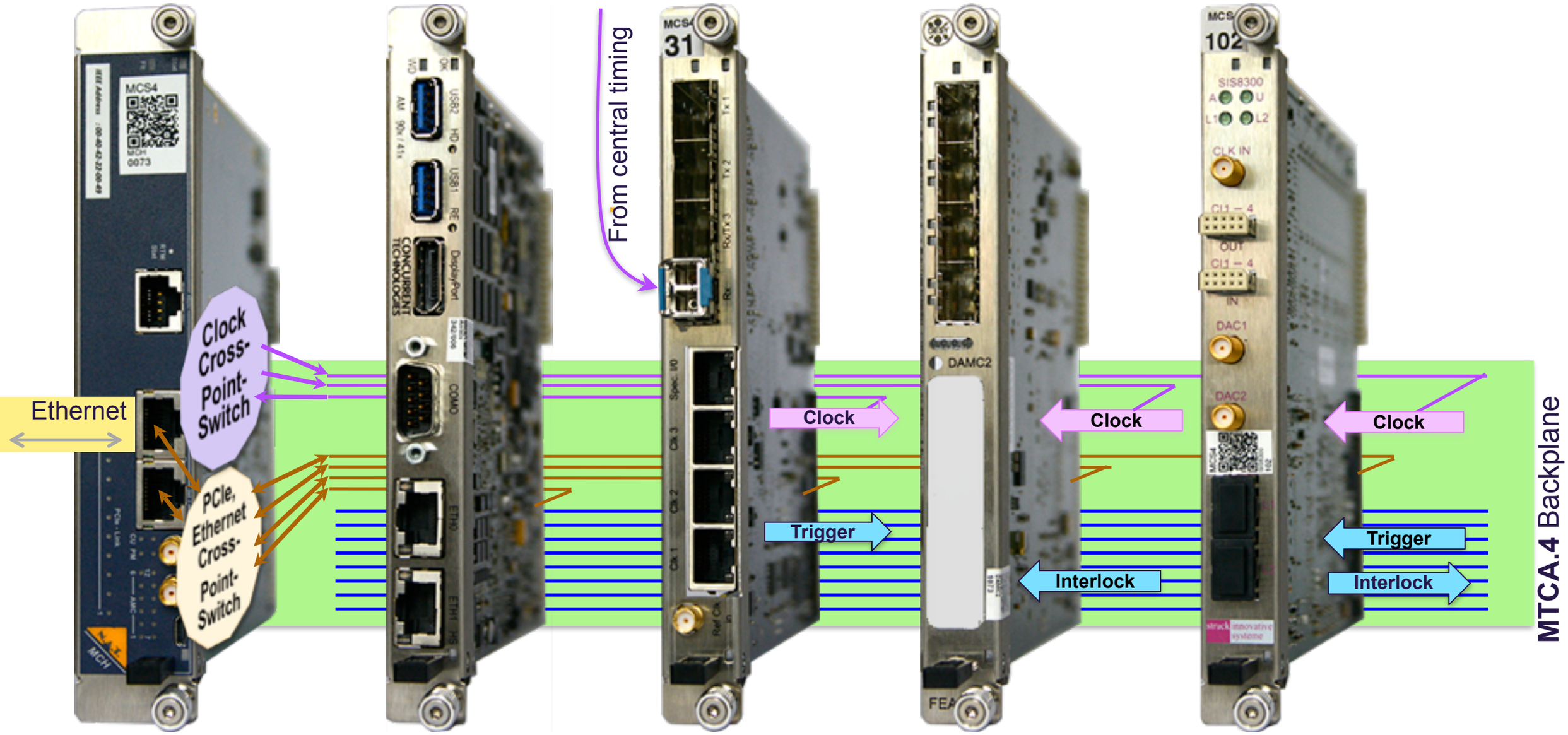
MCH
Management

CPU

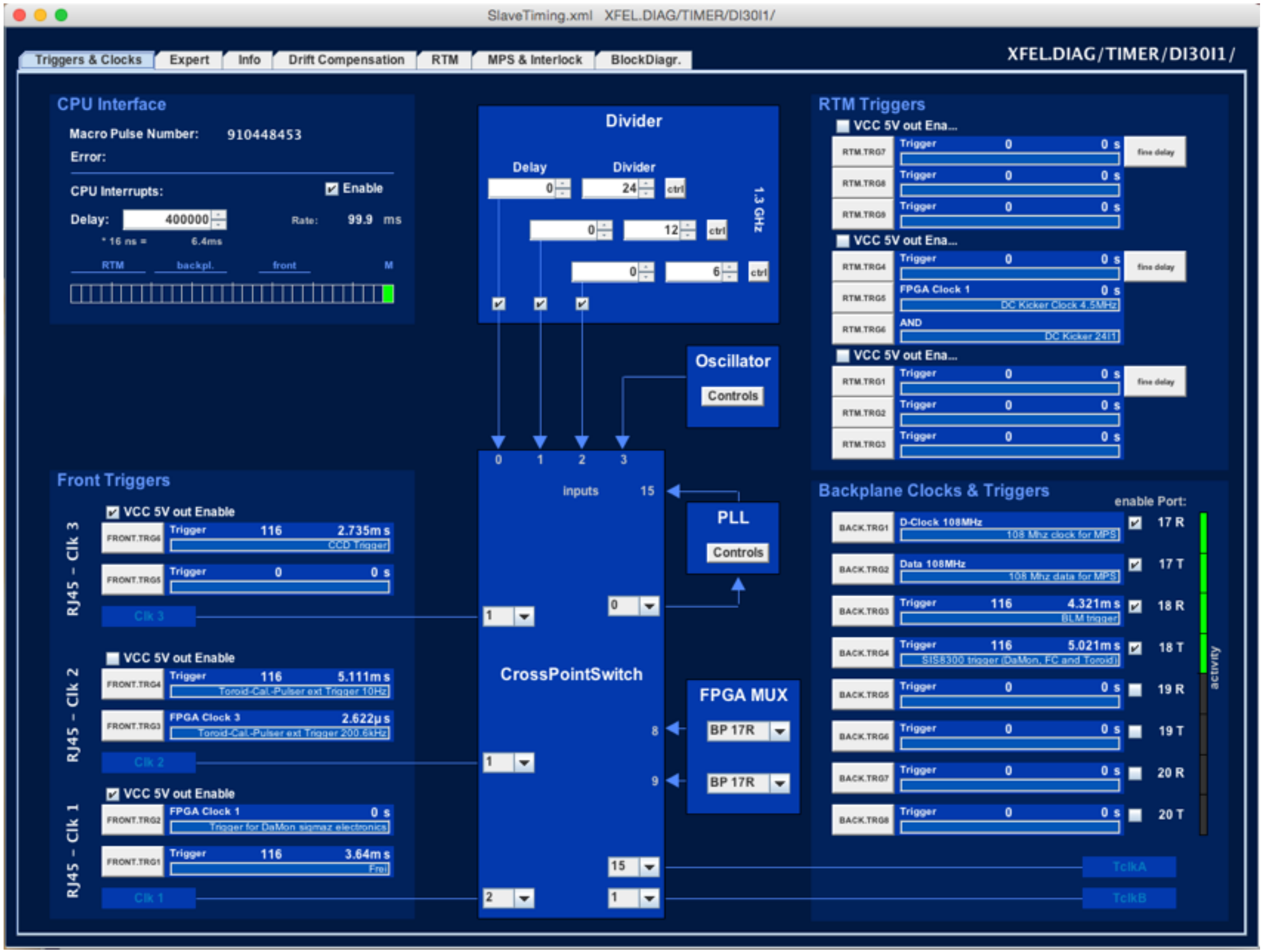
Timing

Machine
Protection
System

ADC
Digi. IO
Controller
….



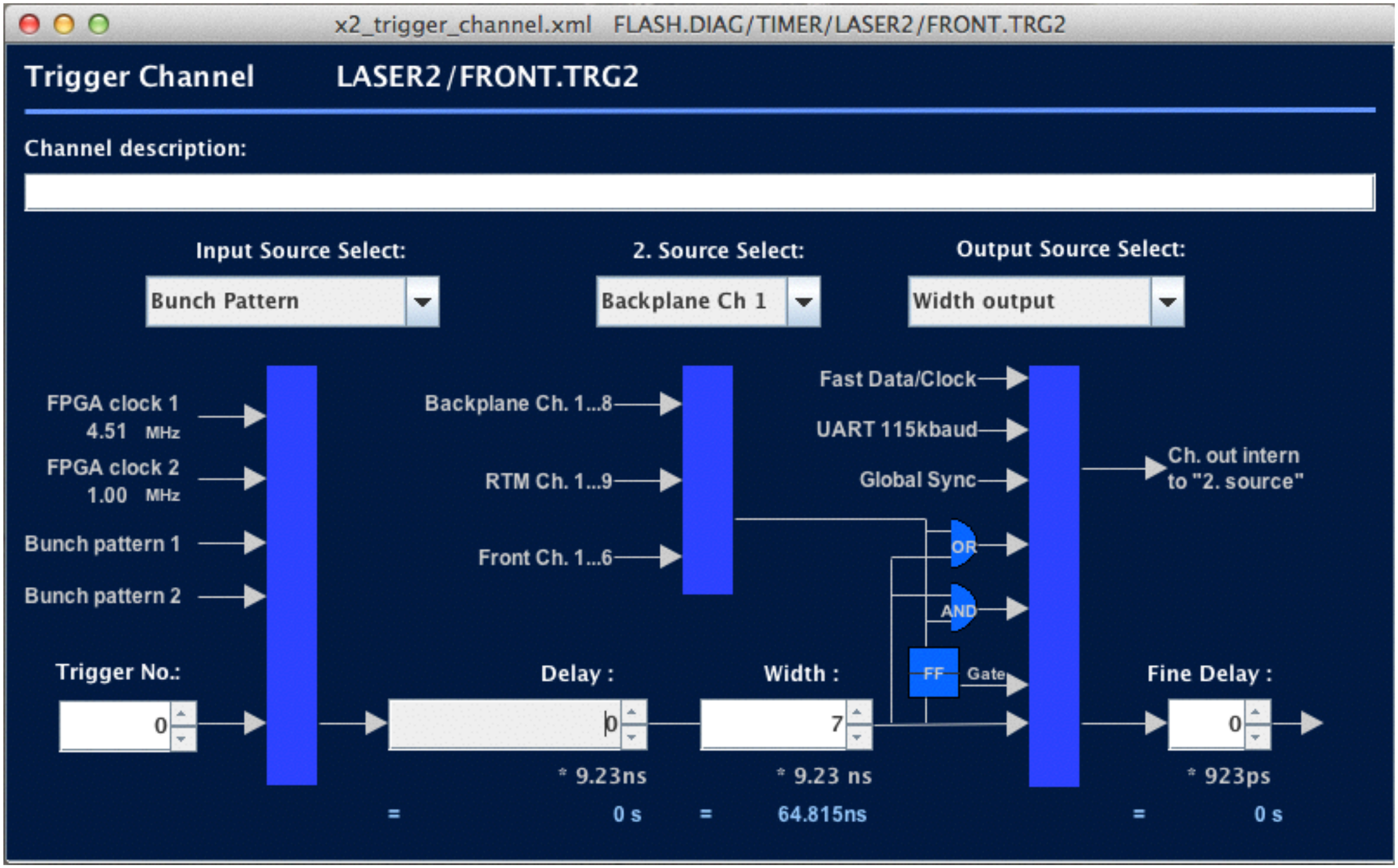
Timing Main Controls



23 Channels:
trigger/clock/data

5 Channels:
precision clocks

One Trigger/Clock/Data Channel Configuration



Delay and Width:
- up to 150ms
- in 9.23ns steps

Fine delay:
- 0.92ns steps

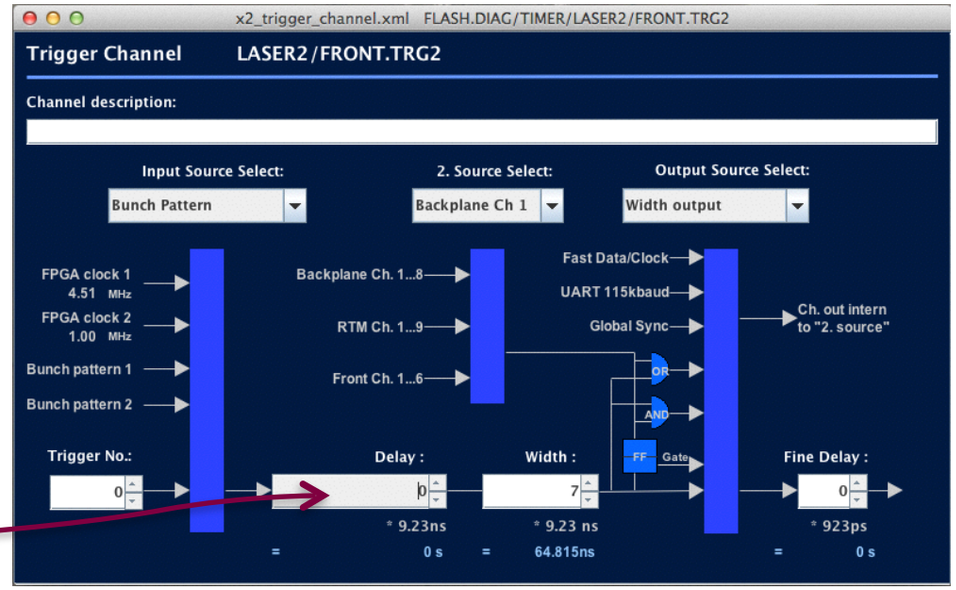
256 Triggers

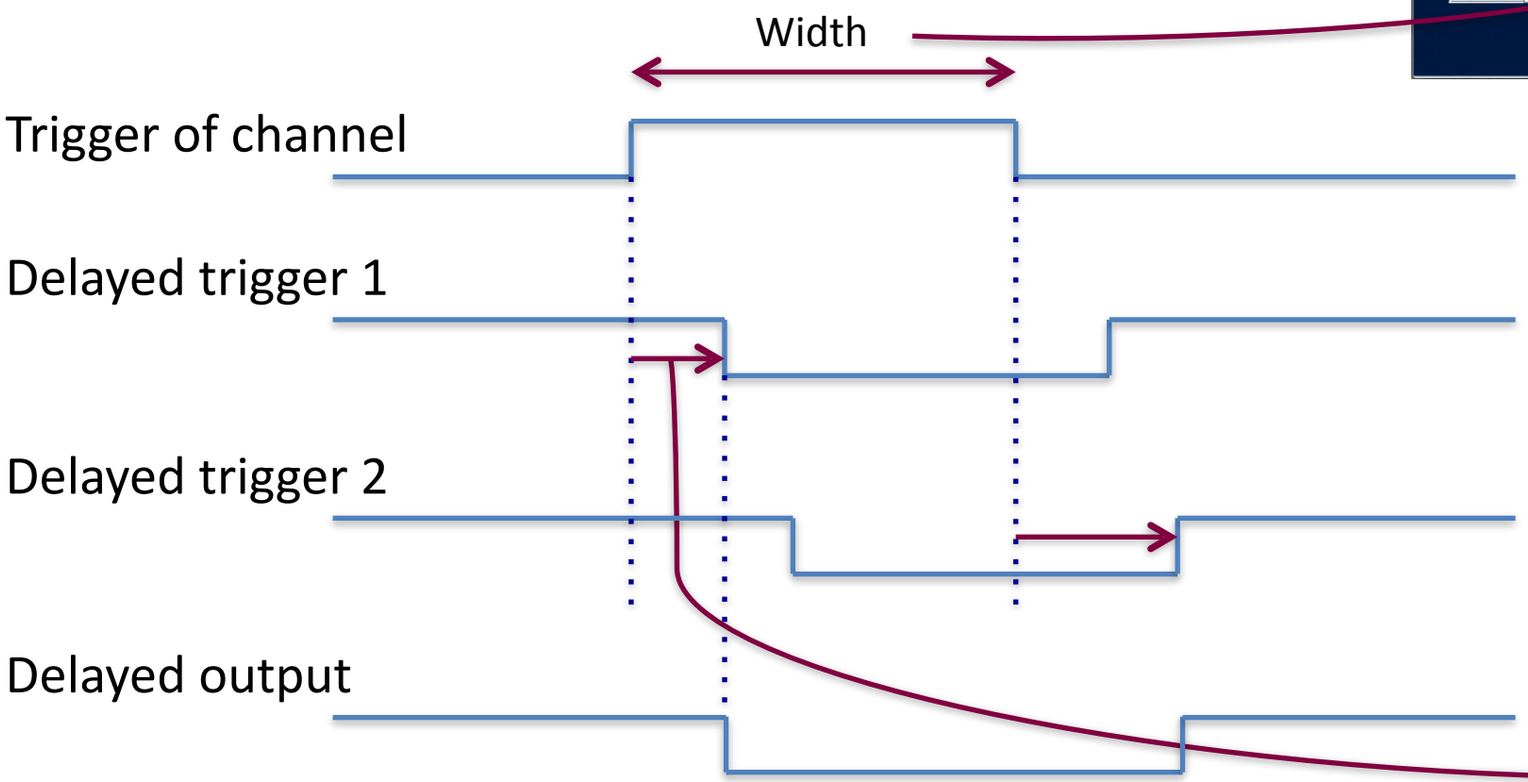
Selection of:
- Trigger #
- Bunch Pattern
- Clock from FPGA

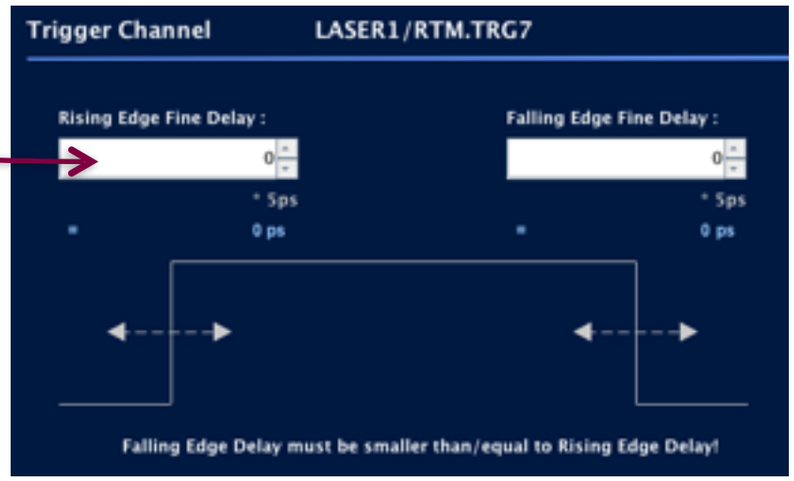
Combination w/ second channel:
- Gates
- Bursts
- Combine

Select source:
- Single delayed with width
- Combination
- Serial data

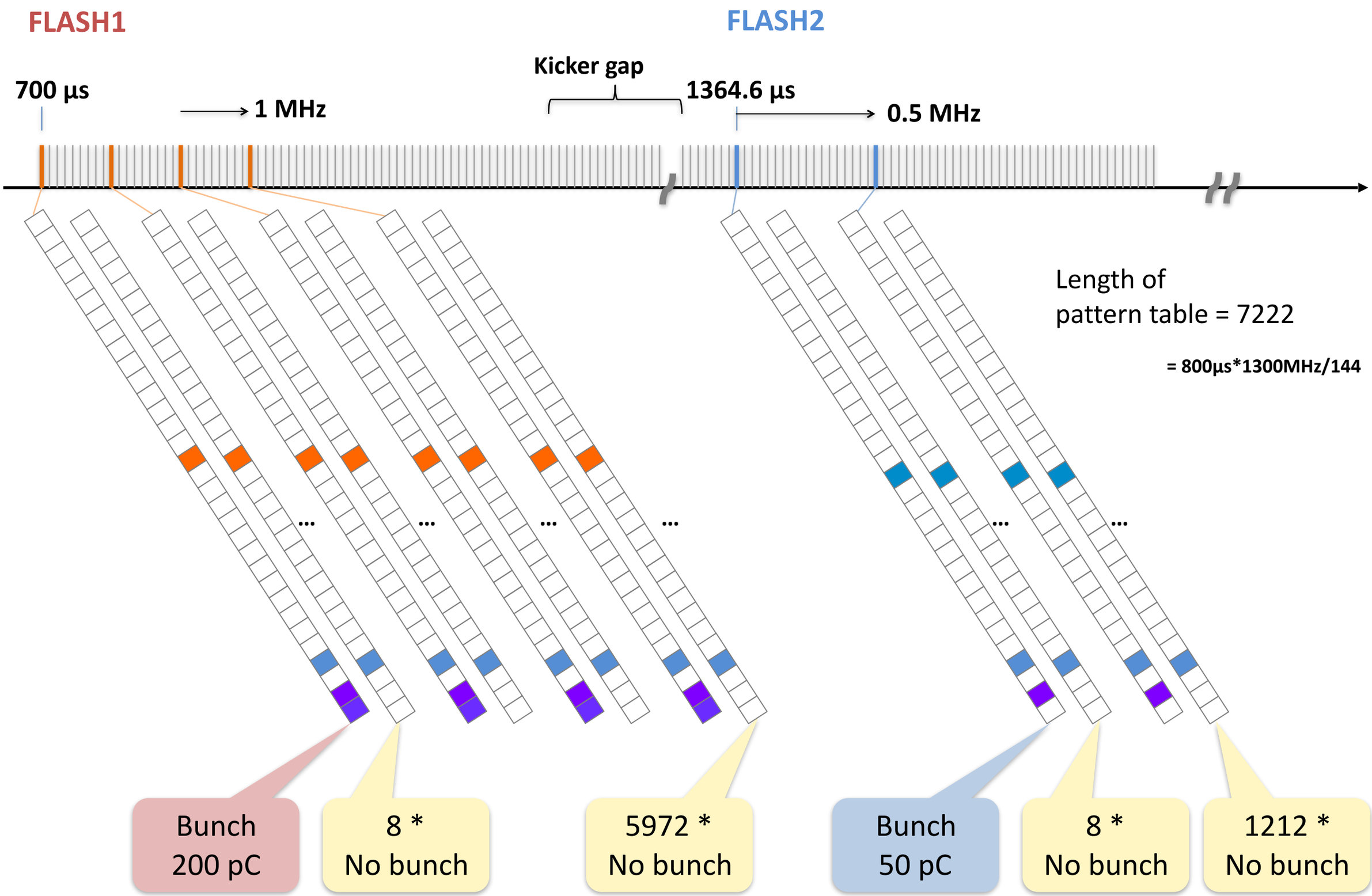
3 Channels with 5 ps resolution on RTM



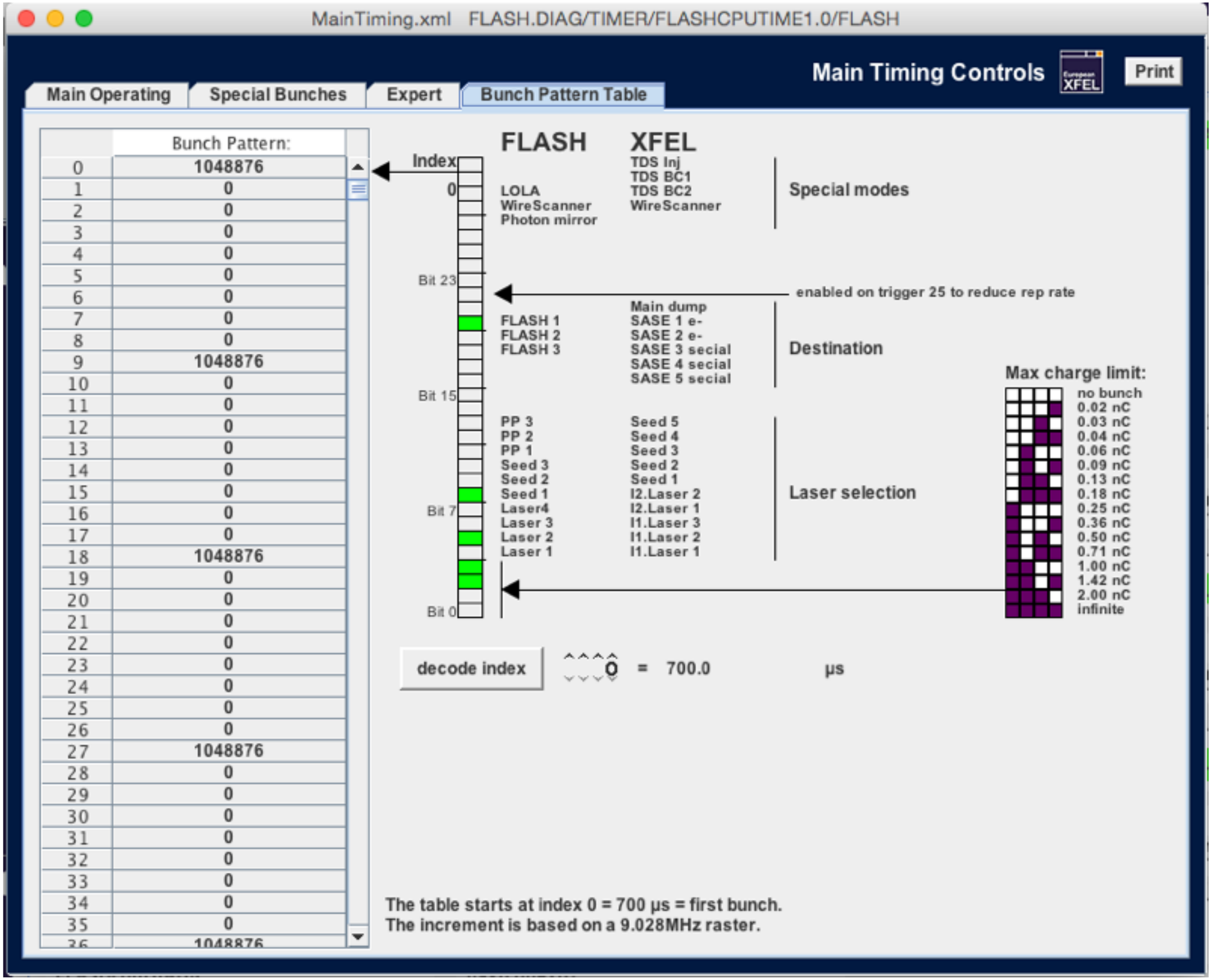




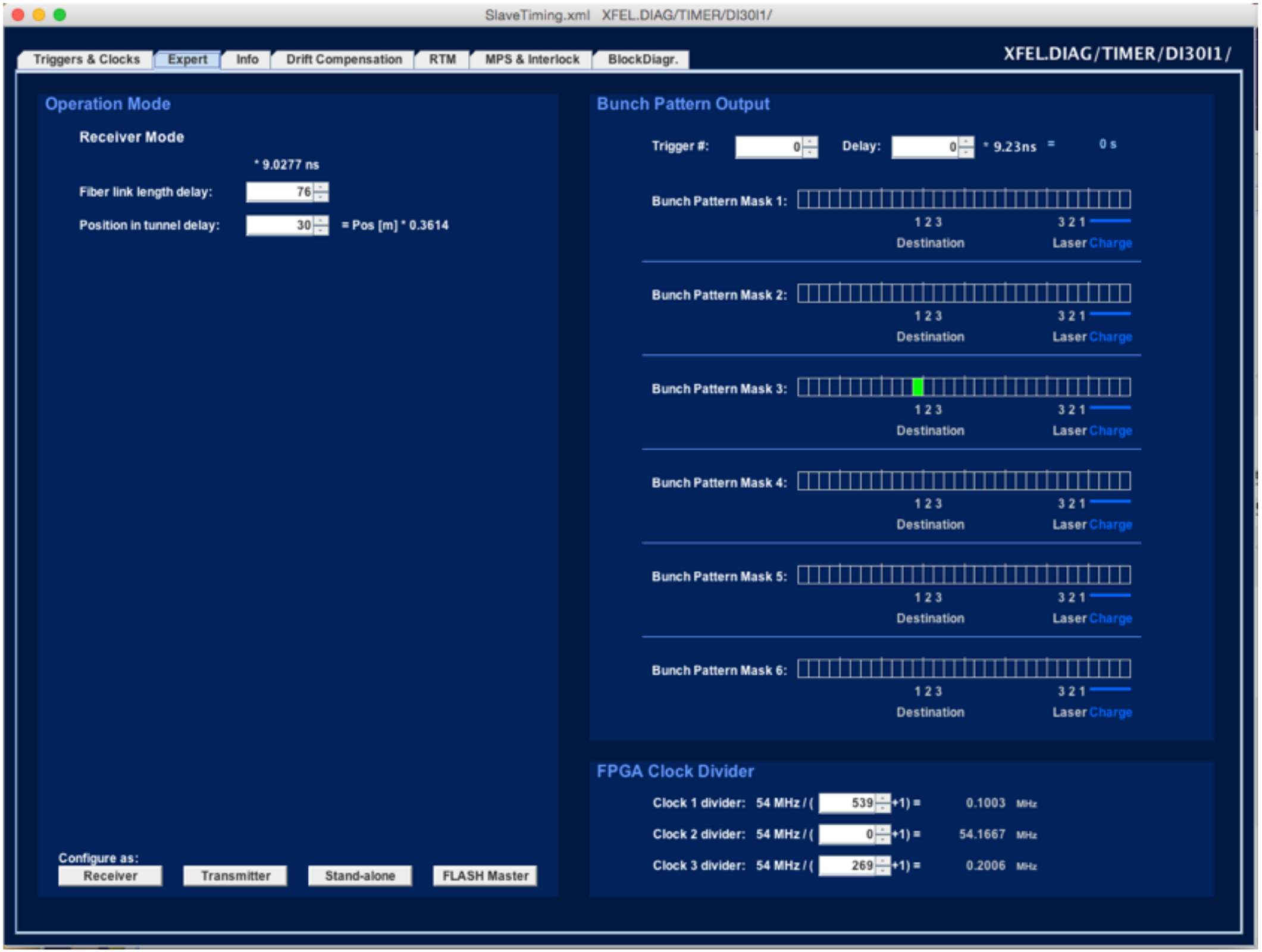
Bunch Pattern



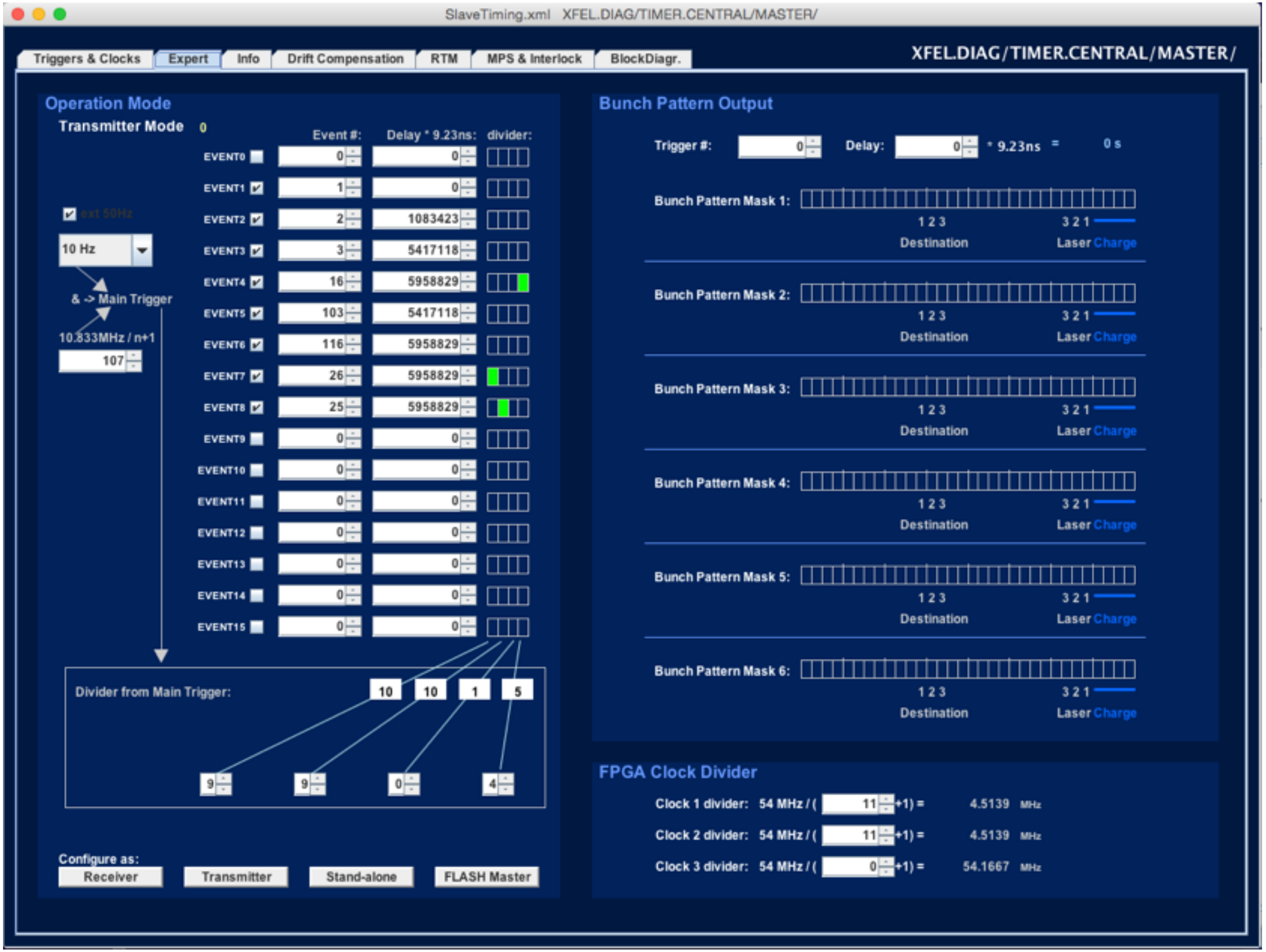
Bunch Pattern in the Timing System



Burst Outputs by Bunch Pattern



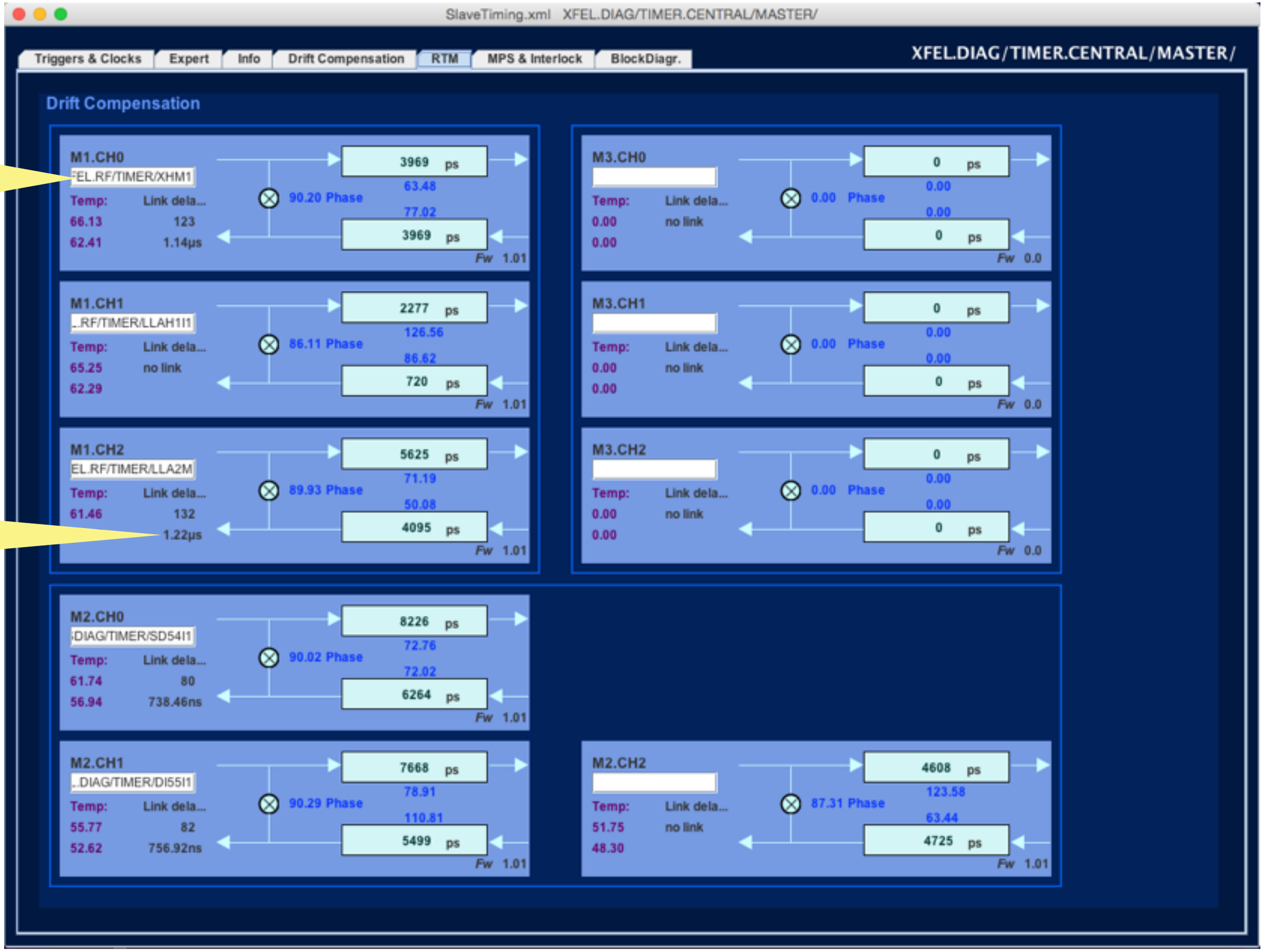
Master Timing: Definition of Triggers



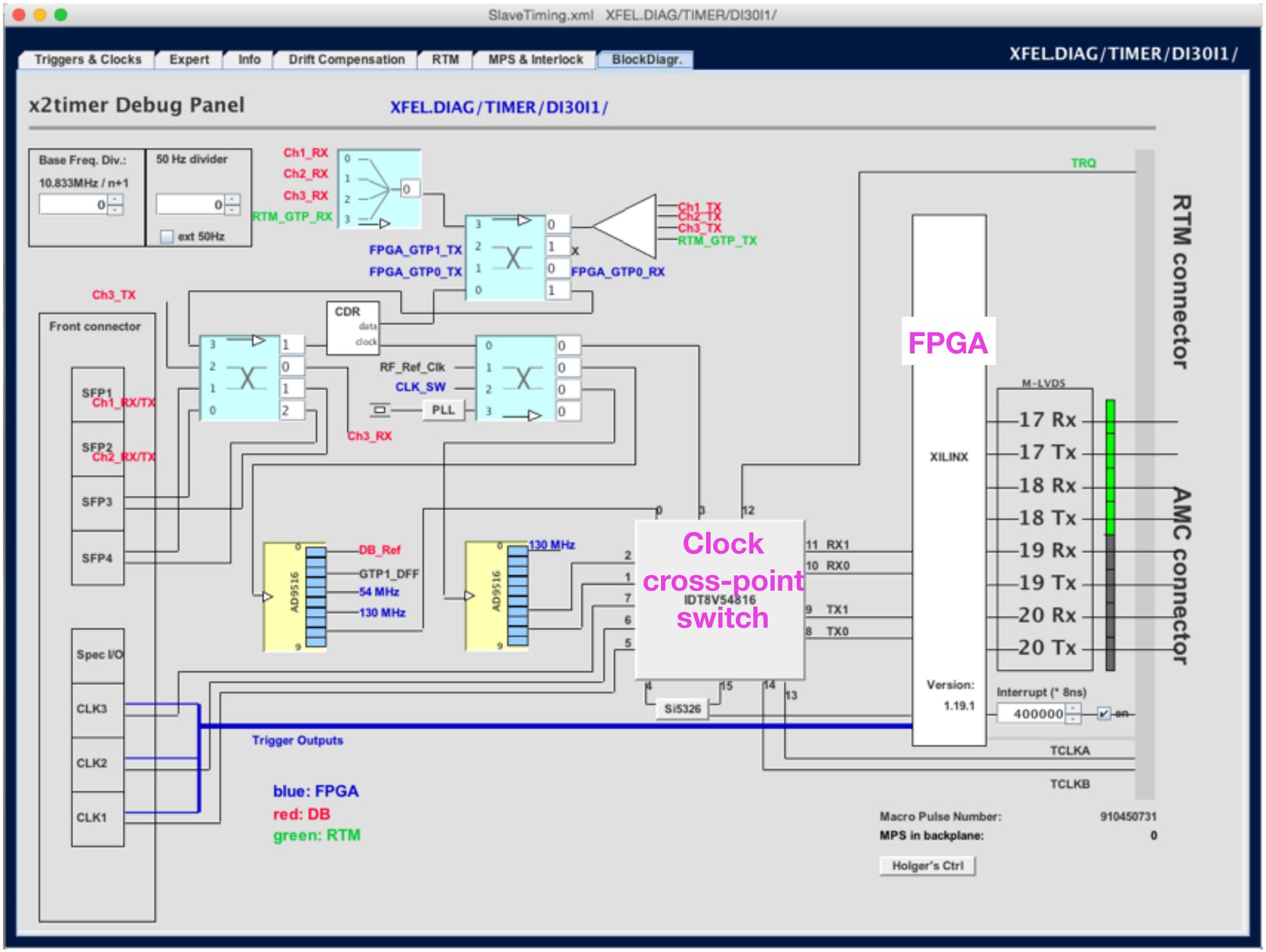
Fiber Link Outputs

Auto-detect: is connected to

Measured link delay



Timing Block Diagram



Summary

- 10 ps RMS jitter and drift after 4 km
- Provides:
  - Triggers with delays and width (9.23 ns resolution, 24 bit)
  - 3 Channels with 5 ps resolution on optional RTM
  - Wide rage clocks with and without FPGA
  - Distributes data words and tables
  - Divider synchronization with main rep rate
  - Outputs on: front, backplane, RTM, RTM backplane
- User panels for complex functions
- Timing server has 1880 properties (incl. 160 archive chan.)
- Available from N.A.T: NAMC_psTimer