Top Level

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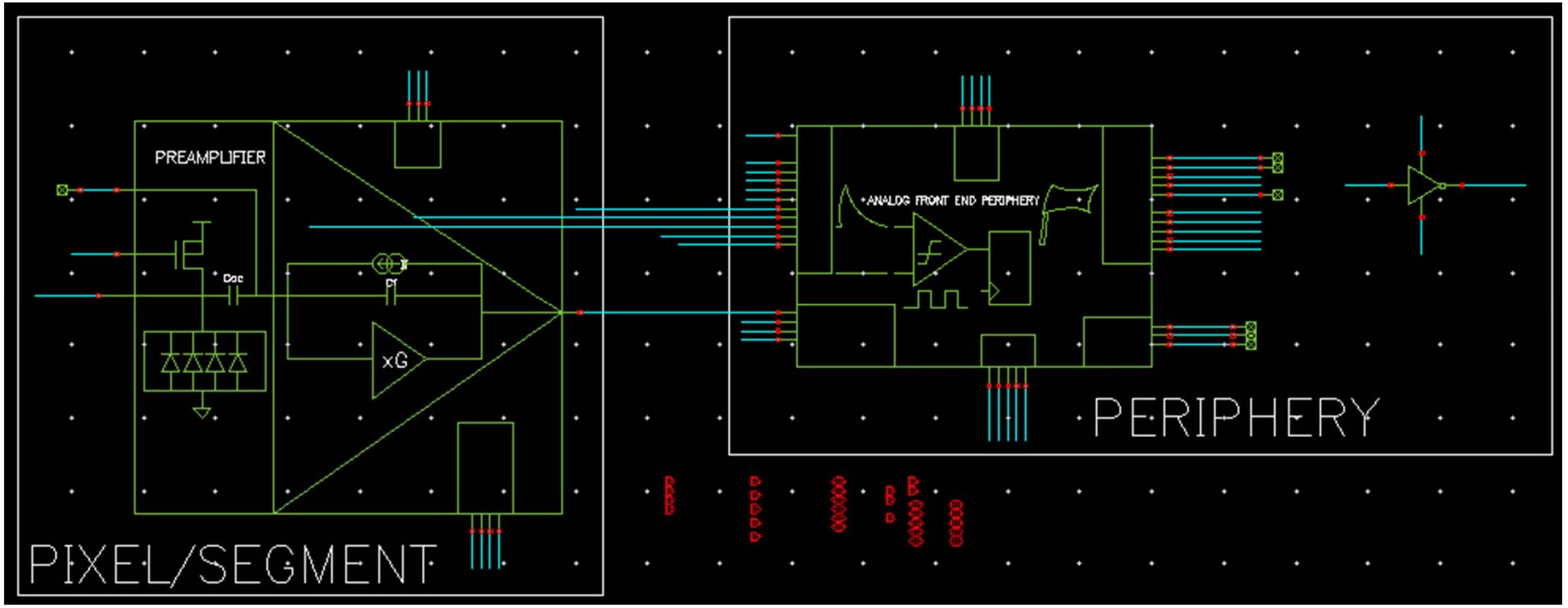
Front-end schematic



- 32 Pixels + 32 HIT Encoding blocks

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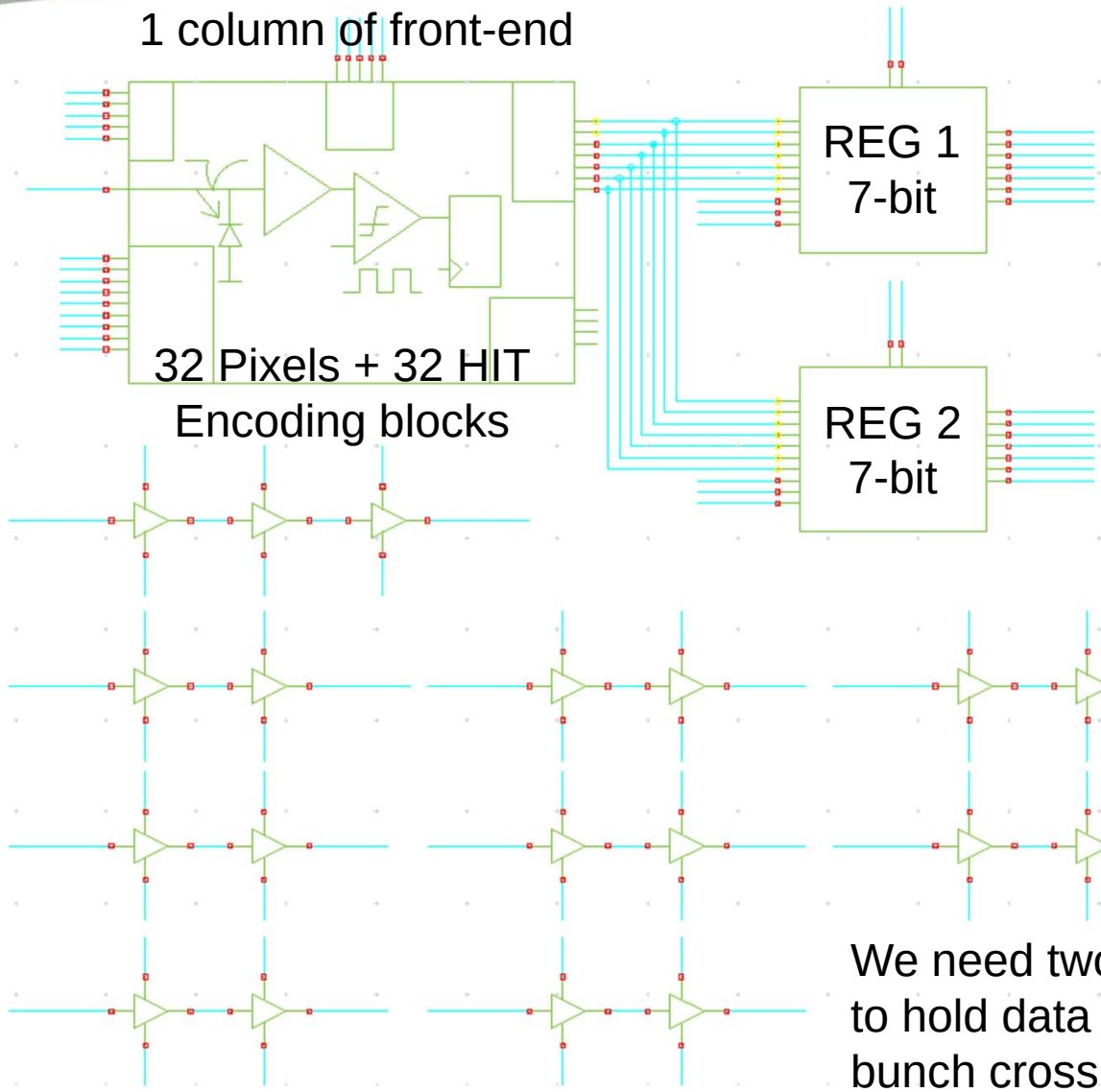
Complete column schematic



5-bit pixel address
+ 1-bit FLAG
+ 1-bit to indicate strip was hit

We need two 7-bit registers to hold data from 2 successive bunch crossings

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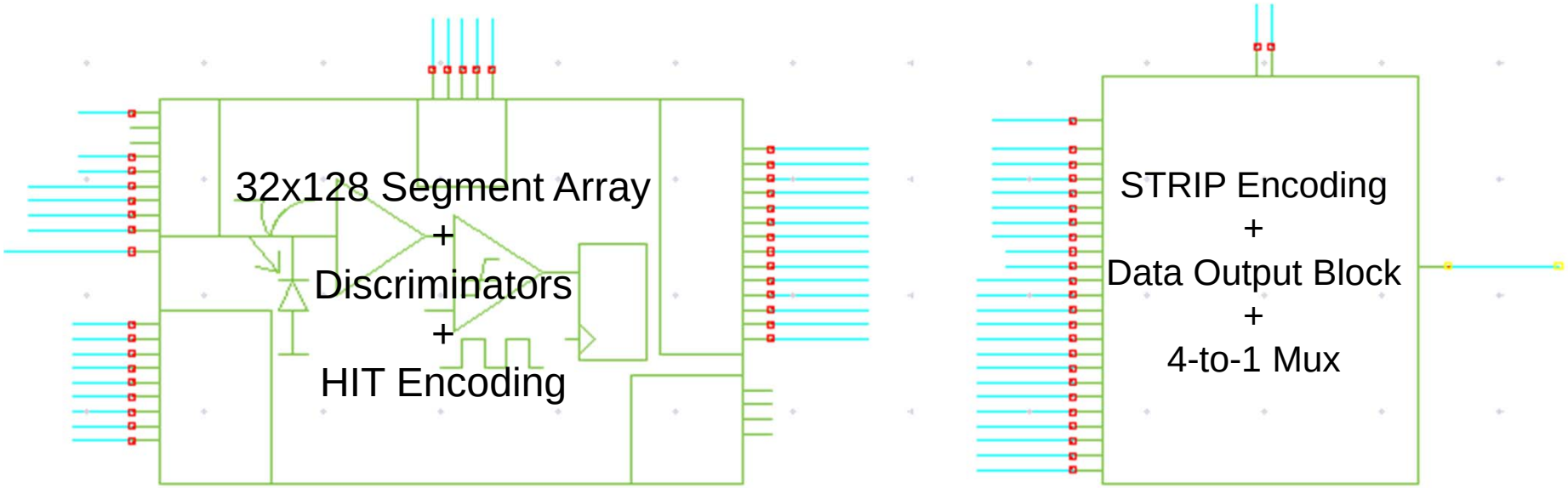
Top-level block



NOT Simulated in this block:

- Bias Generation
- CONFIG REG/SPI
- PLL
- LVDS

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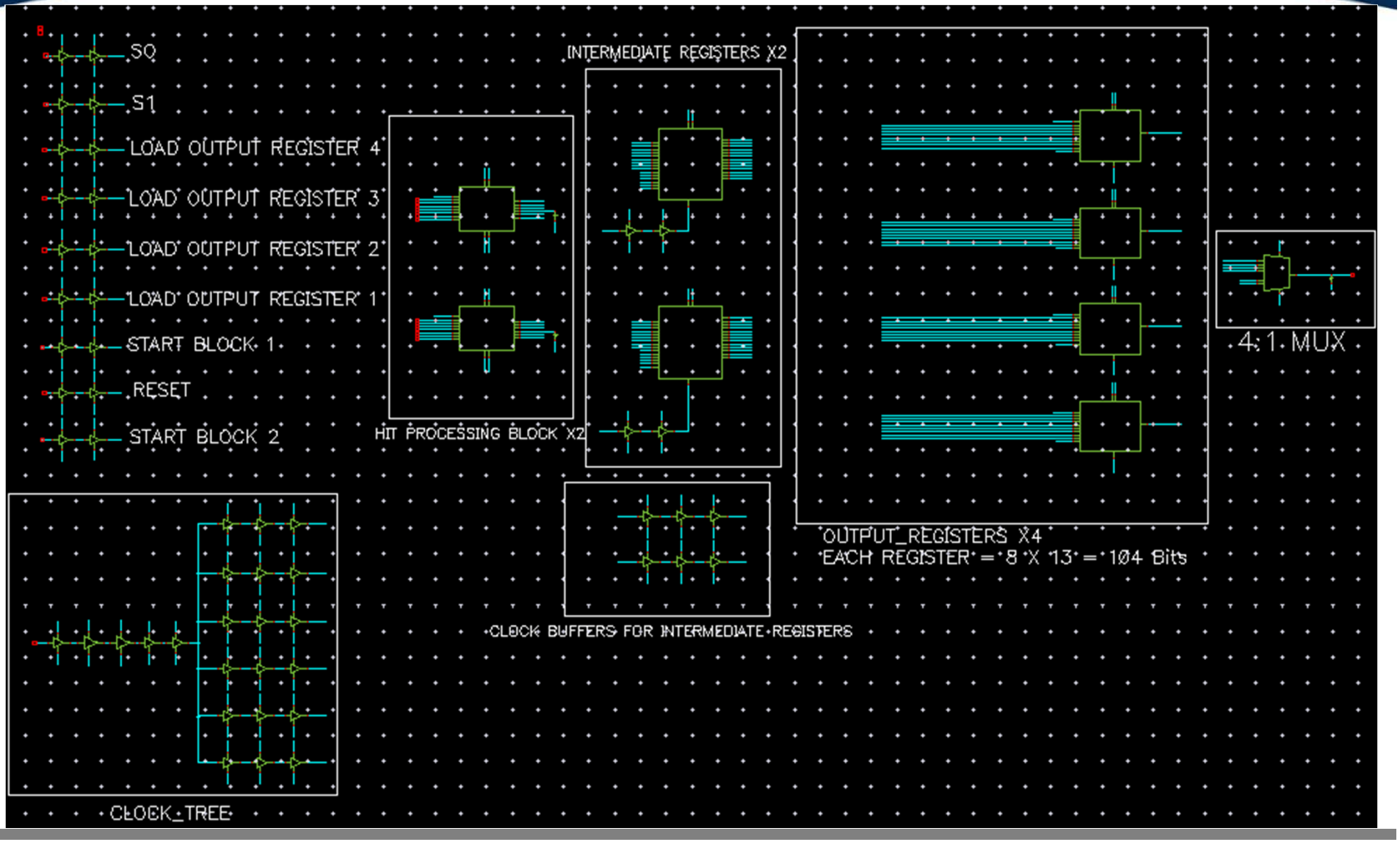
Strip Encoding and HIT Readout Block



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Top-Level simulation

- We simulate 3 Strips being hit
- For each strip the last Segment/Pixel was hit
- 7-bit Strip address Gray coded.
- Goal is to read out these 3 hits and output their address inside 2 bunch crossing periods or 50 ns.
- Clock period used in simulation is 320 MHz
- The Hit addresses corresponding to each bunch crossing are then stored and readout through LVDS stages every 25 ns.
- Table below shows the Hit locations and corresponding 7-bit Strip address (Gray coded).

Hits	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0	Strips
1	0	0	0	0	0	0	0	0
2	0	0	0	0	1	1	0	4
3	0	0	0	1	1	0	1	9

Data 4	Data 3	Data 2	Data 1	Data 0	Segment
1	0	0	0	0	32

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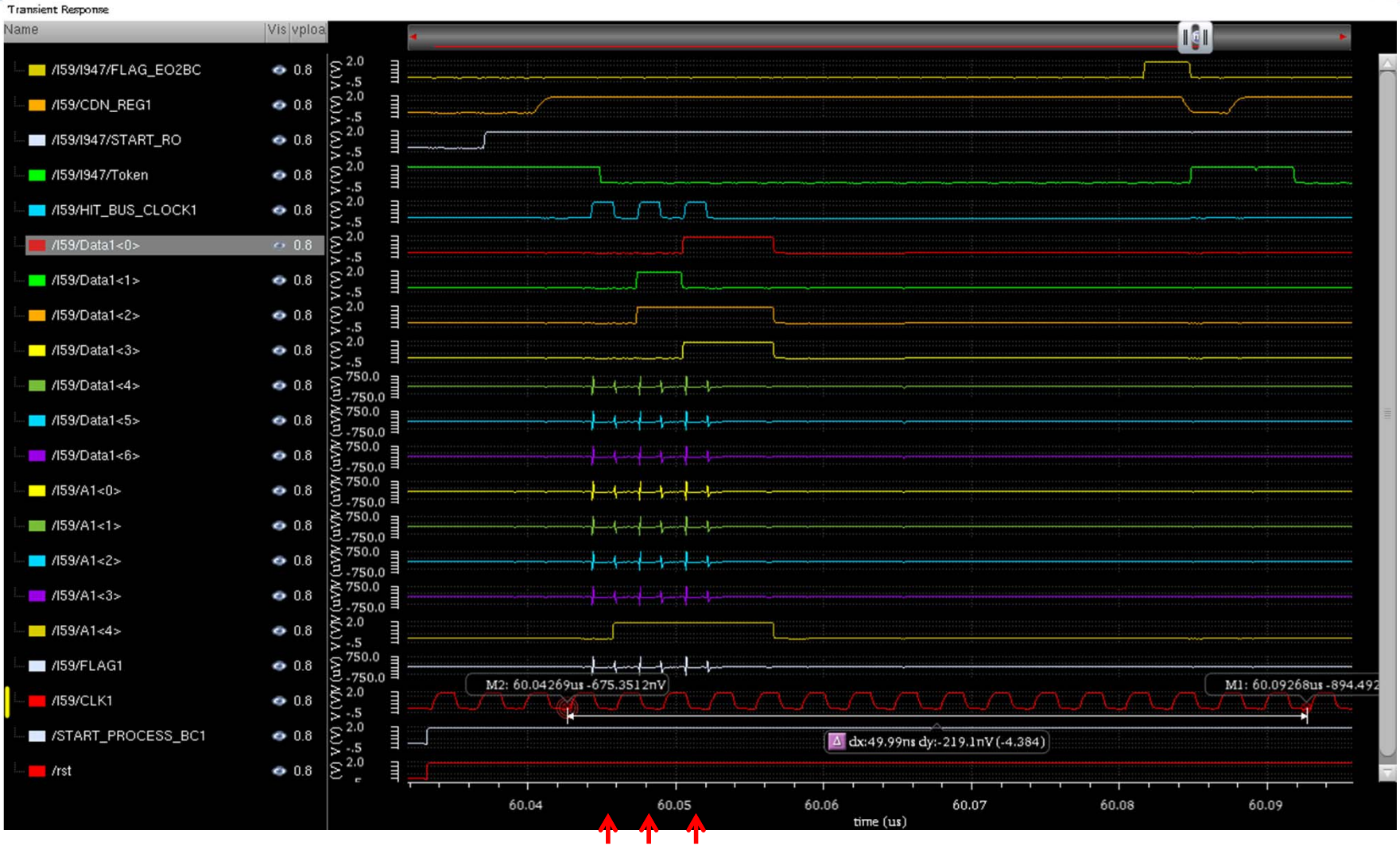
HIT detect & address output



Strip: 0 4 9

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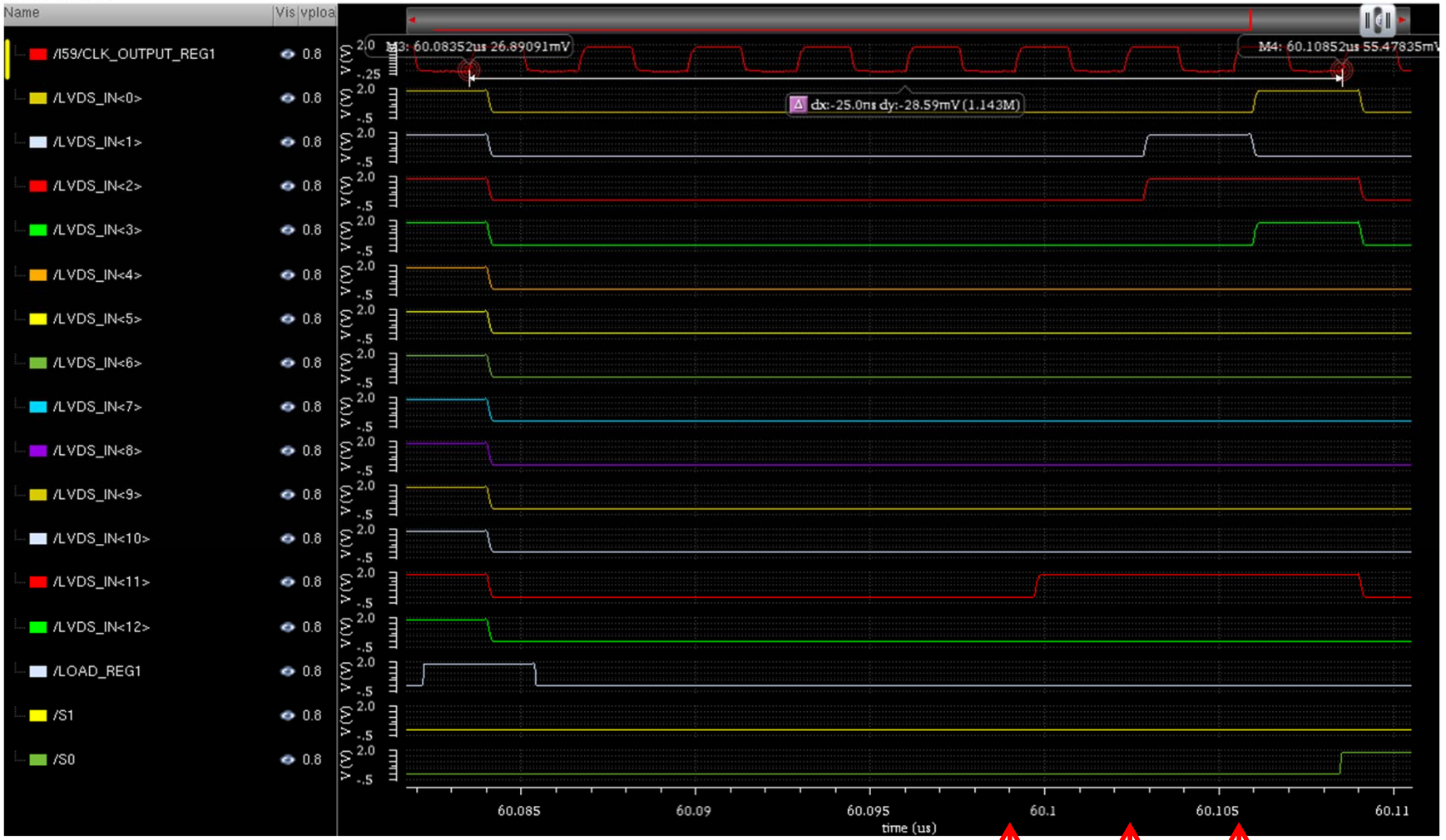
Input to LVDS



Strip: 0 4 9

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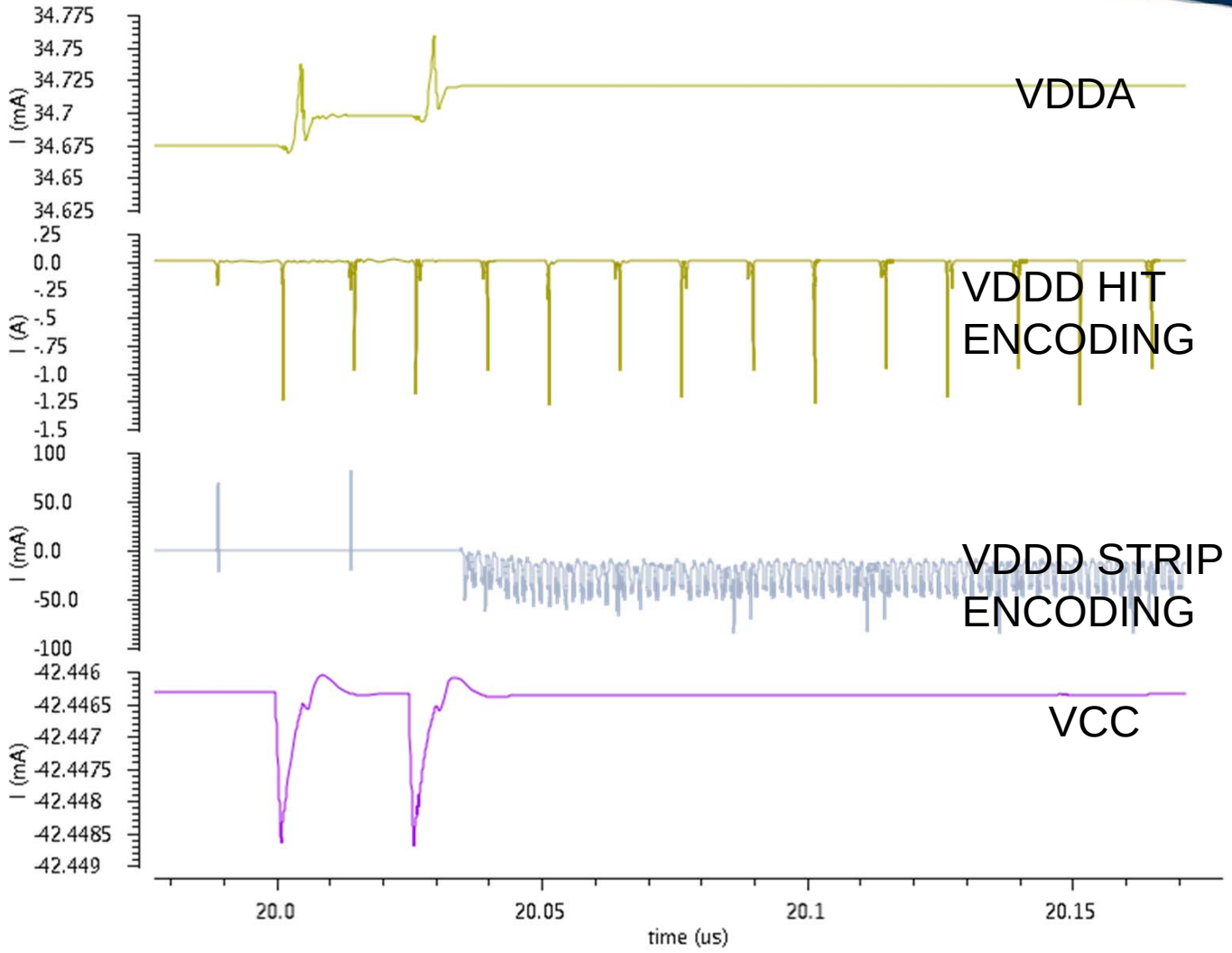
Top level simulation
Total power drawn

Rail	Irms
VDDD (Strip encoding)	2.2mA
VDDD (HIT Encoding)	7.6mA
vRef	42mA
VDDA	230mA



Temp=27C
Nominal corner