STRIP ENCODING

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HIT READOUT ILLUSTRATION

HIT READOUT ILLUSTRATION FOR 6 BUNCH CROSSINGS (BC)

		25ns	50ns	75ns	100ns	125ns	150ns	175ns	200ns	225ns
	BUNCH CROSSINGS (BC)	BC1	BC2	BC3	BC4	BC5	BC6			
ODD BUNCH GROUP	128-bit REG	REG1	RESET	REG1	RESET	REG1	RESET	REG1	RESET	REG1
EVEN BUNCH GROUP	128-bit REG	RESET	REG2	RESET	REG2	RESET	REG2	RESET	REG2	RESET
ODD BC	HIT PROCESSING BLOCK 1		PROCESS BC1		PROCESS BC3		PROCESS BC5		PROCESS BC7	
EVEN BC	HIT PROCESSING BLOCK 2			PROCESS BC2		PROCESS BC4		PROCESS BC6		PROCESS BC8
ODD BC	8x13-bit INTERMEDIATE REG1		STORE BC1		STORE BC3		STORE BC5		STORE BC7	
EVEN BC	8x13-bit INTERMEDIATE REG2			STORE BC2		STORE BC4		STORE BC6		STORE BC8
	8x13-bit OUTPUT REG1				READ BC1				READ BC5	
ODD BUNCH GROUP	8x13-bit OUTPUT REG2					READ BC2				READ BC6
	8x13-bit OUTPUT REG3						READ BC3			
EVEN BUNCH GROUP	8x13-bit OUTPUT REG4							READ BC4		
	OUTPUT				BC1	BC2	BC3	BC4	BC5	BC6
		LATENCY = 75ns			**OUTPUT 8 HITS PER BC PERIOD**					

IF LESS THAN 8 HITS IN ANY BC PERIOD THEN FILL WITH '1' TO DENOTE BLANK HITS

We use 4 OUTPUT REGs instead of 2 as we already have silicon proven 4-to-1mux following the registers; some penalty in space and power is paid but this block draws very little power when compared to the analogue blocks and compared to the array occupies a small percentage of total area.

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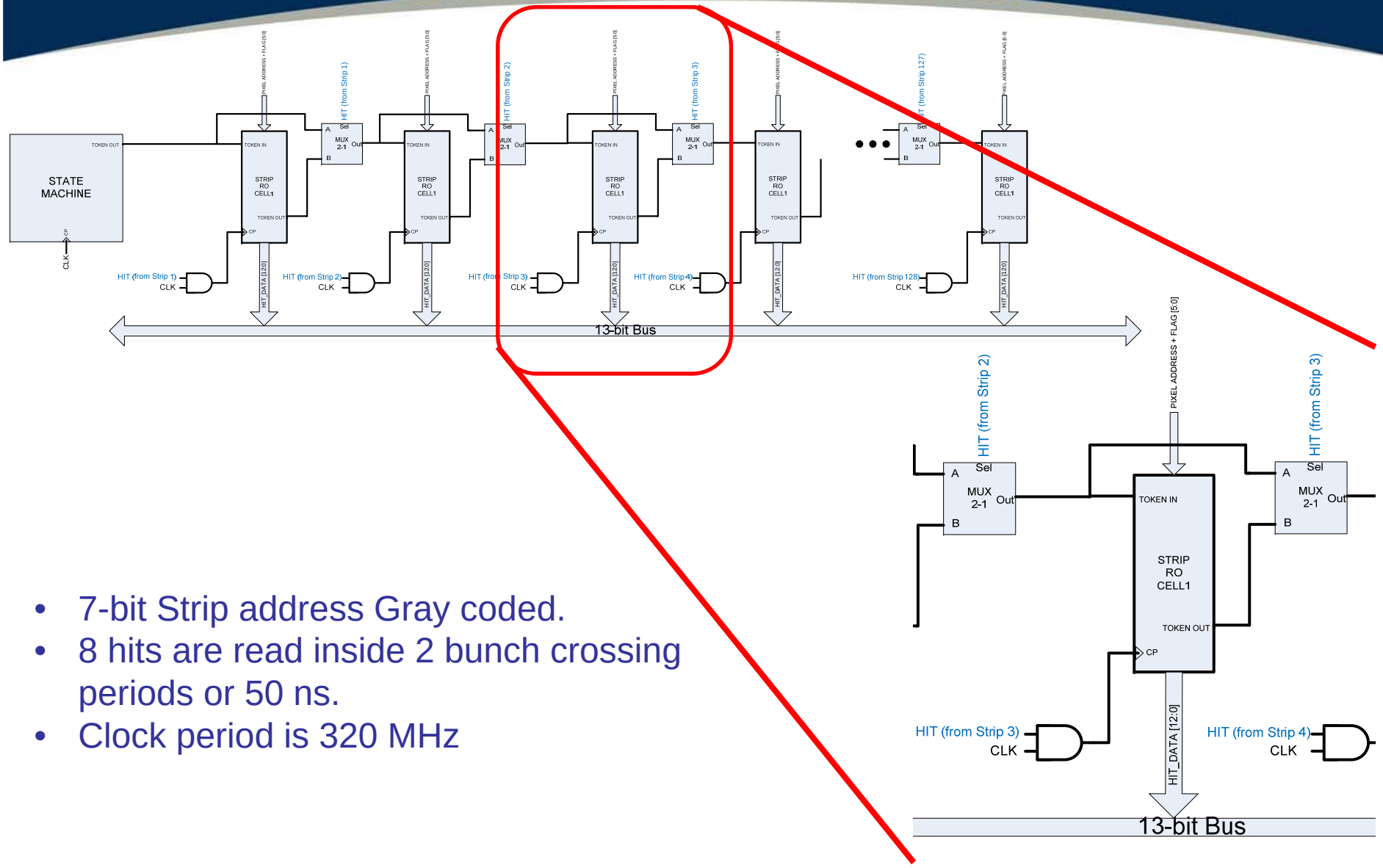
Strip Encoding Functional Block Diagram



- 7-bit Strip address Gray coded.
- 8 hits are read inside 2 bunch crossing periods or 50 ns.
- Clock period is 320 MHz

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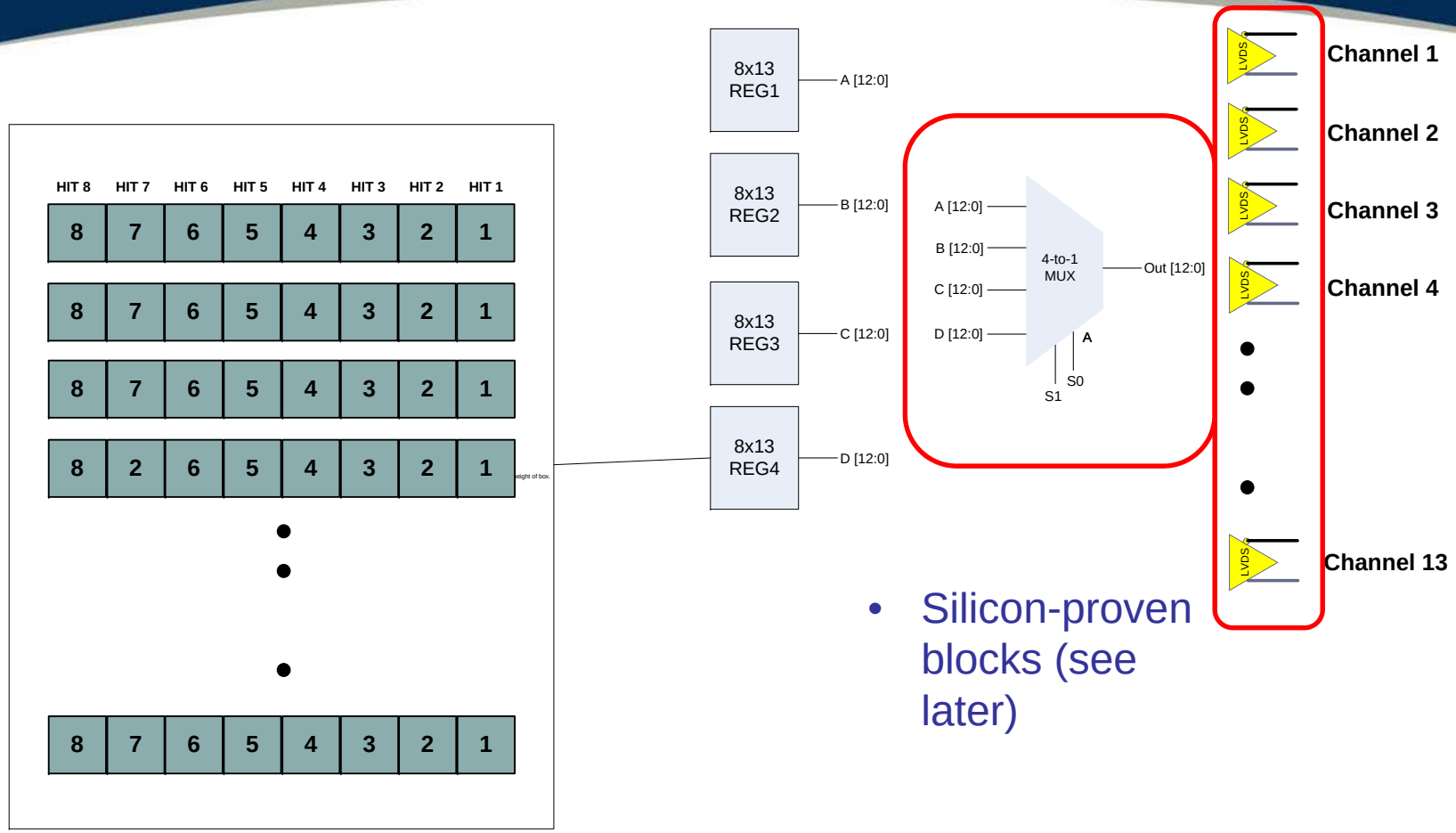
Data Output Block



- Silicon-proven blocks (see later)

- 4.16 Gbits/sec total data-rate
- Each LVDS channel operates at 320 Mbits/sec (single data-rate)
- Read-out 104-bits in 25 ns
- Reference clock for sync to be added (not shown here)

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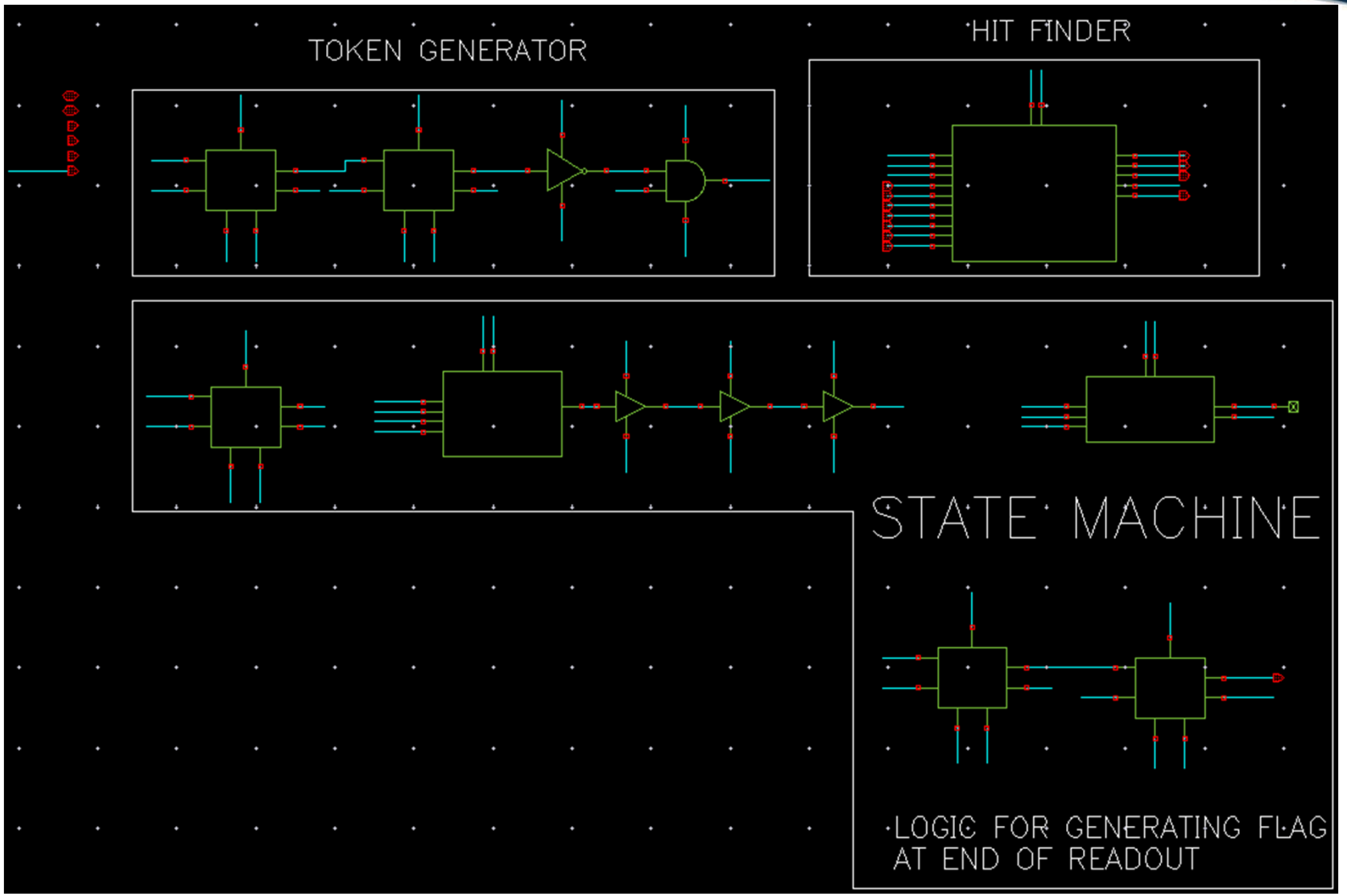
HIT Processing Block



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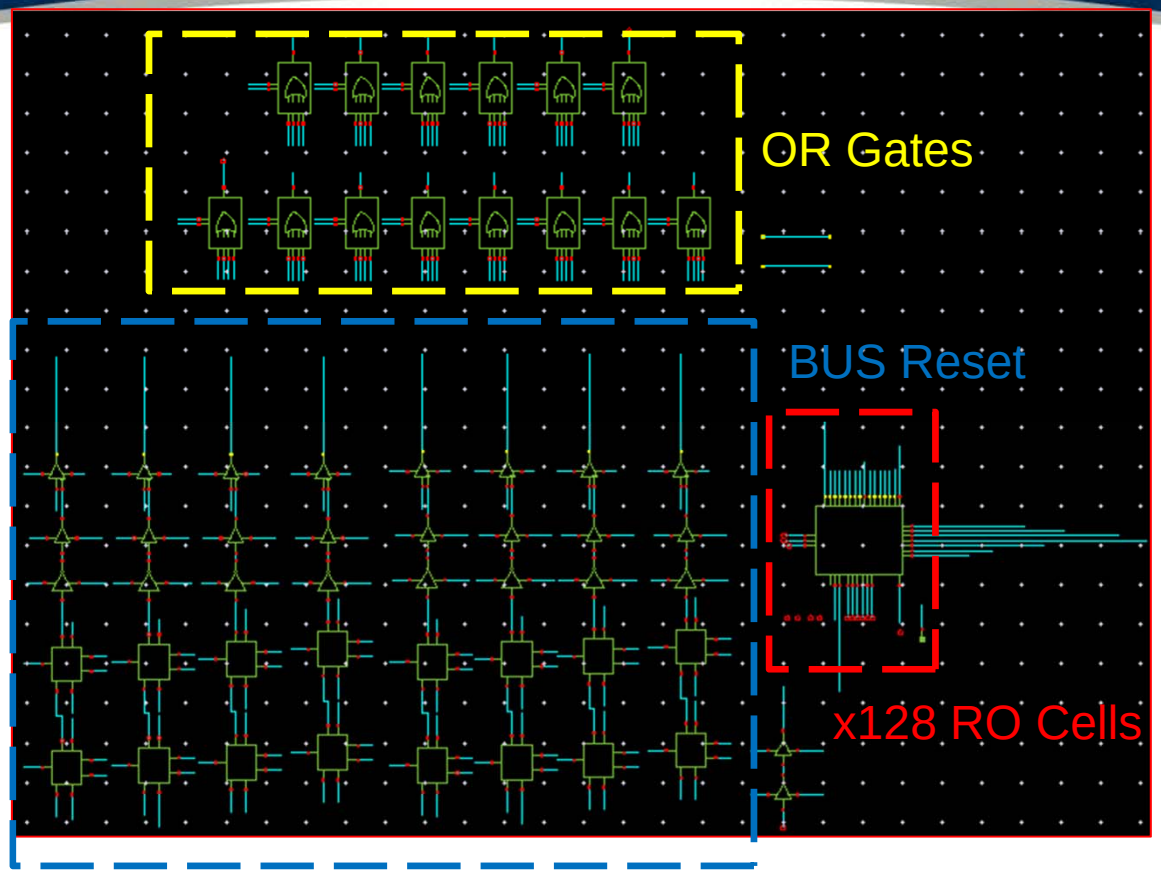
HIT Finder Block



- There are two multi-bit buses and two 1-bit bus; each bus is divided into 4 parts
- The buses are divided to reduce loading; dividing the buses improves SR
- Each part of a bus serves 32 RO cells; need to OR the signal of each part in the bus
- We need 4 input OR gate; we also need to bring the bus back to known state once the Token passes through; we use the Token to reset the state of the Bus to 0V

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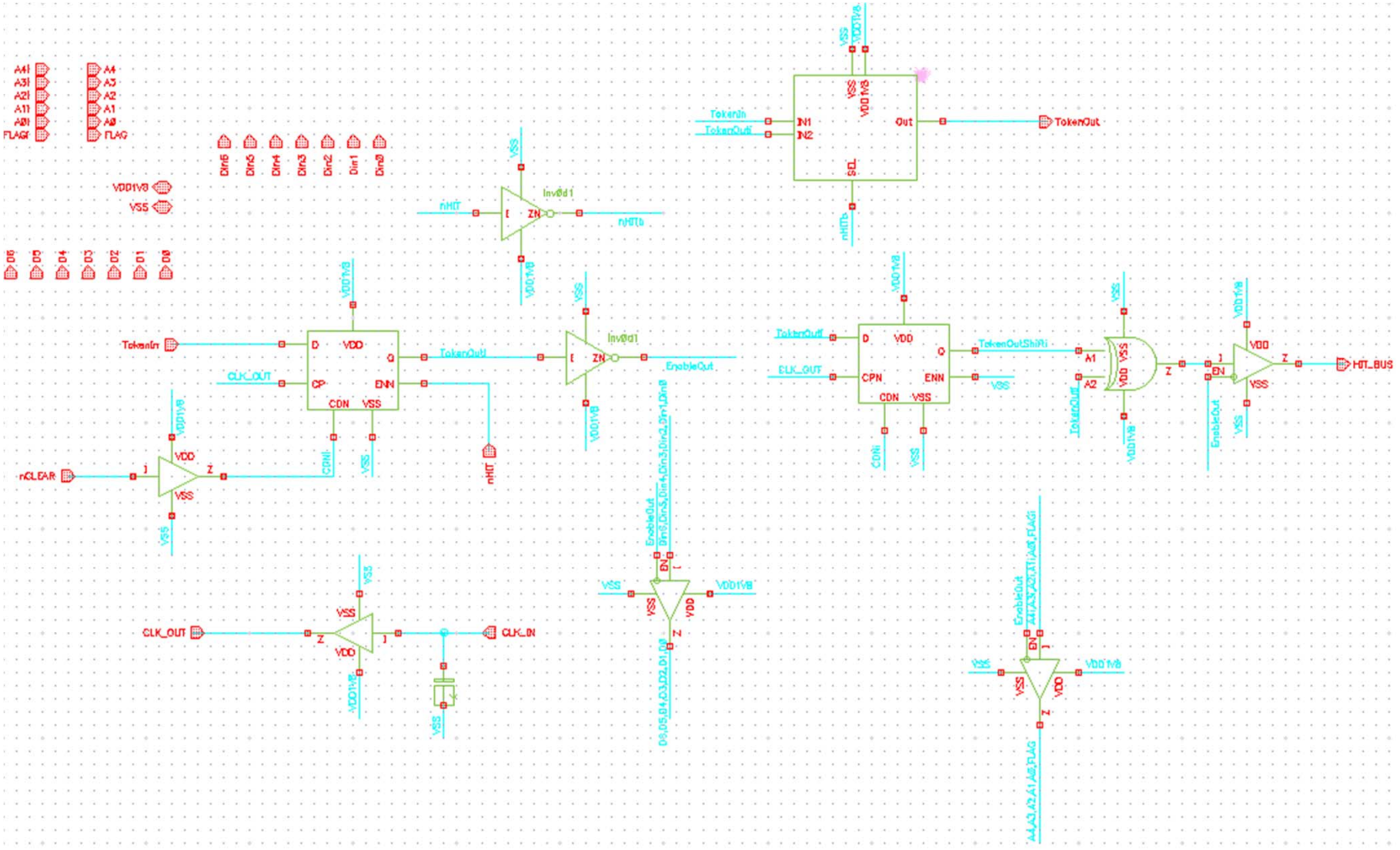
STRIP Readout Cell with Fast Skip Logic



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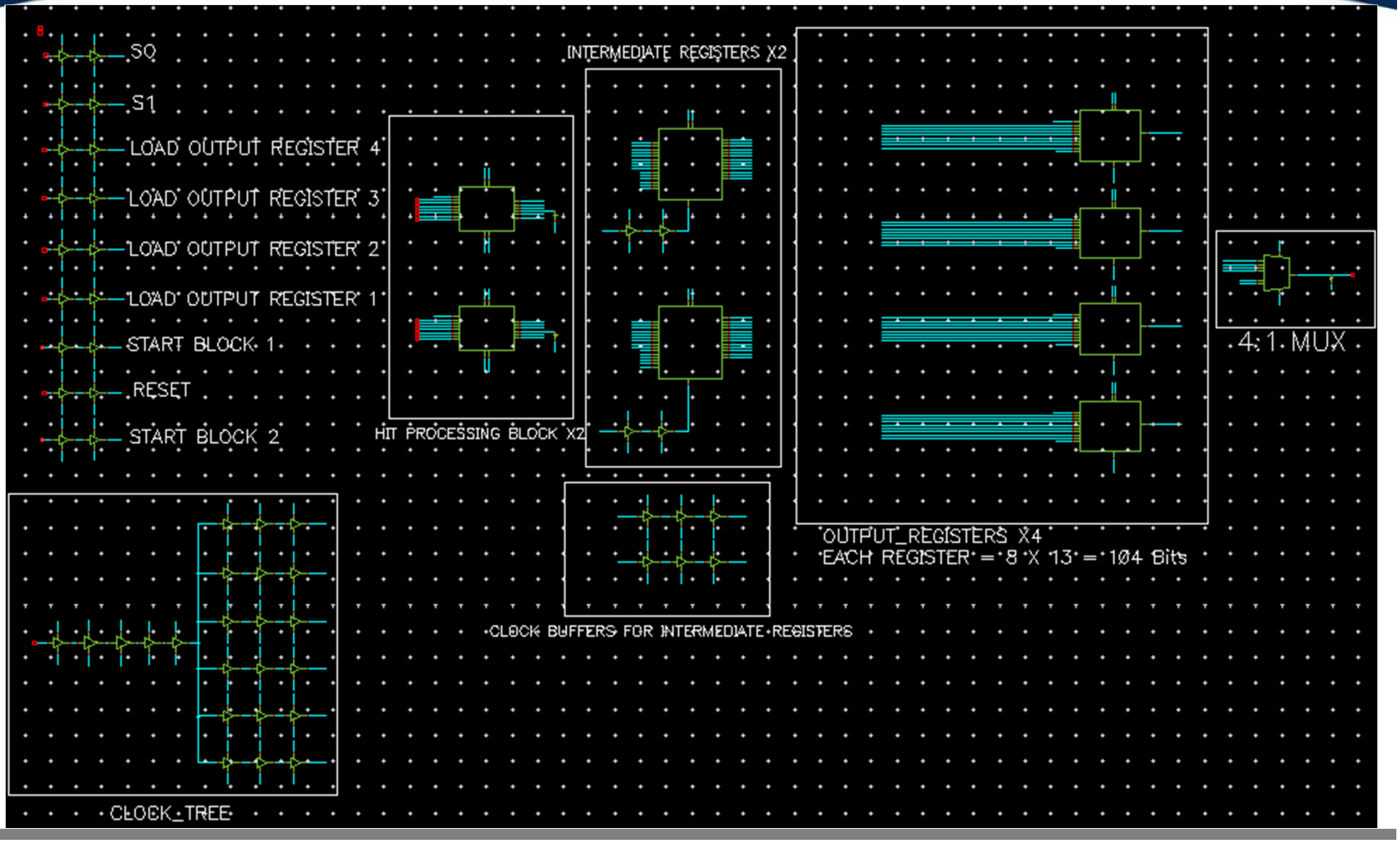
Strip Encoding and HIT Readout Block



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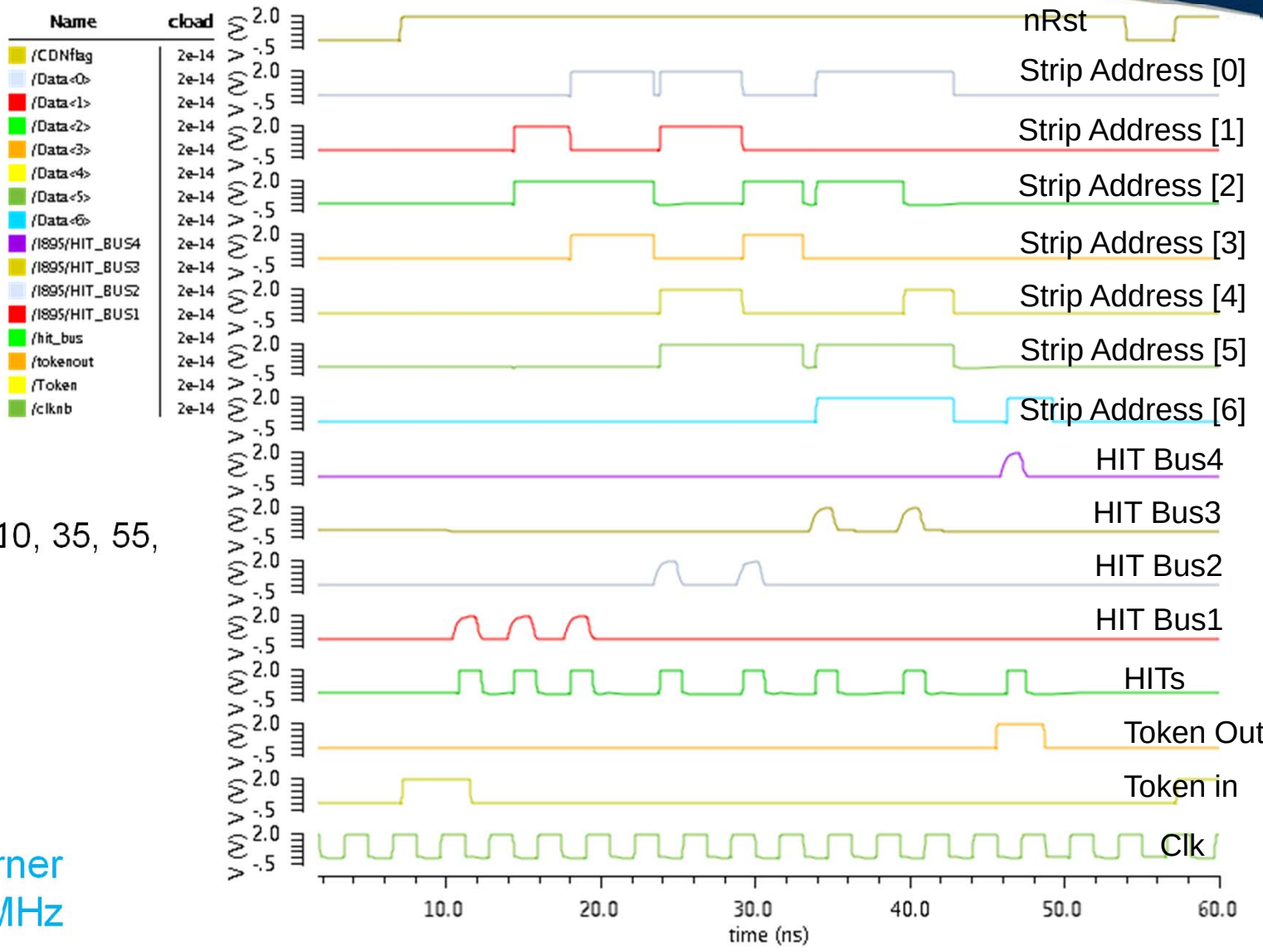
Simulation of one HIT finder block (STRIP Encoding)



Strips hit: 8
Locations: 1, 5, 10, 35, 55, 71, 95, 128

Temp=27C
Nominal corner
Clock=320MHz

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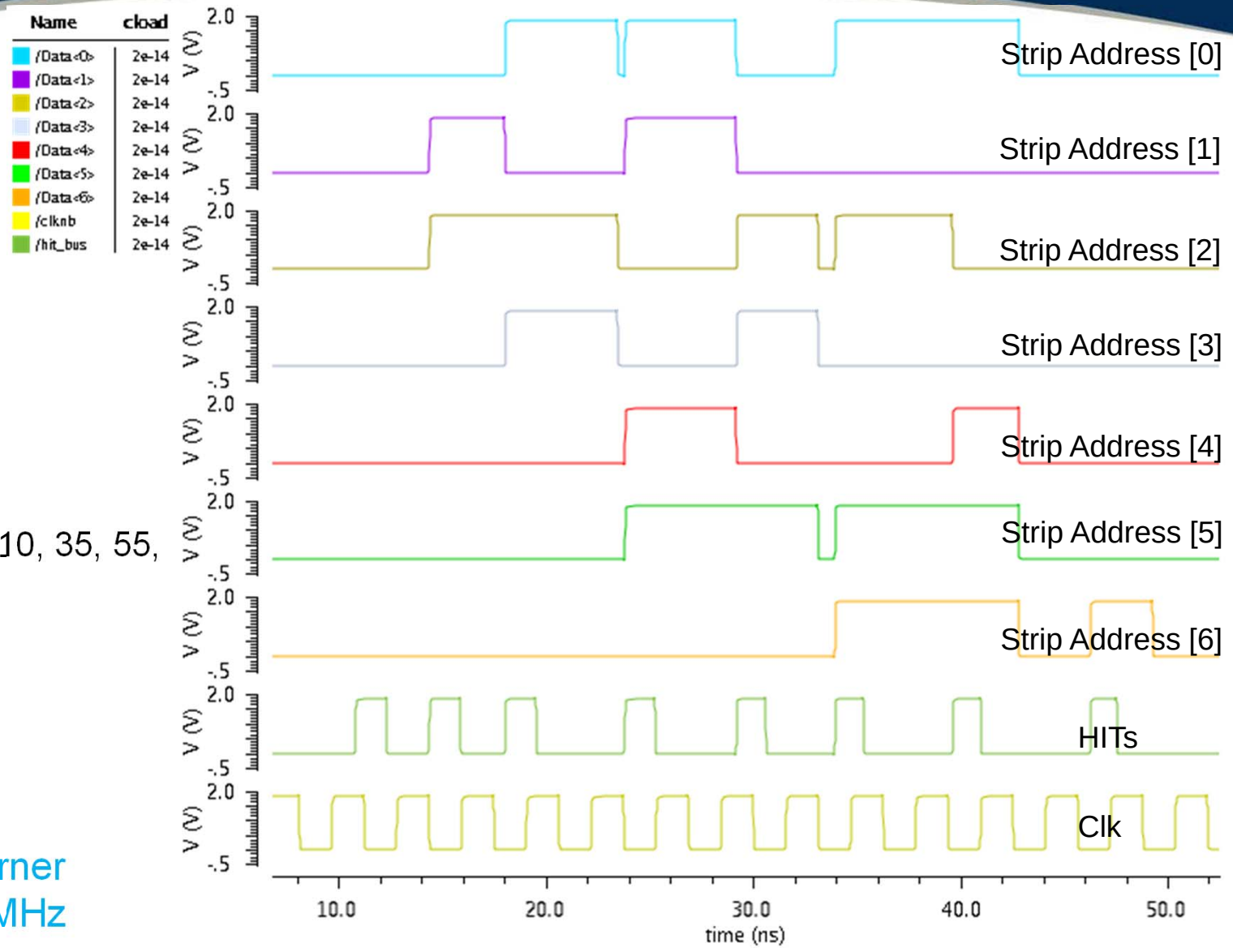
Simulation of strip encoding
Strip Address



Strips hit: 8
Locations: 1, 5, 10, 35, 55, 71, 95, 128

Temp=27C
Nominal corner
Clock=320MHz

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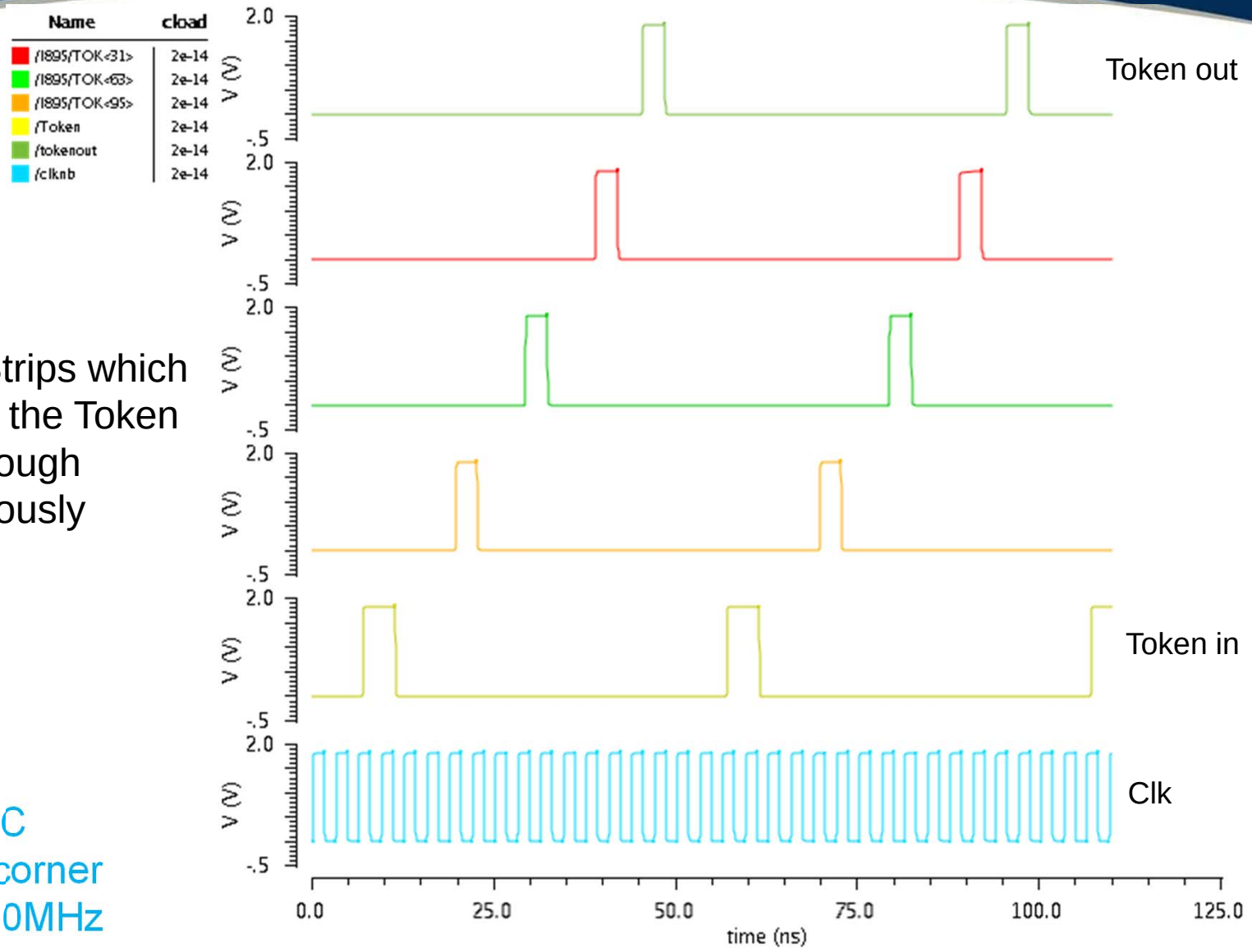
Simulation of strip encoding Tokens



Between Strips which are not hit, the Token passes through asynchronously

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Nominal corner
Clock=320MHz

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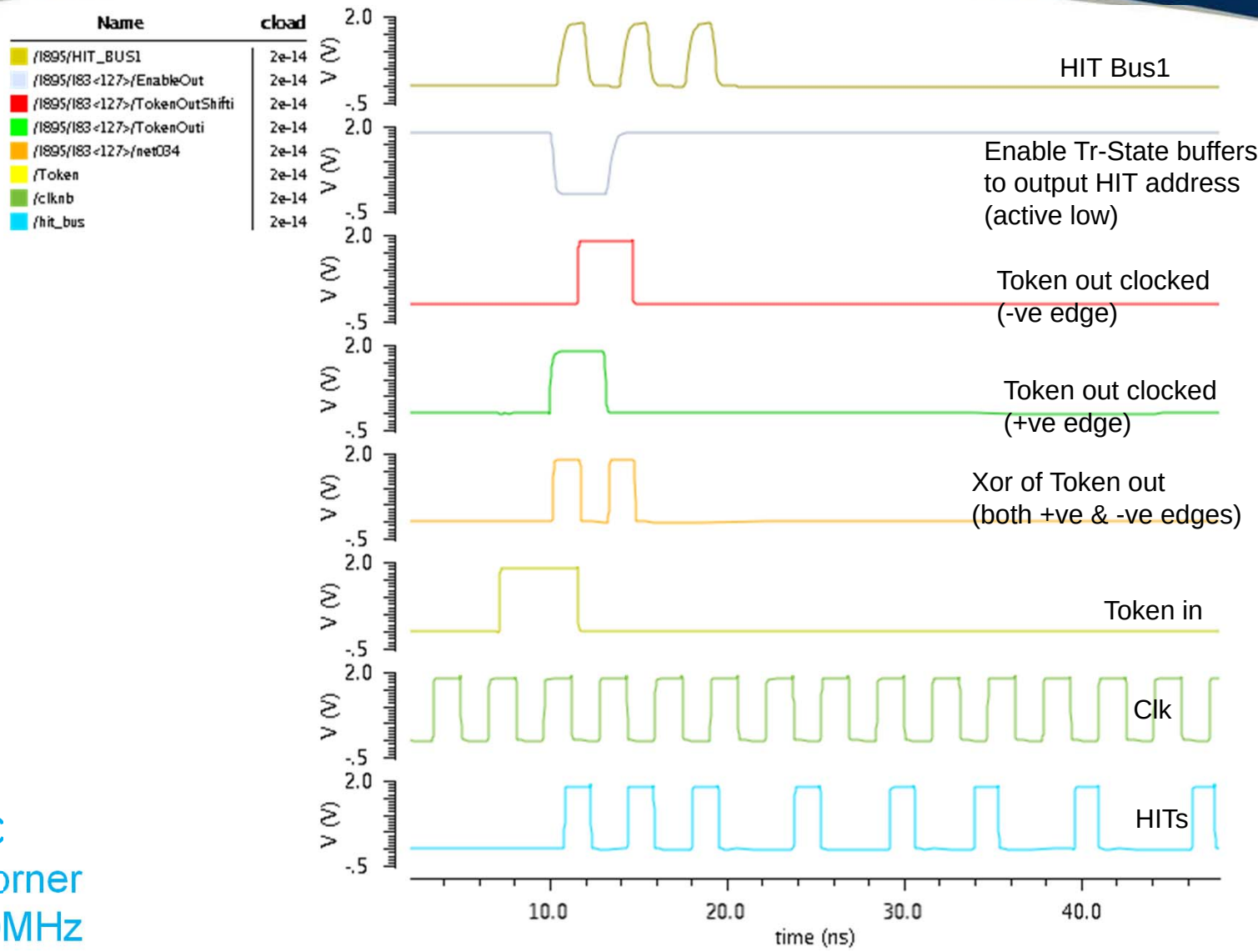
Simulation of strip encoding 1st Hit RO Cell Signals



Temp=27C
Nominal corner
Clock=320MHz

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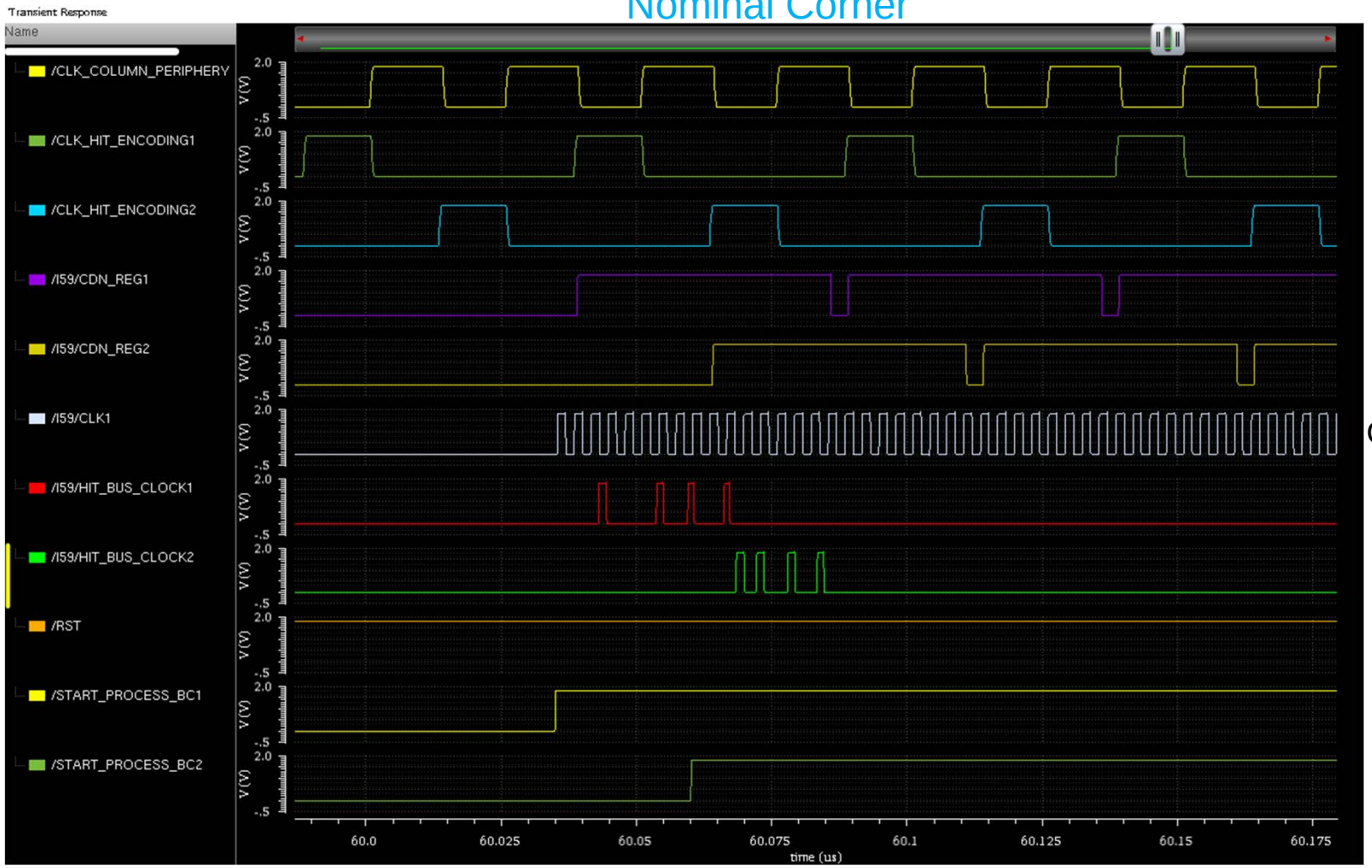
Simulation of complete STRIP Encoding Block

Temp=27C
Nominal Corner



Clk (40MHz)

Clk (320MHz)

HITs BX1

HITs BX2

We simulate 4 hits per bunch crossing (BX) and all 8 hits detected

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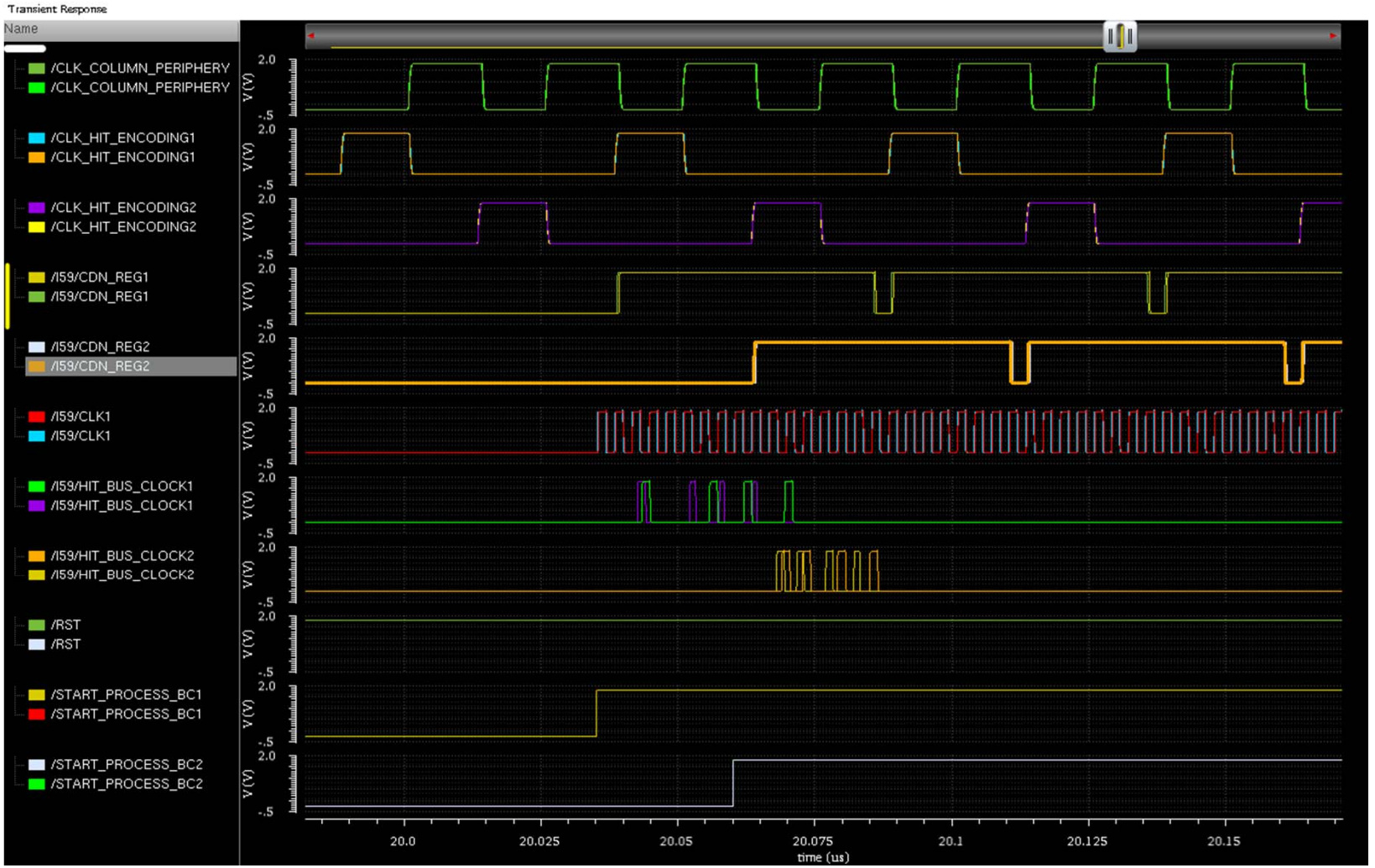
Simulation of complete STRIP Encoding Block

Temp=27C
SLOW and FAST corners



Clk (40MHz)

Clk (320MHz)

HITs BX1

HITs BX2

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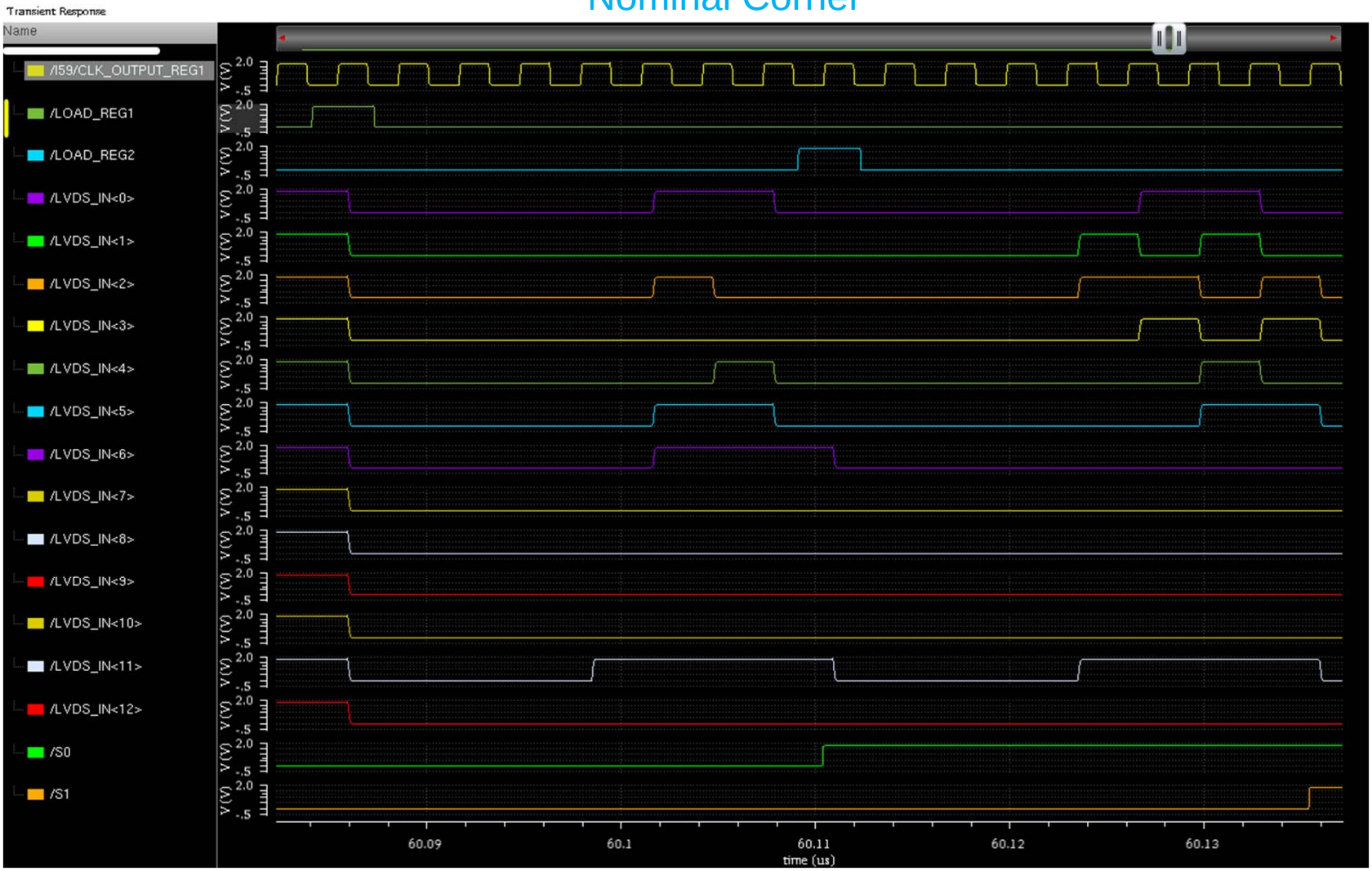
Simulation of complete STRIP Encoding Block (LVDS i/p)

Temp=27C
Nominal Corner



Clk (320MHz)

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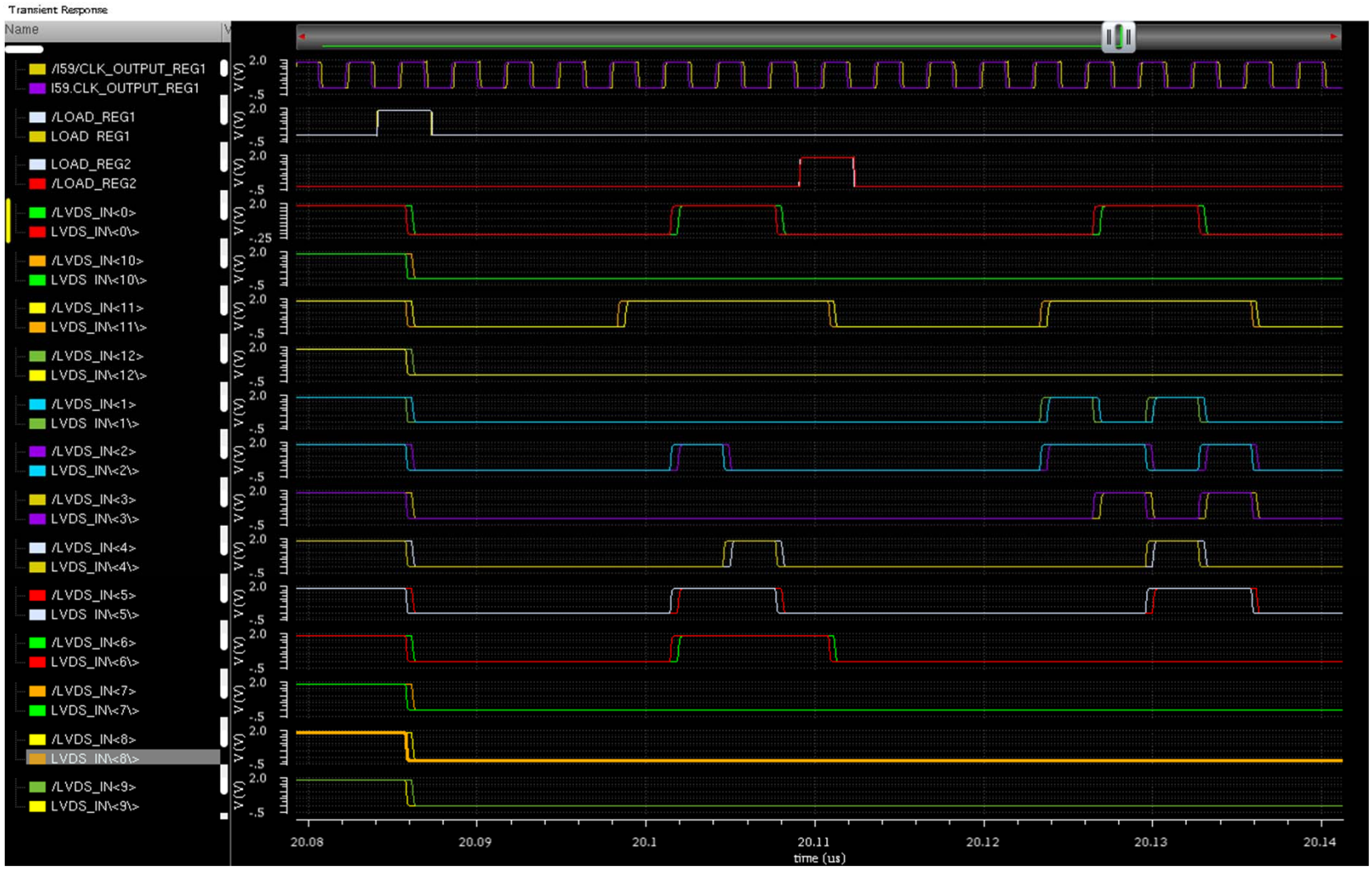
Simulation of complete STRIP Encoding Block (LVDS i/p)

Temp=27C
SLOW and FAST corners



Clk (320MHz)