INTRO & OVERVIEW

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HR-CHESS2 technical specifications summary

Close to HV-CHESS2 spec (Physics requirements!)
Specifications below for one block:

Technology: *TowerJazz 180 nm*
Voltage supply: 1.8V
Wafers: Epitaxial
Epi resistivity/thickness: up to 25um >1kOhmcm* (MIP: 2000e-)
Segment size: 40um x 800um (Segments could contain smaller pixels*)
Number of strips: 128
Number of segments per strip: 32
Readout speed ≥ 320 Mbit/sec
Output buffers: LVDS with adjustable bias current and CM level
Maximum number of hits per strip: 1 + overflow flag
Maximum number of hits in block: 8
Size of data output per strip: 13 bits
Format of data output: 5-bits (segment) + 1-bit (segment overflow flag) + 7-bits (strip address)

* pending results from OVERMOS1

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HR-CHESS2 technical specifications summary (cont.)

Coupling: AC

Charge collection time: < 10ns

Noise: 60e- for sensor capacitance of 50fF

Power(analogue): 23μW/channel(pixel[1])+33μW/channel(periphery[2])=56μW/channel

Power(digital): 5μW/channel

Power total: 250mW (ARRAY)+187mW (LVDS)=437mW (Current best estimate[3])

Power supply: 1.8V

Gain: 100μV/e- (0.63mV/fC) at comparator input

$T_{peaking}$: < 10ns at comparator input

Time-walk: <10ns for 0.8fC and 0.08fC signals with comp. threshold at 0.044fC

Overload recovery: normal response within ~2μs after 0.8pC signal

[1]Pixel contains pre-amplifier and diode bias circuitry
[2]Periphery contains Discriminator, Trim DAC, & a Voltage Buffer
[3]Simulated schematic only, not layout, doesn't include PLL, SPI, & Bias; effect of leakage current predicted to be negligible; current best estimate of power density is 0.34W/cm^2

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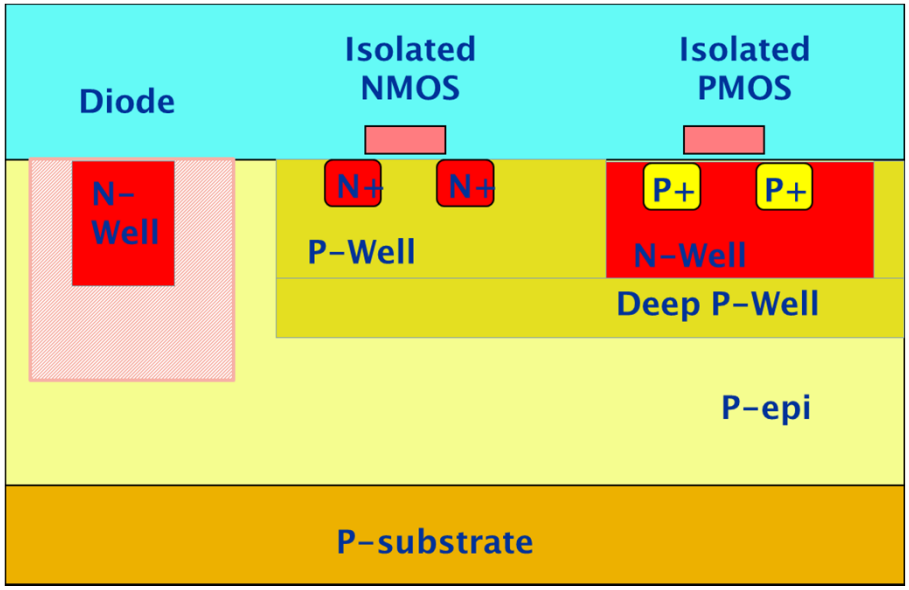
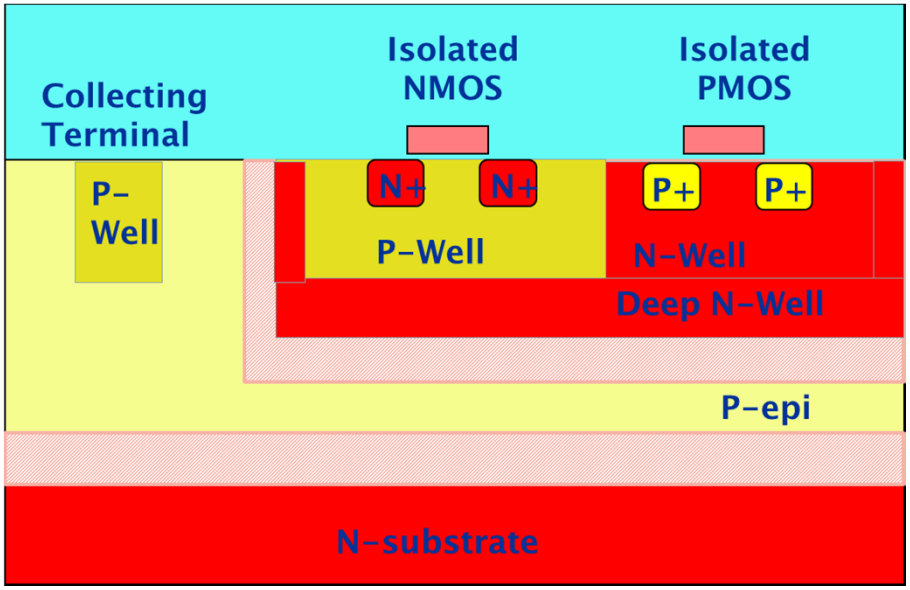
Available wafer types

P on P
aka P epi on P substrate



Conventional
Depletion starting from collecting N-well

P on N
aka P epi on N substrate



New
Depletion starting from deep N-well and N substrate

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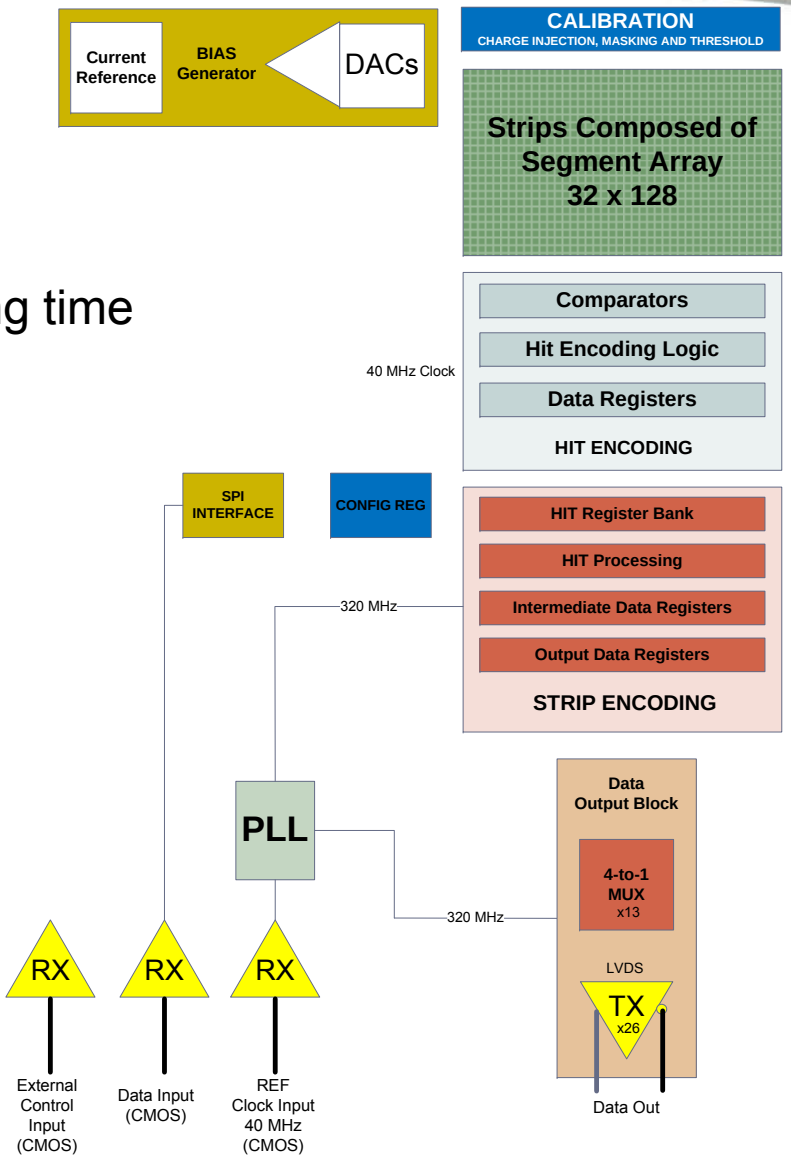
HR-CHESS2 chip

Main Functional Blocks:

- Fast Pre-Amplifier <10ns peaking time
- Comparator with threshold trim
- HIT Encoding
- Strip Encoding
- Data Output Block
- Calibration
- PLL
- LVDS TX/RX
- Programmable Bias
- SPI Interface



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Segment array details and chip area estimation

No. of Strips: 128
32 segments arranged in 128 strips. Each segment may contain multiple pixels

Segment: 40μm x 800μm

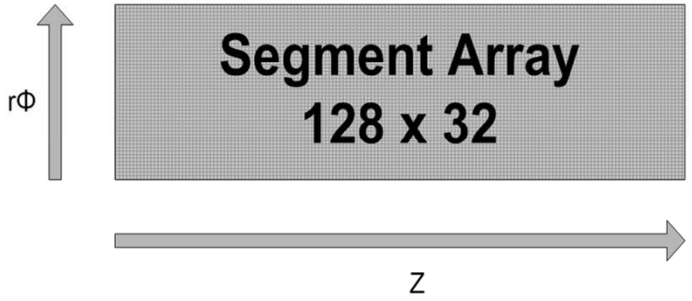
No. of segments in Z direction: 32

No. of strips in rΦ direction: 128

No. of bits per segment:
M (rΦ position) = 7
N (Z position) = 5
Flag/Overflow = 1
Total = 13

Max. Chip area limited by reticle size: 23.5mm x 31.5mm

Size of sensing area: 5.12 mm x 25.6 mm
Add 2mm in Z direction for periphery



Read 8 hits for 128 strips
Each hit contains 13 bits
8 hits contain 13 x 8 = 104 bits