COMPARATOR

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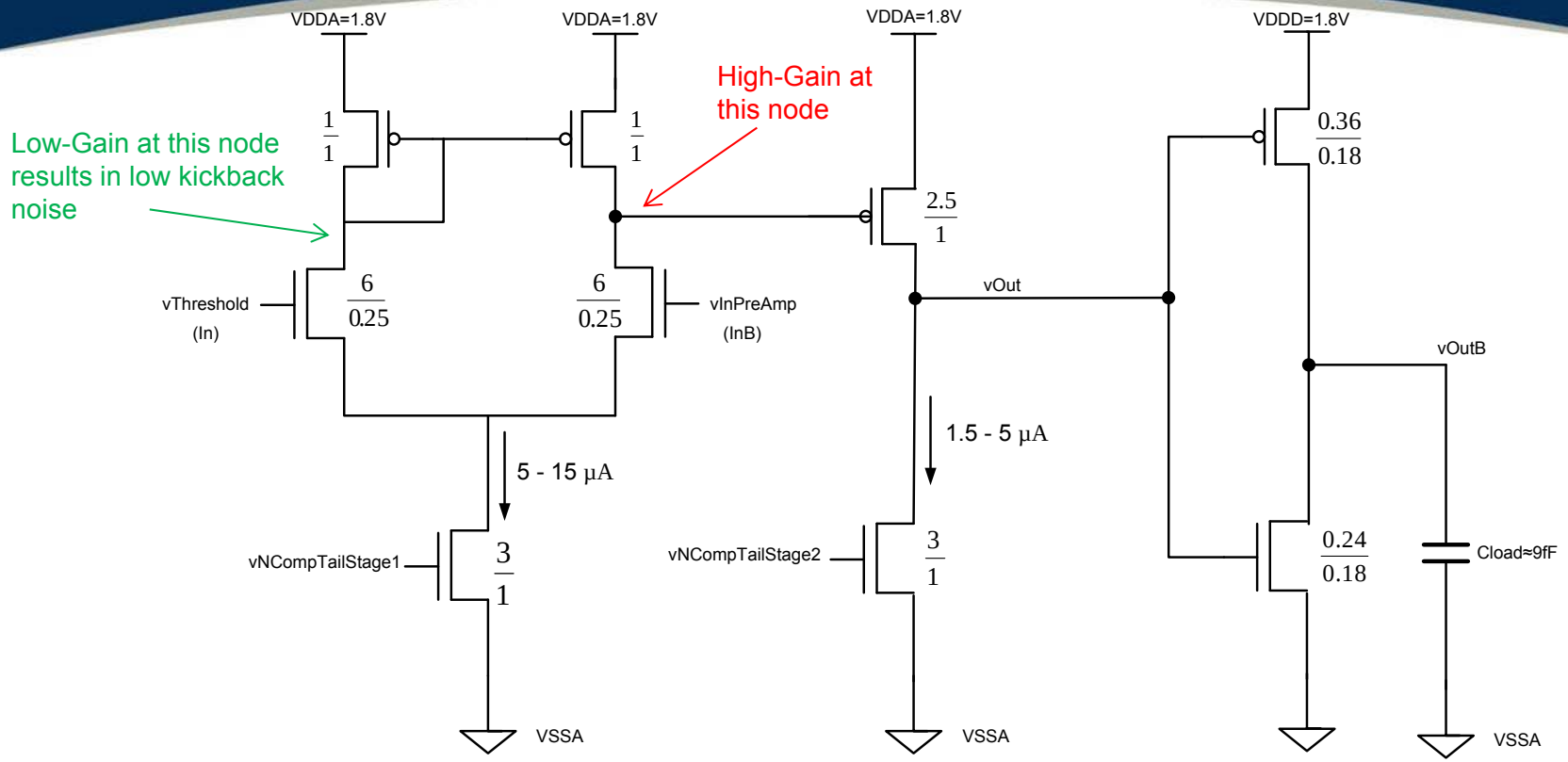
Comparator schematic



- 3 stage open loop comparator design; modified PIMMS comparator
- 3rd stage was changed to a minimum-sized inverter for small propagation delay
- Added gain of 3rd stage increases resolution and reduces propagation delay
- Variable tail bias of the first two stages adds flexibility
- 3rd stage powered from digital supply & only draws power when switching; time-walk performance can be further improved at the expense of more power!

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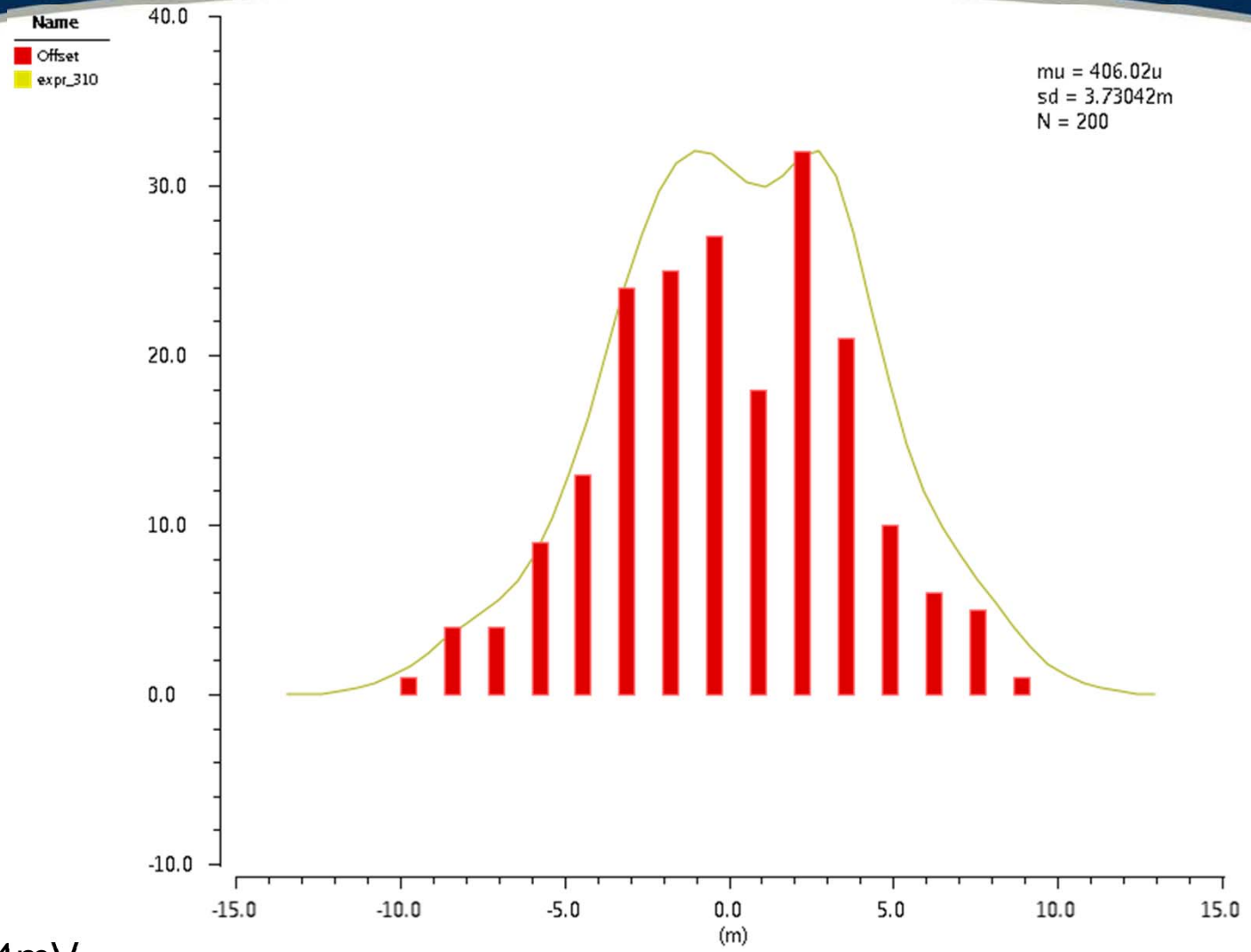
Comparator offset histogram



±3σ = 22.4mV

iTailStage1=15μA; iTailStage2=6μA;Temp=27°C

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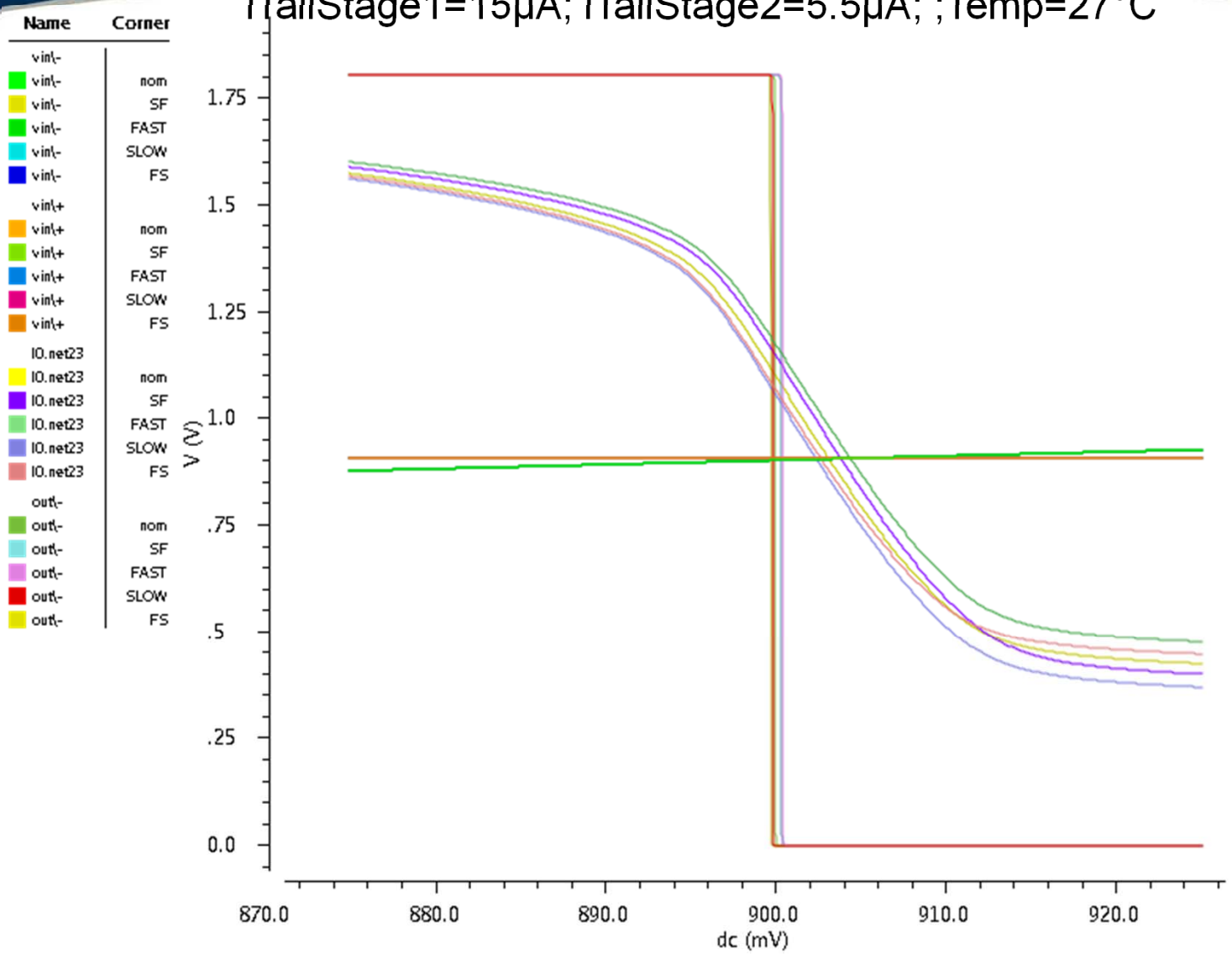
DC Transfer curves of comparator at different corners

iTailStage1=15µA; iTailStage2=5.5µA; ;Temp=27°C



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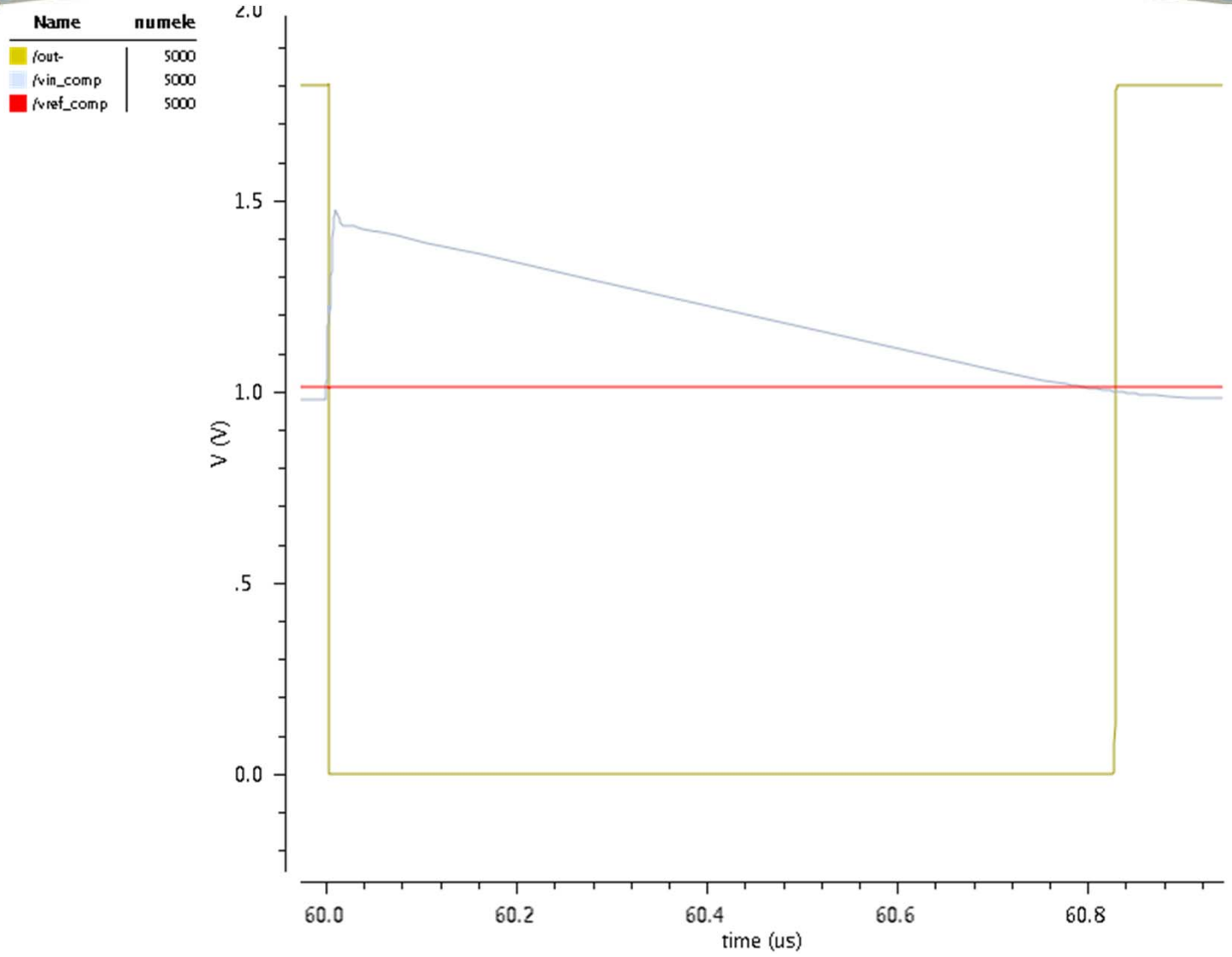
Comparator Transient Simulation @ Temp = 27°C



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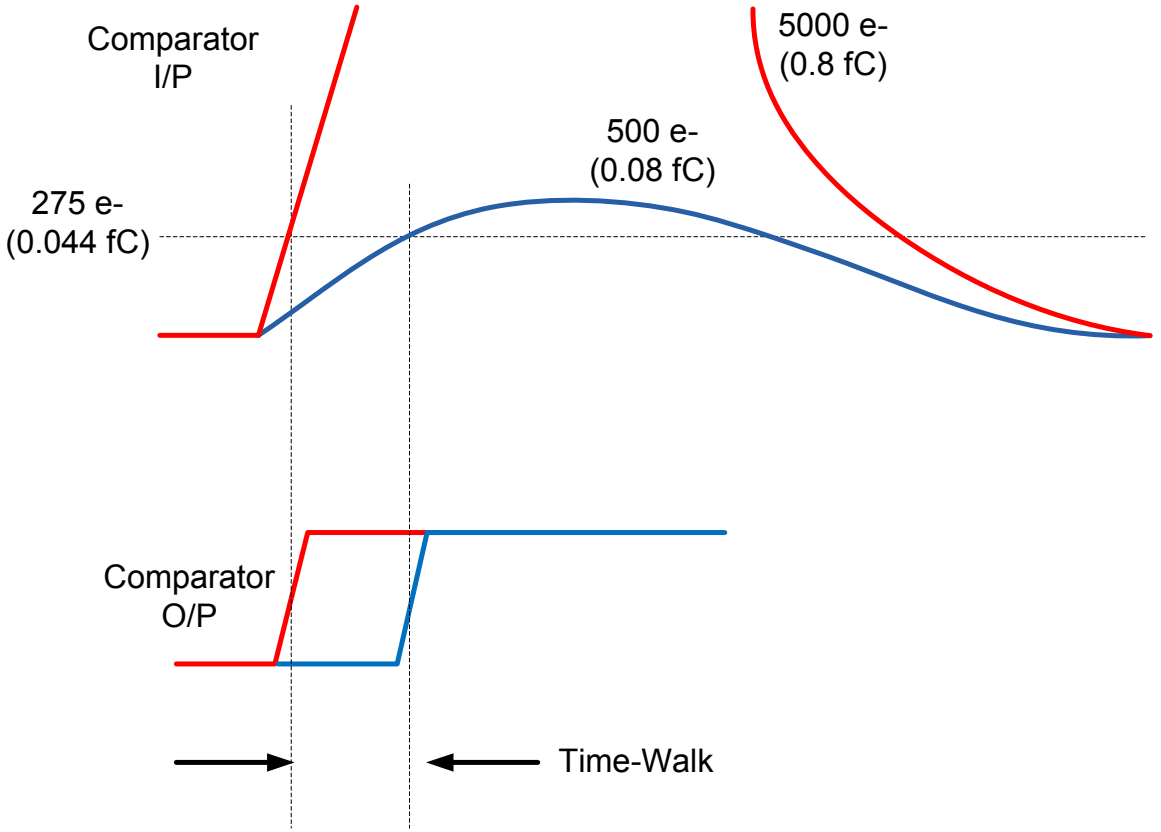
Time-walk specification



Dependence of comparator fire time on signal must be < 1 BX i.e. 25ns

Expected ≤ 16 ns time difference between comparator leading edges for input signal of size 500 e- and 5000 e- with a threshold/vRef set at 275 e-

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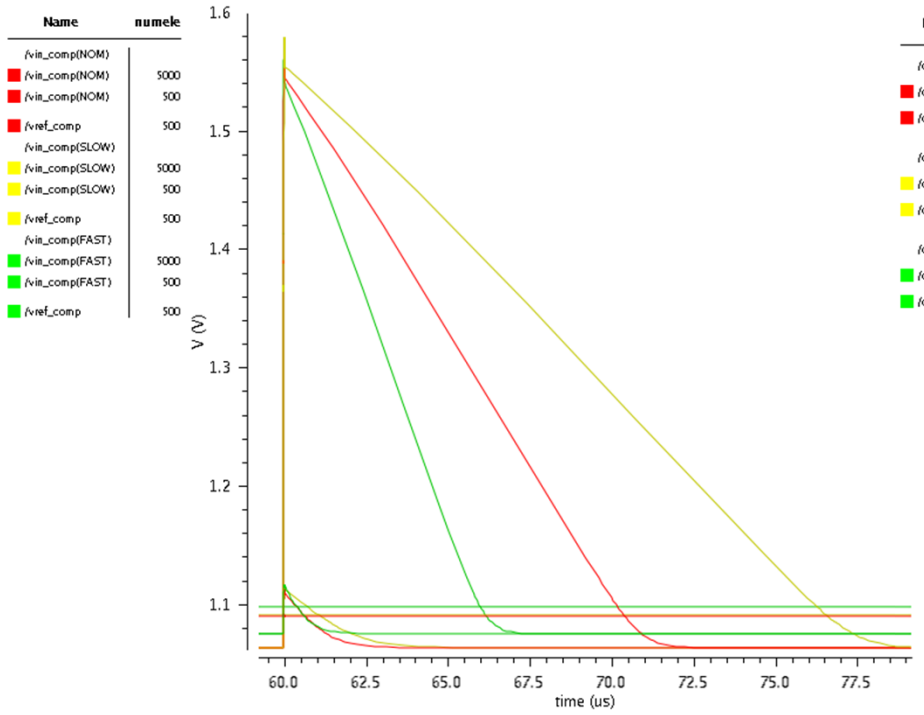
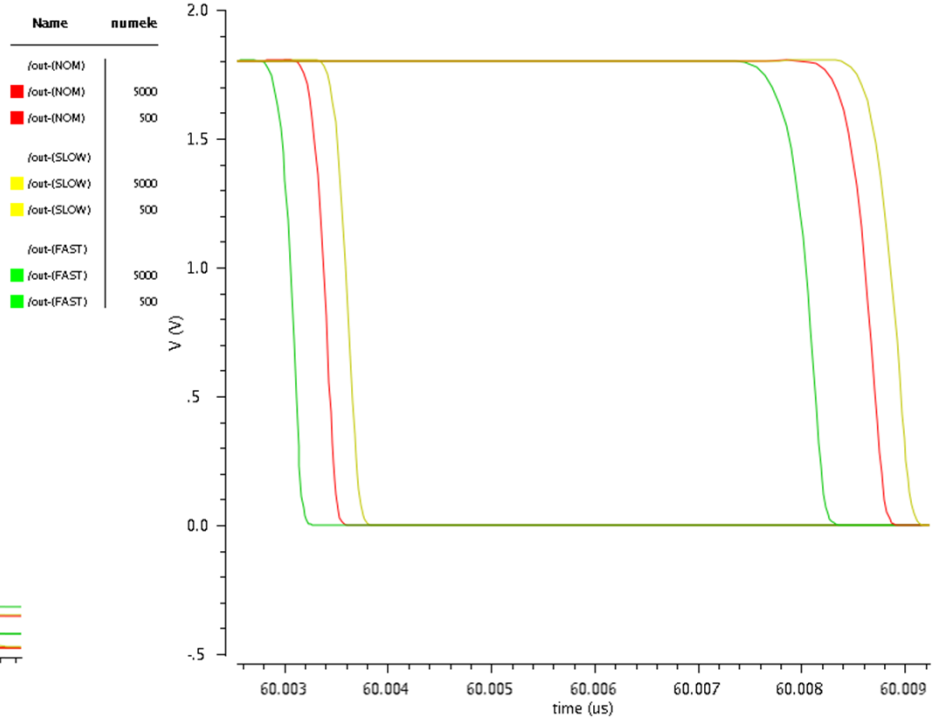
Time-walk simulation
Temp = -40°C & 1ns CC time



Comparator Input



Comparator Output

All process corners simulated; threshold adjusted for each process corner (small differences); temperature varied from +40°C to -40°C

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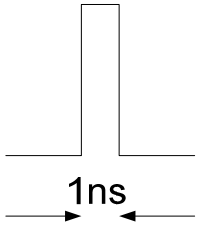
Time-walk simulations

Threshold adjusted for each process corner (small differences)

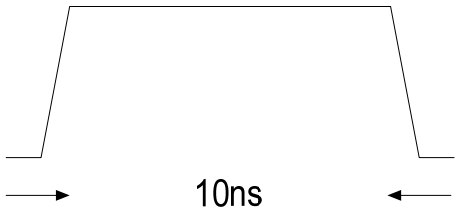
Time-Walk (~1ns charge collection time)

	NOM	FAST	SLOW
+40°C	5.277ns	4.53ns	5.07ns
-40°C	5.237ns	4.984ns	5.26ns



Time-Walk (~10ns charge collection time)

	NOM	FAST	SLOW
+40°C	7.95ns	7.63ns	7.66ns
-40°C	8.34ns	8.1ns	8.15ns



- Meets specification in all corners
- Time-walk can be reduced at the expense of more power!