



Science & Technology Facilities Council

Technology

ATLAS Strip CMOS HR-CHESS2
Initial Design Review

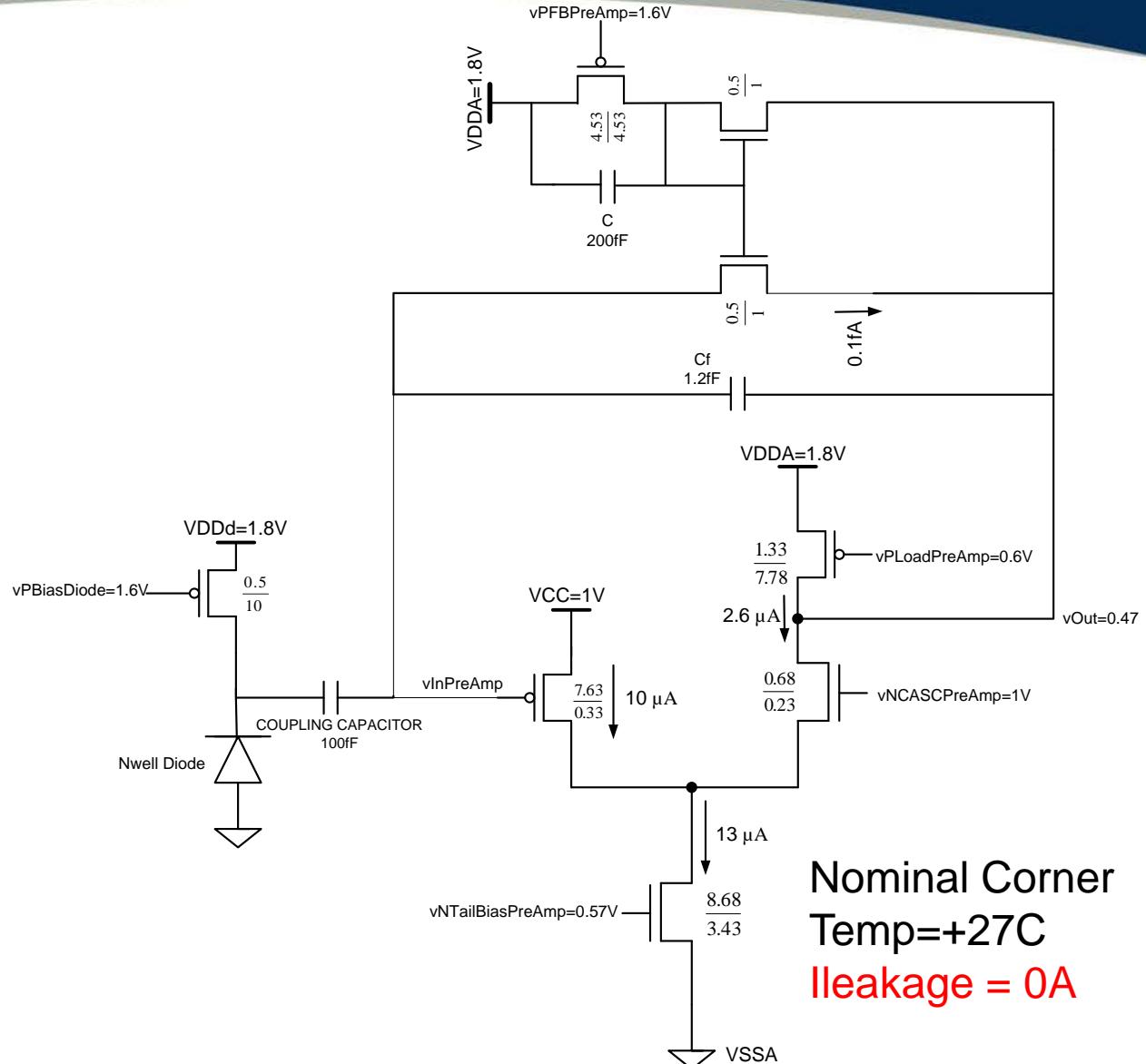
Pre-amplifier

D. Das, STFC-RAL, UK
29/10/15



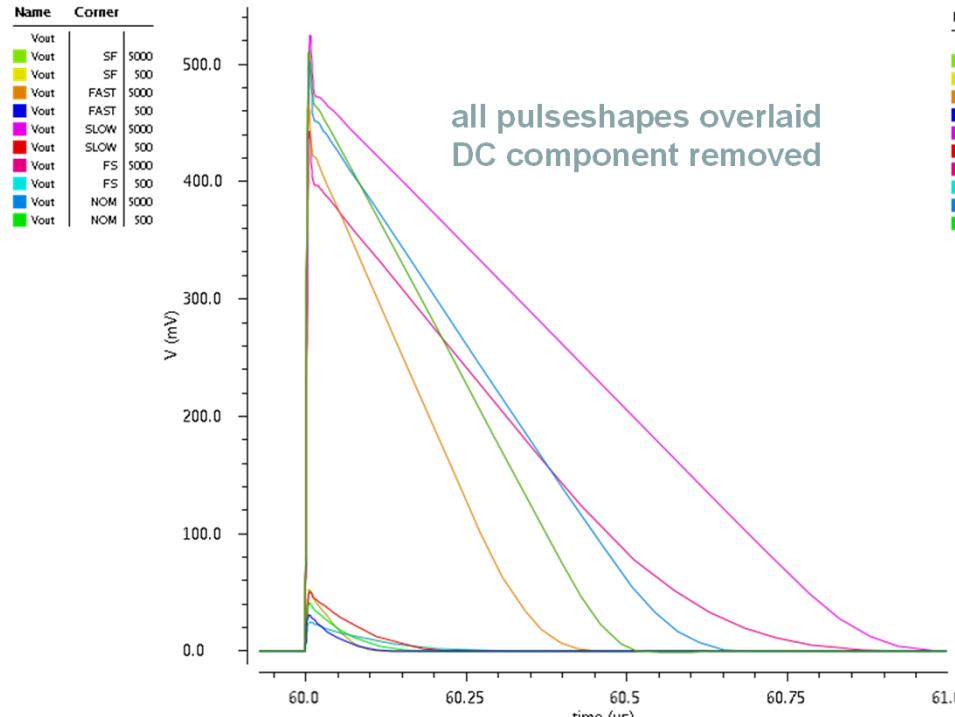
Pre-amplifier schematic

Parameter	Voltage
VDDA	1.8V
VSSA	0V
VCC	1V
VDDd	1.8V
vPBiasDiode	1.6V
vNCASCPreamp	1V
vPFBPreAmp	1.6V
vPLoadPreAmp	0.6V
vNTailBiasPreAmp	0.57V

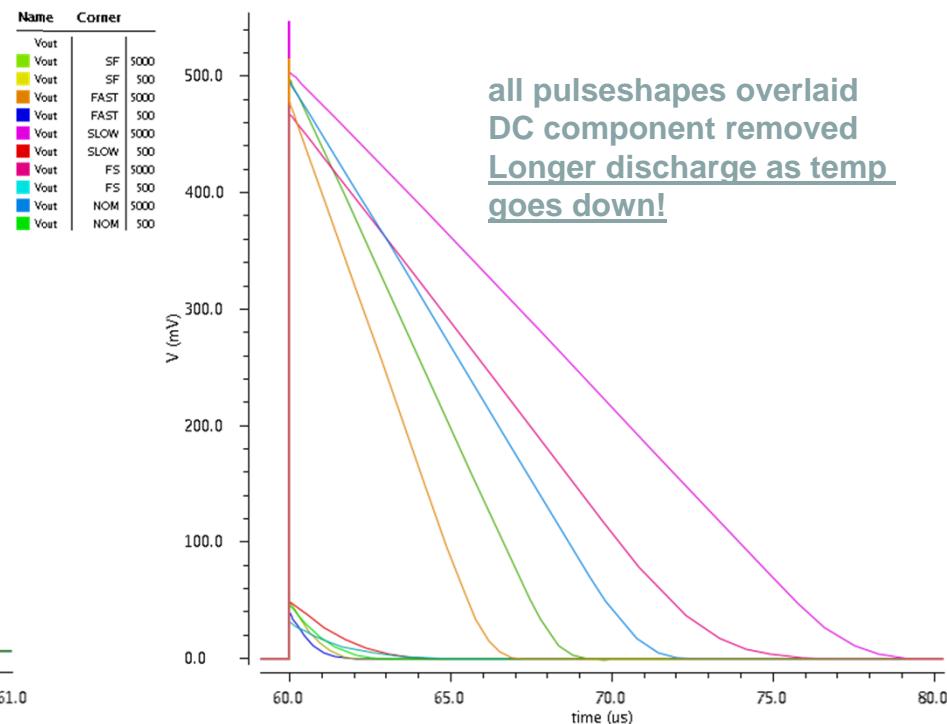




Pre-amplifier performance



$T = +40^\circ$

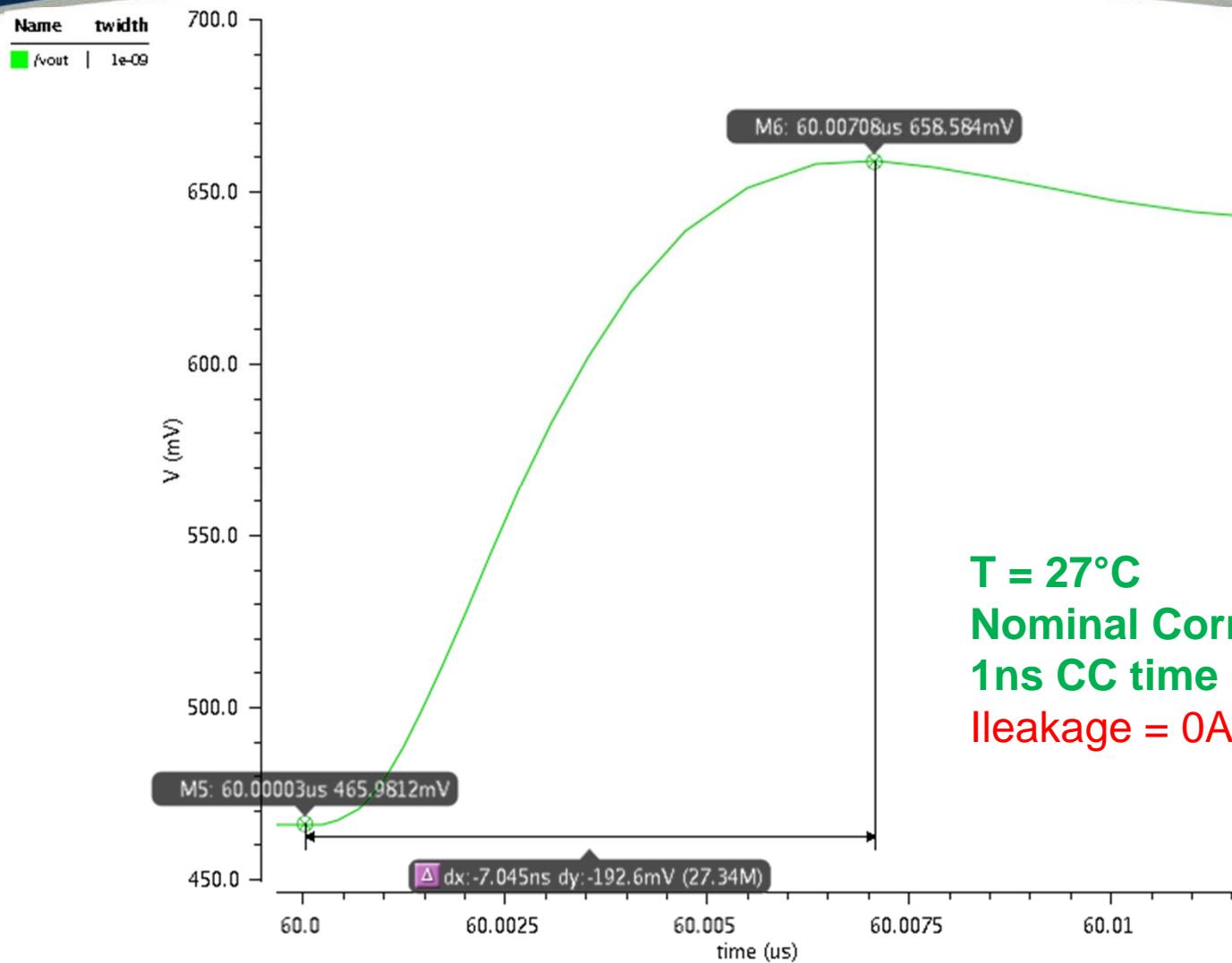


$T = -40^\circ$

- Signal at Pre-Amp output from 500e- to 5Ke- in 2 steps
- All process corners
- Ileakage = 0A



Tpeaking @ 2Ke- (from baseline up to peak)

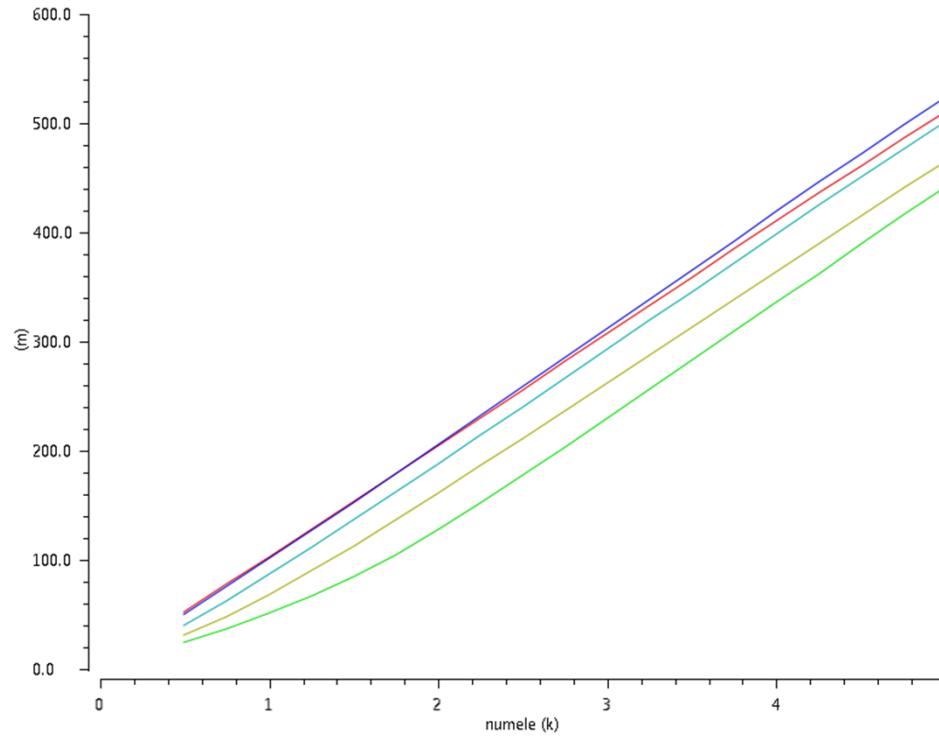


T = 27°C
Nominal Corner
1ns CC time
Ileakage = 0A

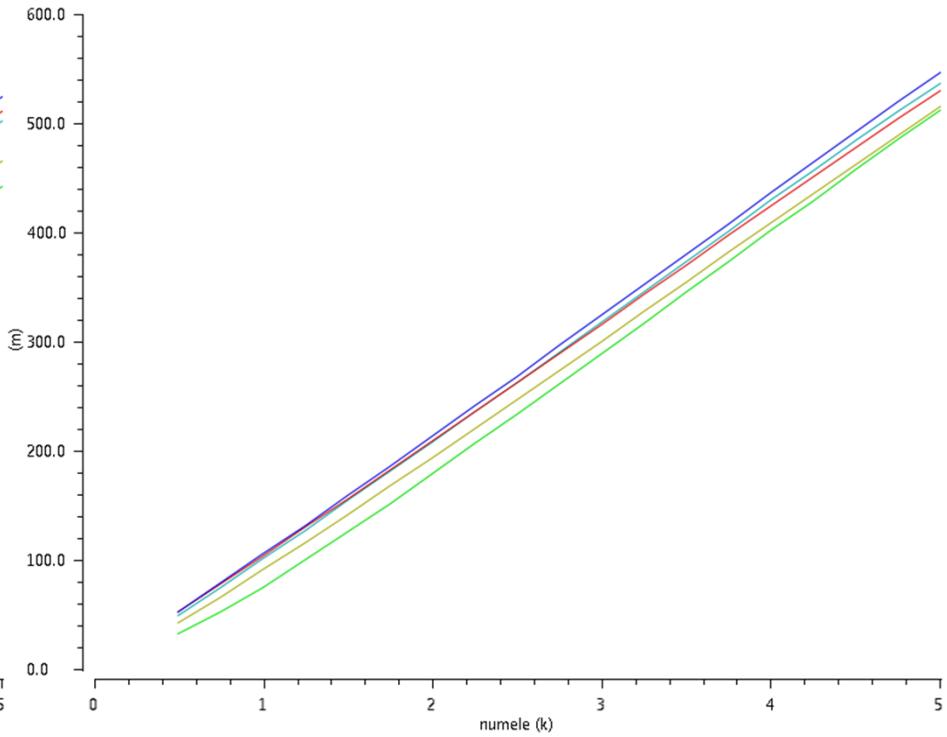
Tpeaking generally a few ns longer than Trise (10% to 90%)



Output pulse amplitude ΔV vs signal



T = +40°

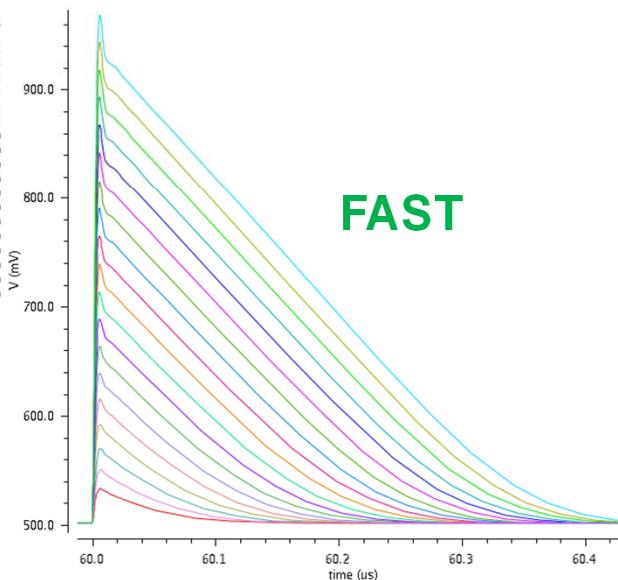
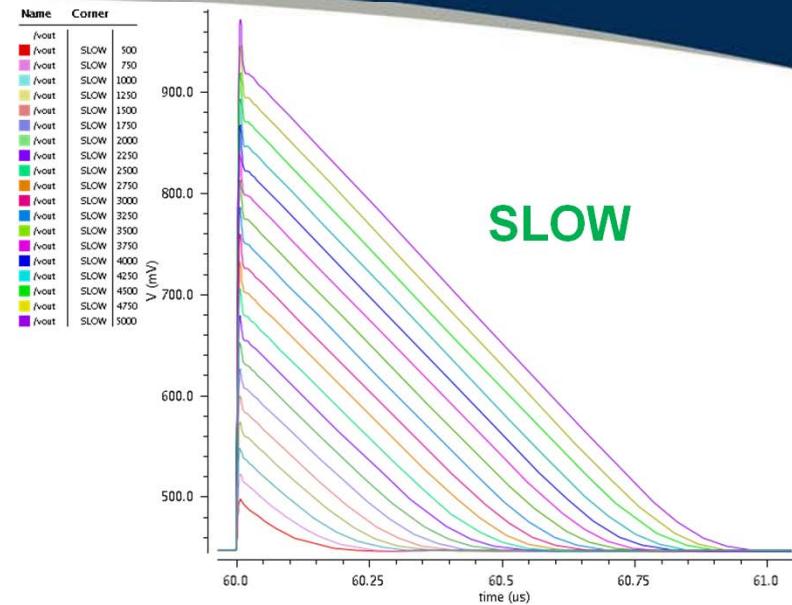
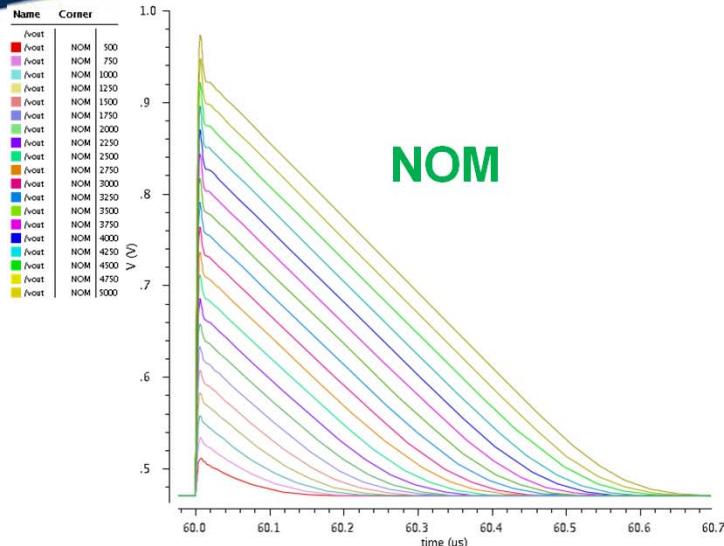


T = -40°

- Difference between peak and baseline voltage from 500e- to 5Ke- in 250e- steps
- All process corners (NOM, FAST, SLOW, SF, FS)
- *No significant change in gain except some non-linearity in FS corner at low e-*



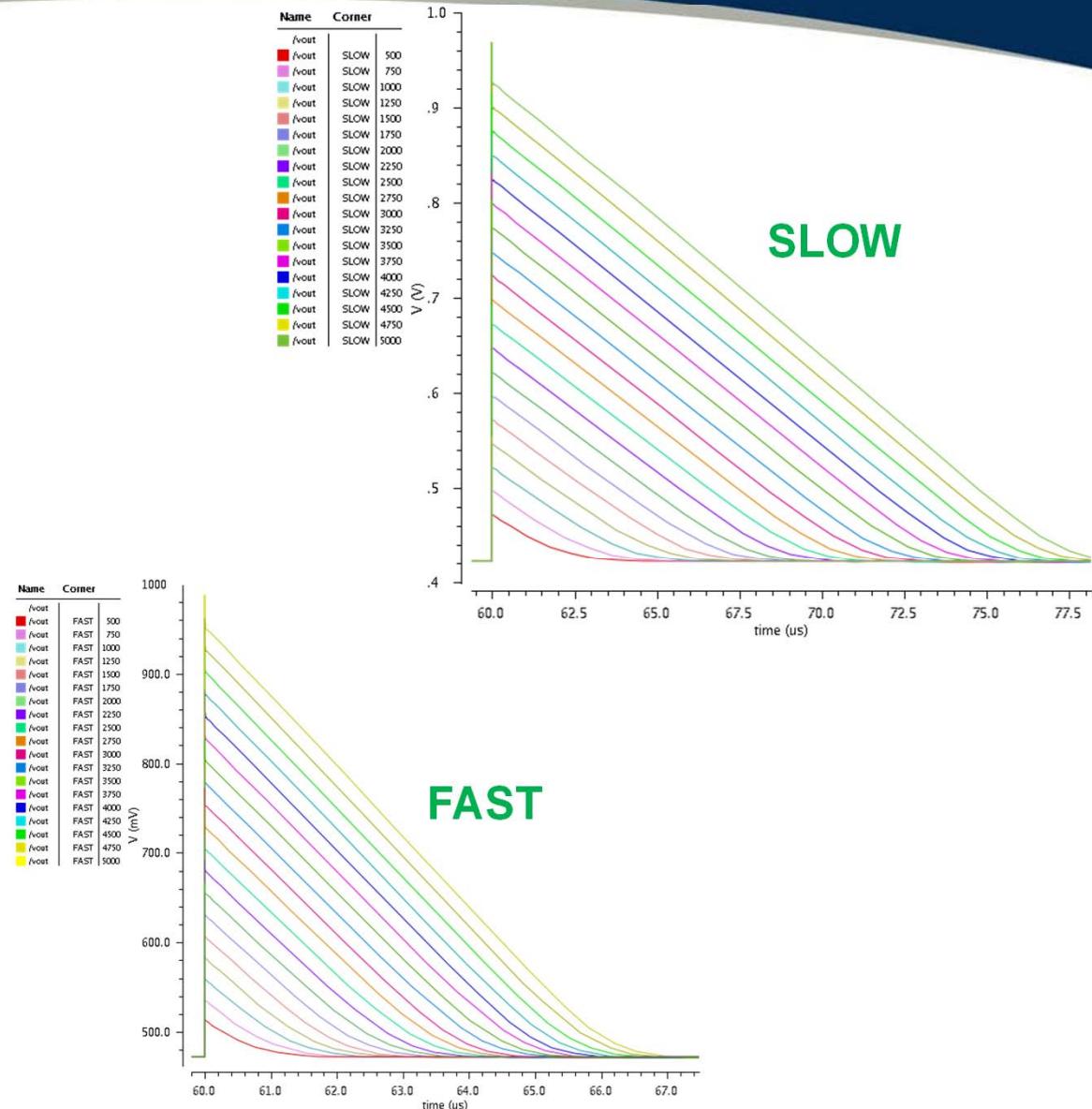
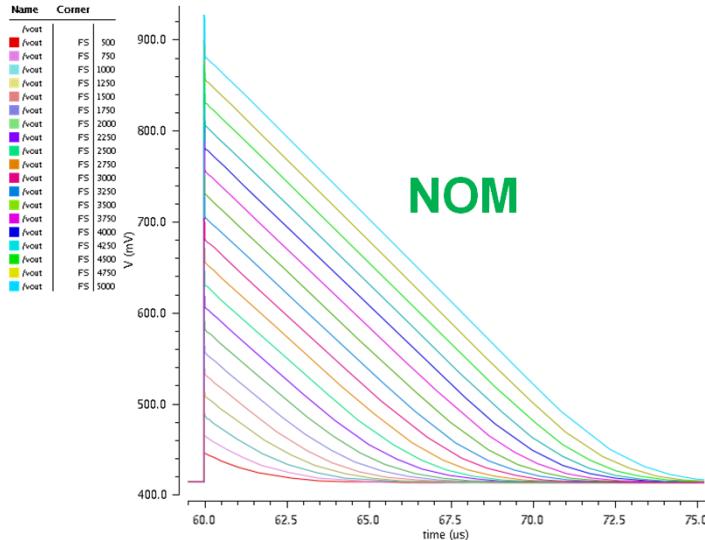
Output pulse shapes vs signal Temp = +40°



Signal at Pre-Amp output from 500e- to 5Ke- in 250e- steps
Ileakage = 0A



Output pulse shapes vs signal Temp = -40°



Signal at Pre-Amp output from 500e- to 5Ke- in 250e- steps
Ileakage = 0A



Pre-amplifier spec. summary

T = +40°
Ileakage = 0A

	NOM	FAST	SLOW
CG [μ V/e]	102	97	105
Tpeaking [ns] (500e-) (input of comp.)	9	7.9	9.6
Noise [e-] (50fF det. cap)	48	41	61
*Phase Margin [°]	115	103	103
Gain Margin [dB]	43	45	41
A_{OL} [dB]	52	49	55
Power [μ W]	19.2	22.9	15.9

T = -40°
Ileakage = 0A

	NOM	FAST	SLOW
CG [μ V/e]	107	105	110
Tpeaking [ns] (500e-) (input of comp.)	7.6	6.8	8.9
Noise [e-] (50fF det. cap)	50	42	56
*Phase Margin [°]	93	123	81
Gain Margin [dB]	36	38	35
A_{OL} [dB]	61	59	63
Power [μ W]	16.2	20	13.1

*Phase margin of $>90^\circ$ is big enough not to find any form of gain peaking or oscillation