HIT ENCODING

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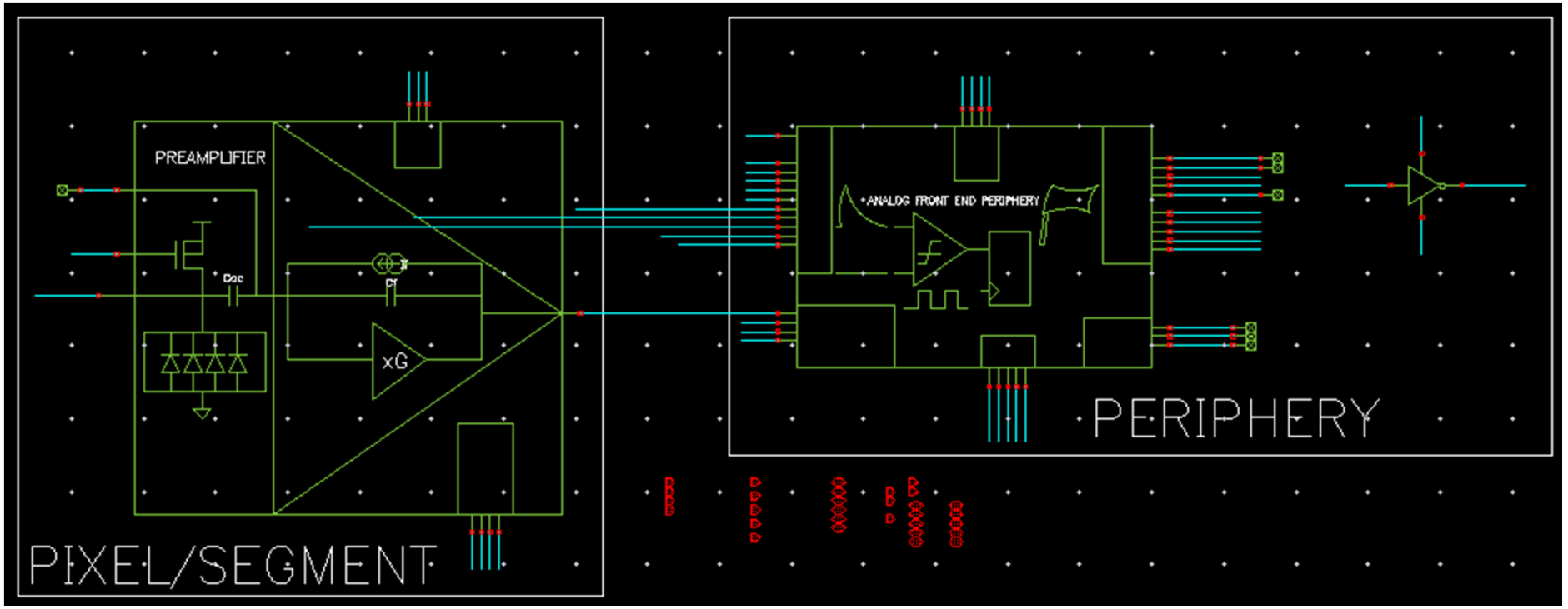
Front-end implementation



1 column of front-end circuitry
Pixel contains 32 pre-amps
Periphery contains 32 Discriminators + 32 HIT Encoding Blocks

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HIT encoding principle (Same as HV-CHESS2)

Hit	HitNext	nEncode	Flag
0	0	1	0
0	0	1	0
0	0	1	0
0	0	1	0
1	0	0	0
0	1	1	0
0	1	1	0
0	1	1	0
1	1	1	1
1	1	1	1
0	1	1	1

Logic functions:

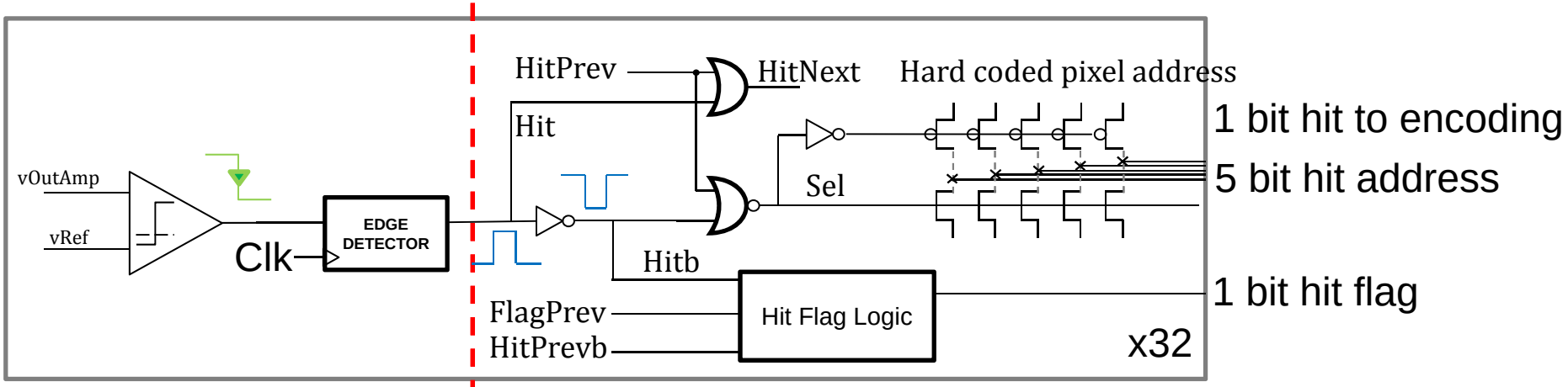
HitNext = $(HitNext_{-1}\ OR\ Hit)$

Encoded = $(\overline{Hit}\ OR\ HitNext_{-1})$

Flag = $Flag_{-1} OR\ (\overline{HitNext_{-1}} NOR\ \overline{Hit})$

The *Encoded* signal controls sending the segment/pixel address (5-bits) to the periphery along with the Flag if it's raised.

HIT encoding logic conceptual block diagram



Edge detector latching on the leading (falling) edge of the comparator

Hit encoding

Hit address GRAY coded!

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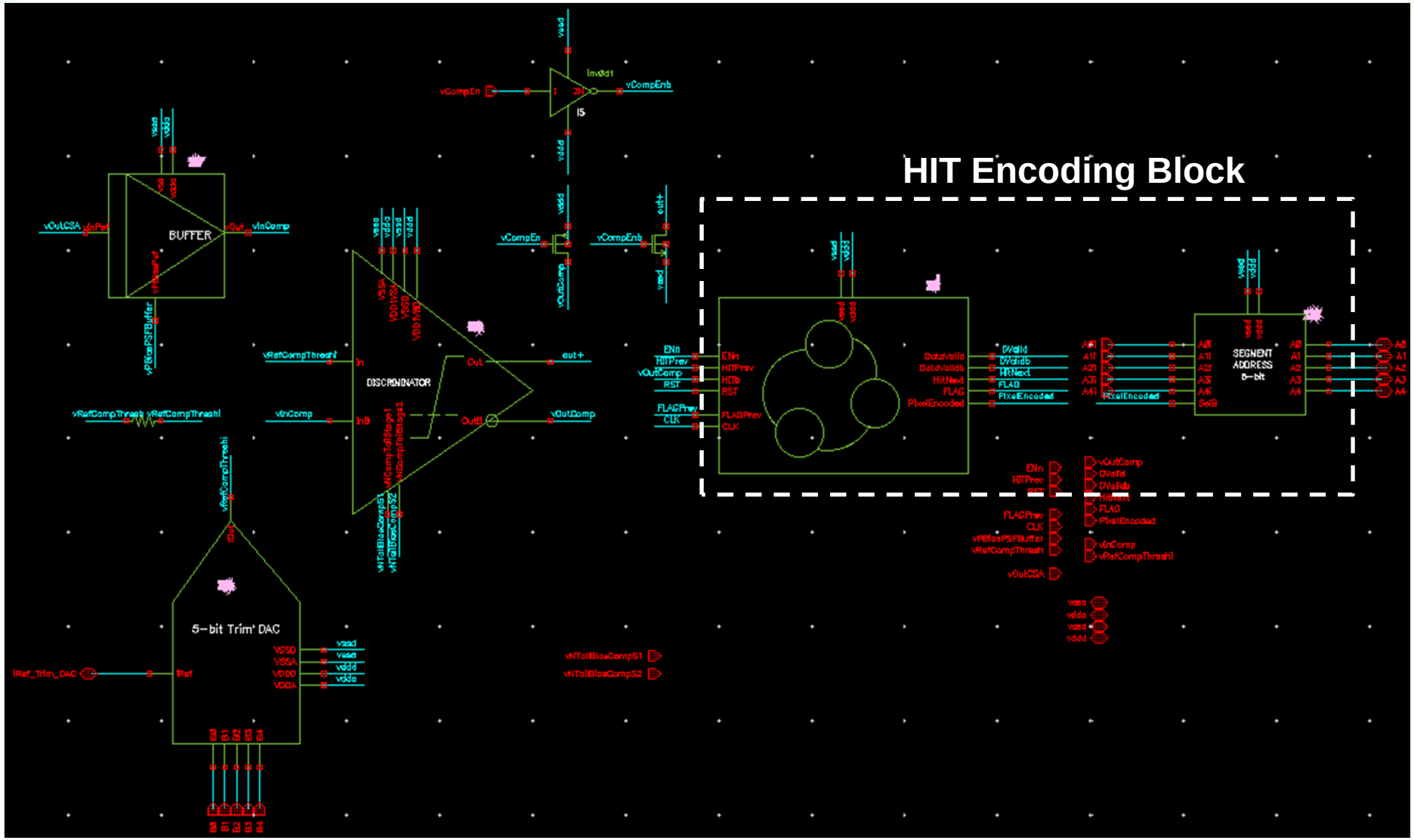
Column Periphery Implementation



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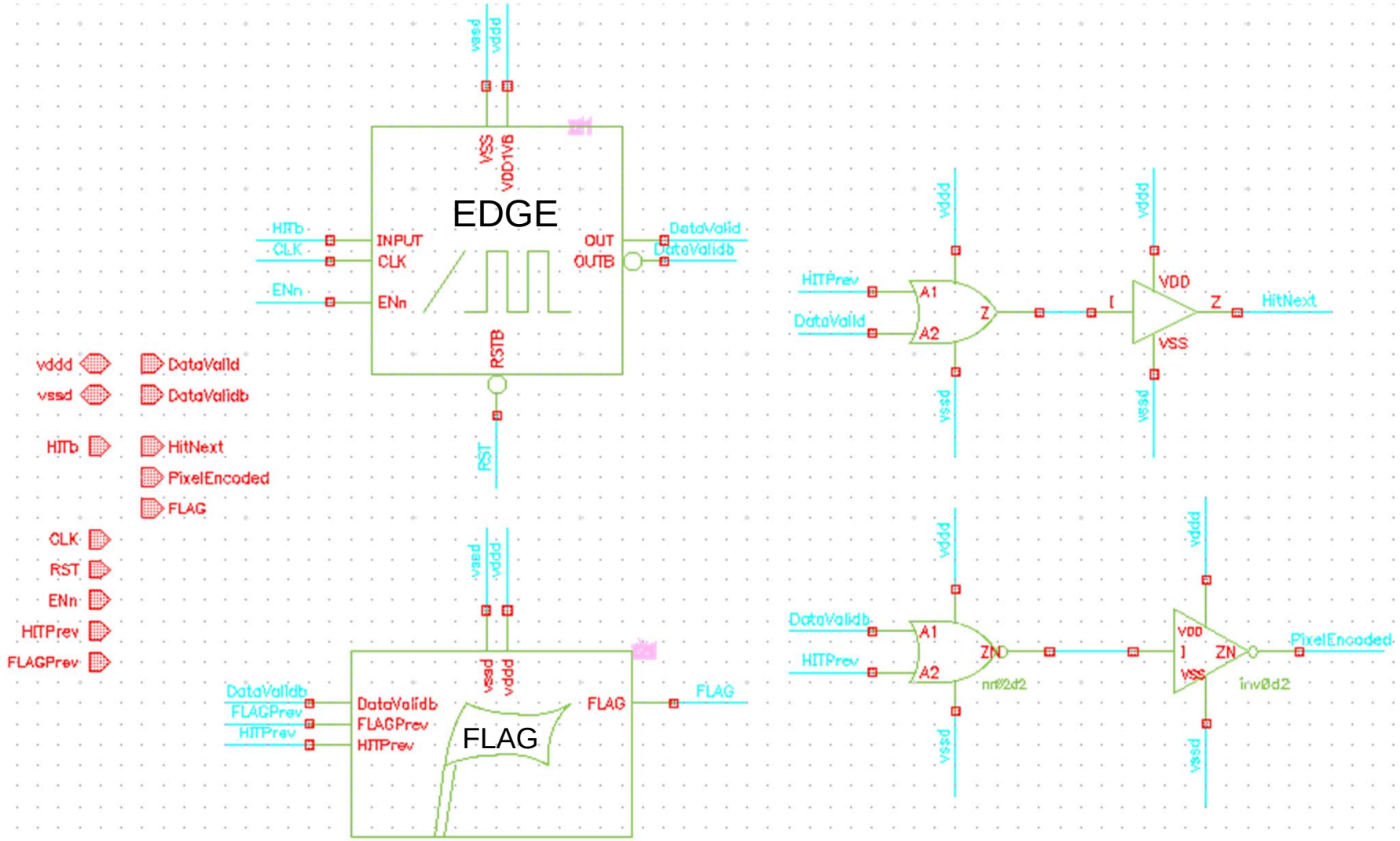
HIT detect and encoding logic implementation



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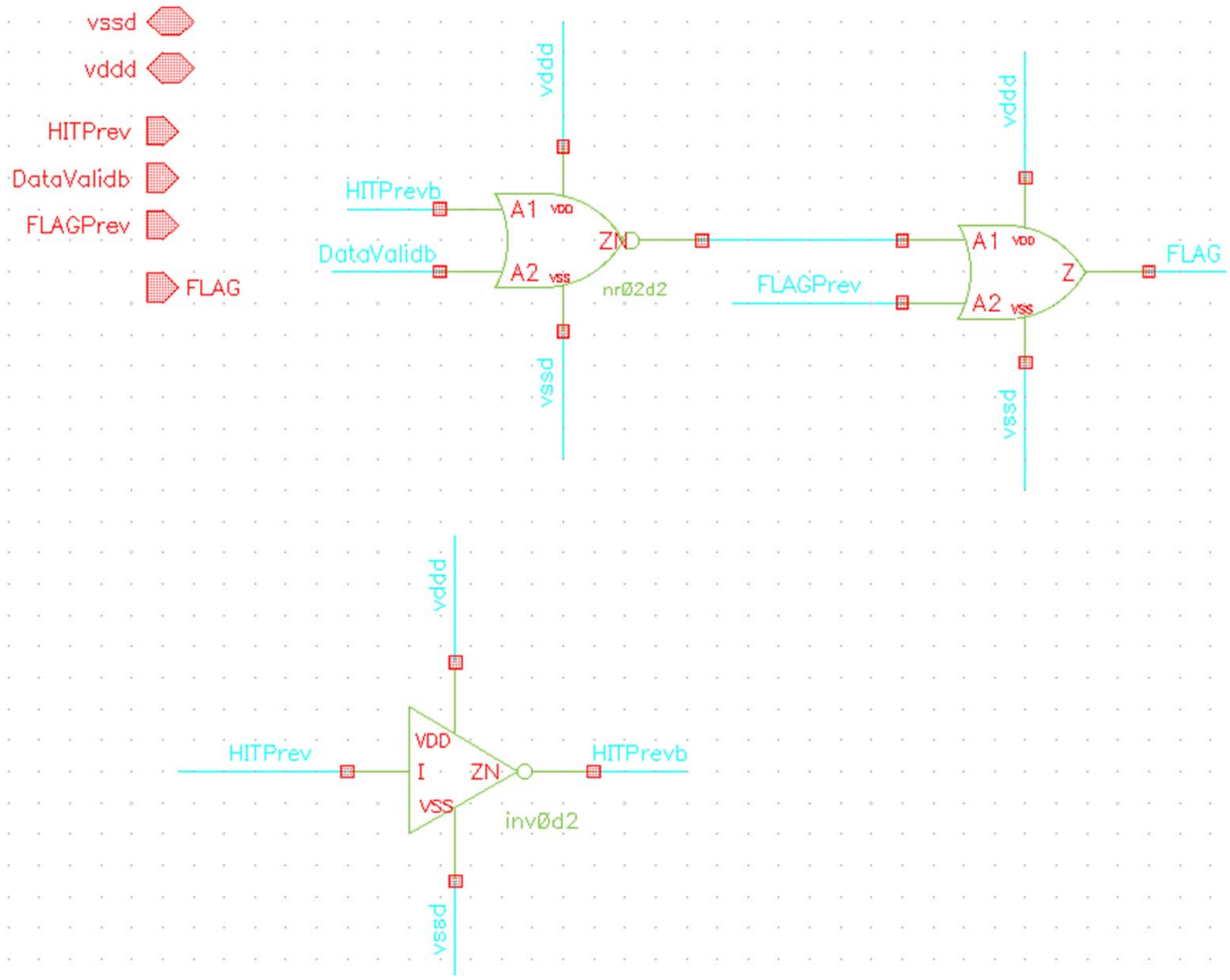
FLAG raising logic schematic



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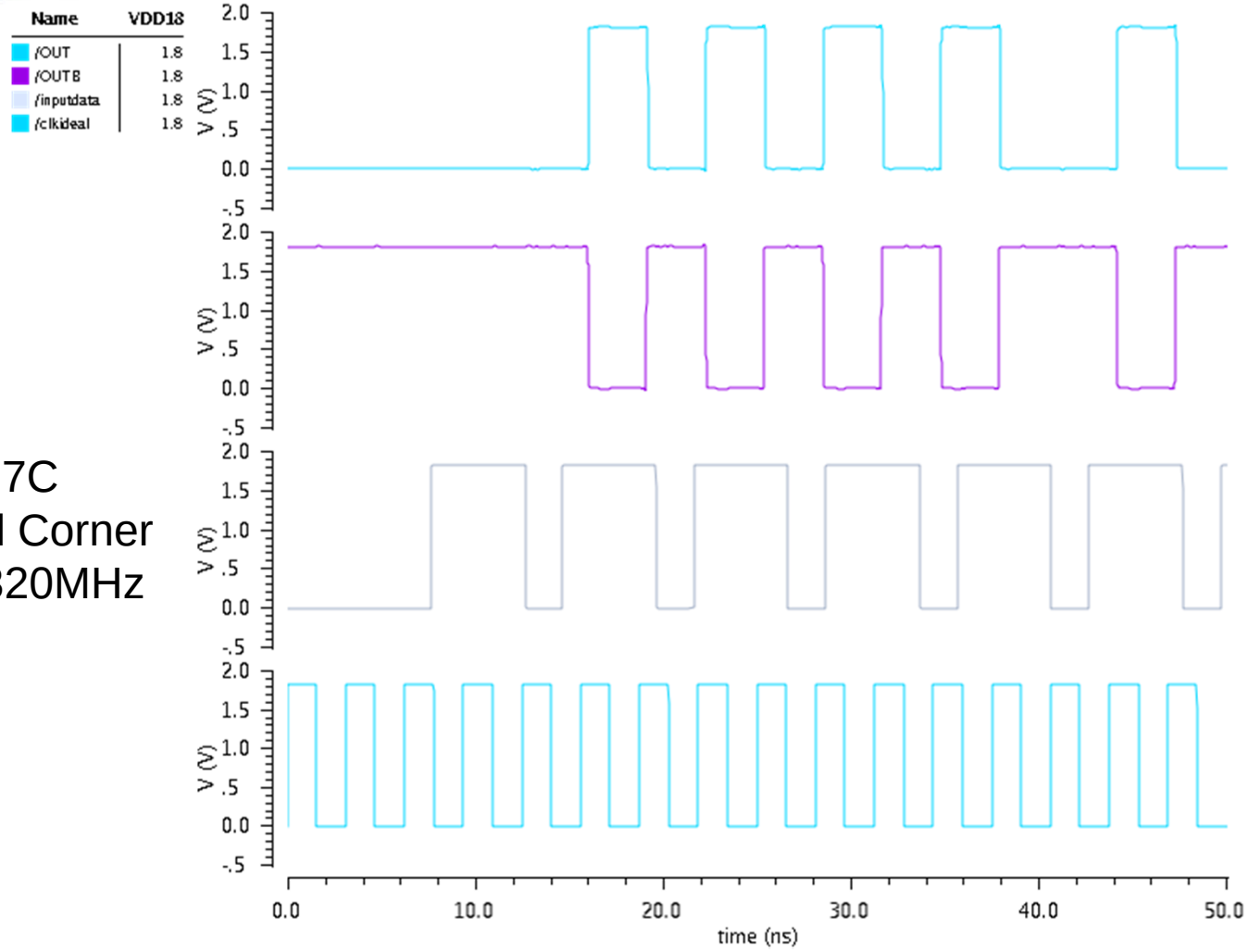
Edge detector / Monostable simulation



Temp=27C
Nominal Corner
Clock=320MHz

Detects all falling edge transitions on the input data even at 320 MHz clock speed
This block will operate at 40 Mhz

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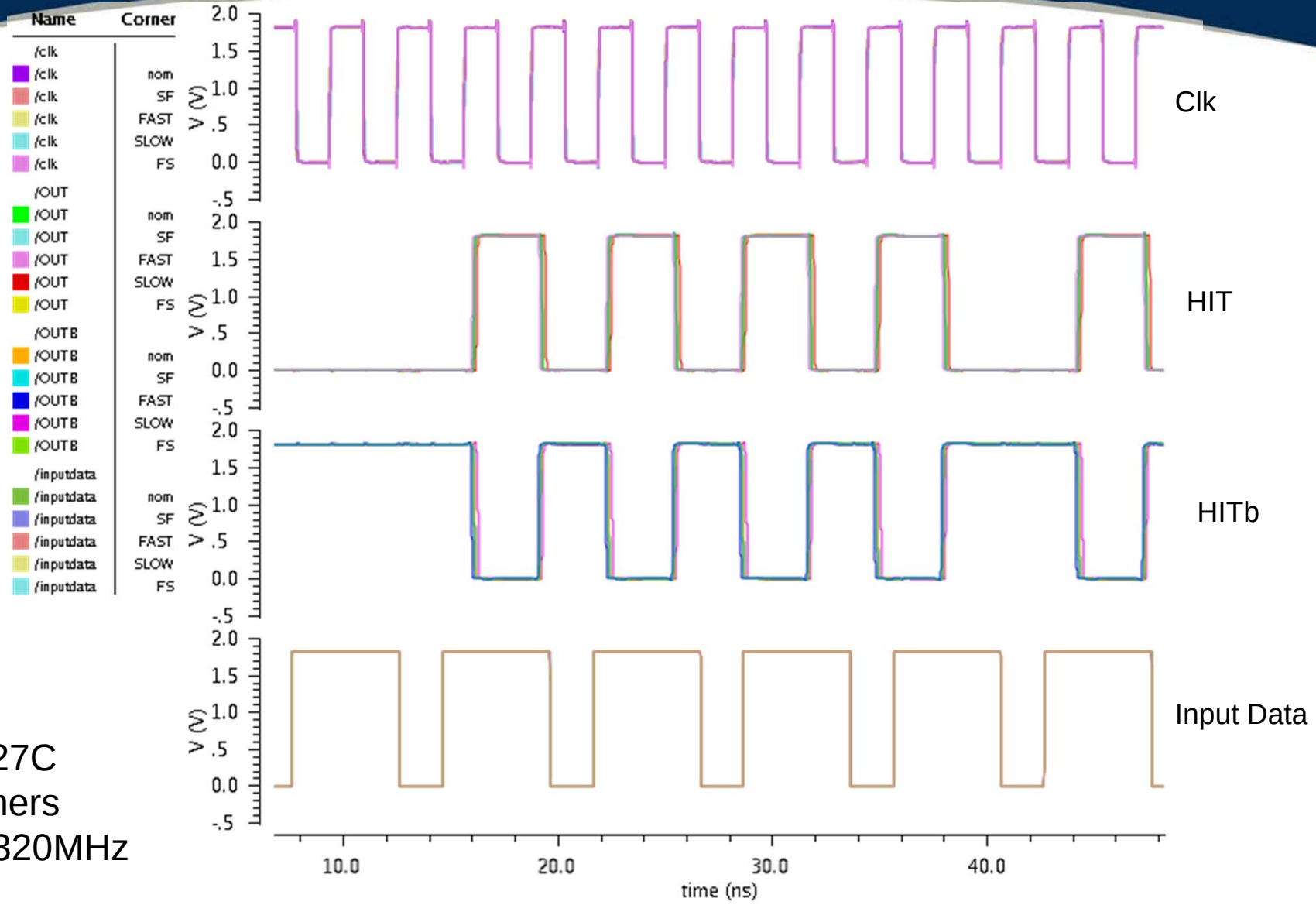
Edge detector / Monostable simulation



Temp=27C
All Corners
Clock=320MHz

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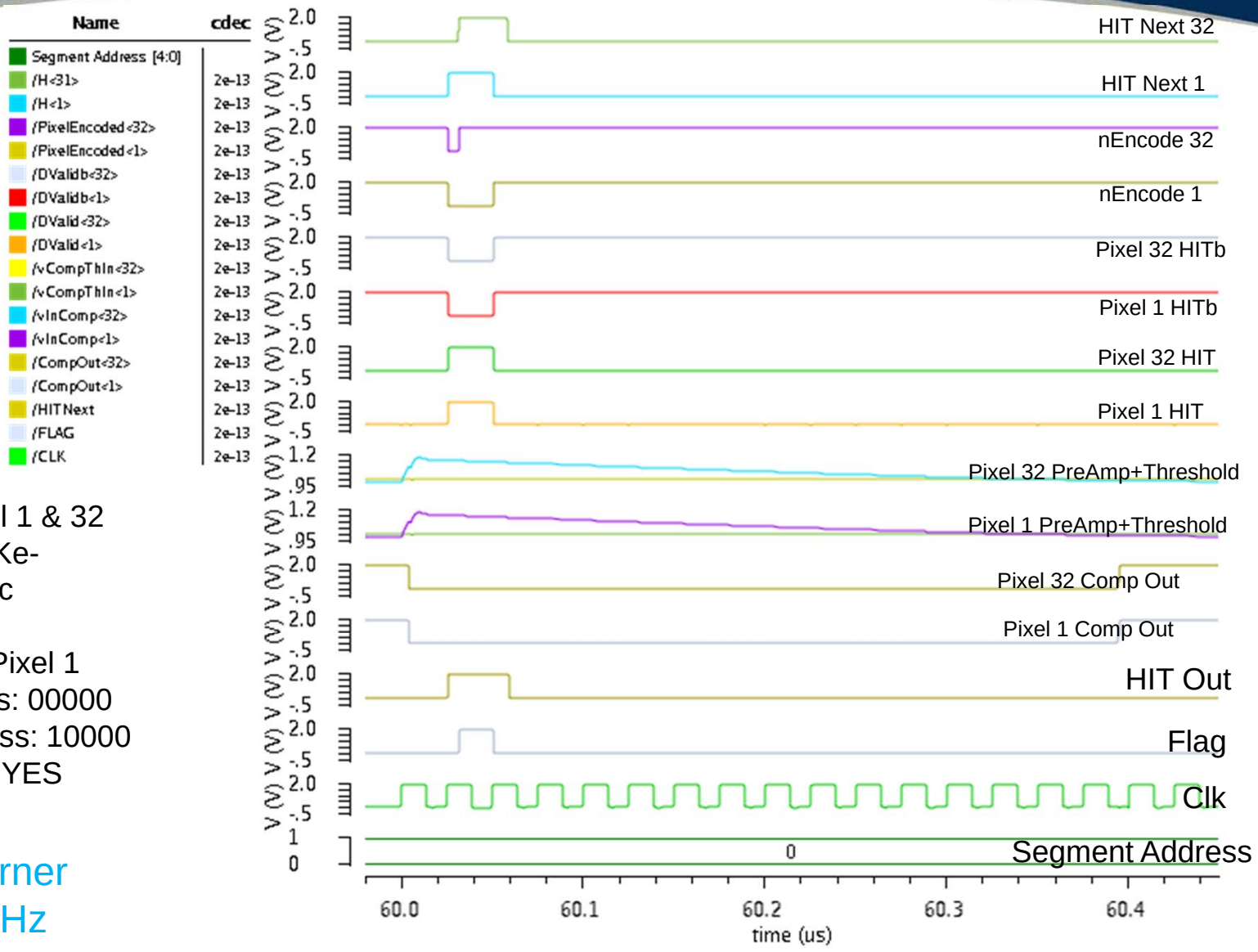
HIT encoding simulation for one complete column



Pixels hit: Pixel 1 & 32
Signal: Both 2Ke-
Hit time:60µsec
CC time:1ns
Address Out: Pixel 1
Pixel 1 address: 00000
Pixel 32 Address: 10000
FLAG Raised: YES

Temp=27C
Nominal corner
Clock=40MHz

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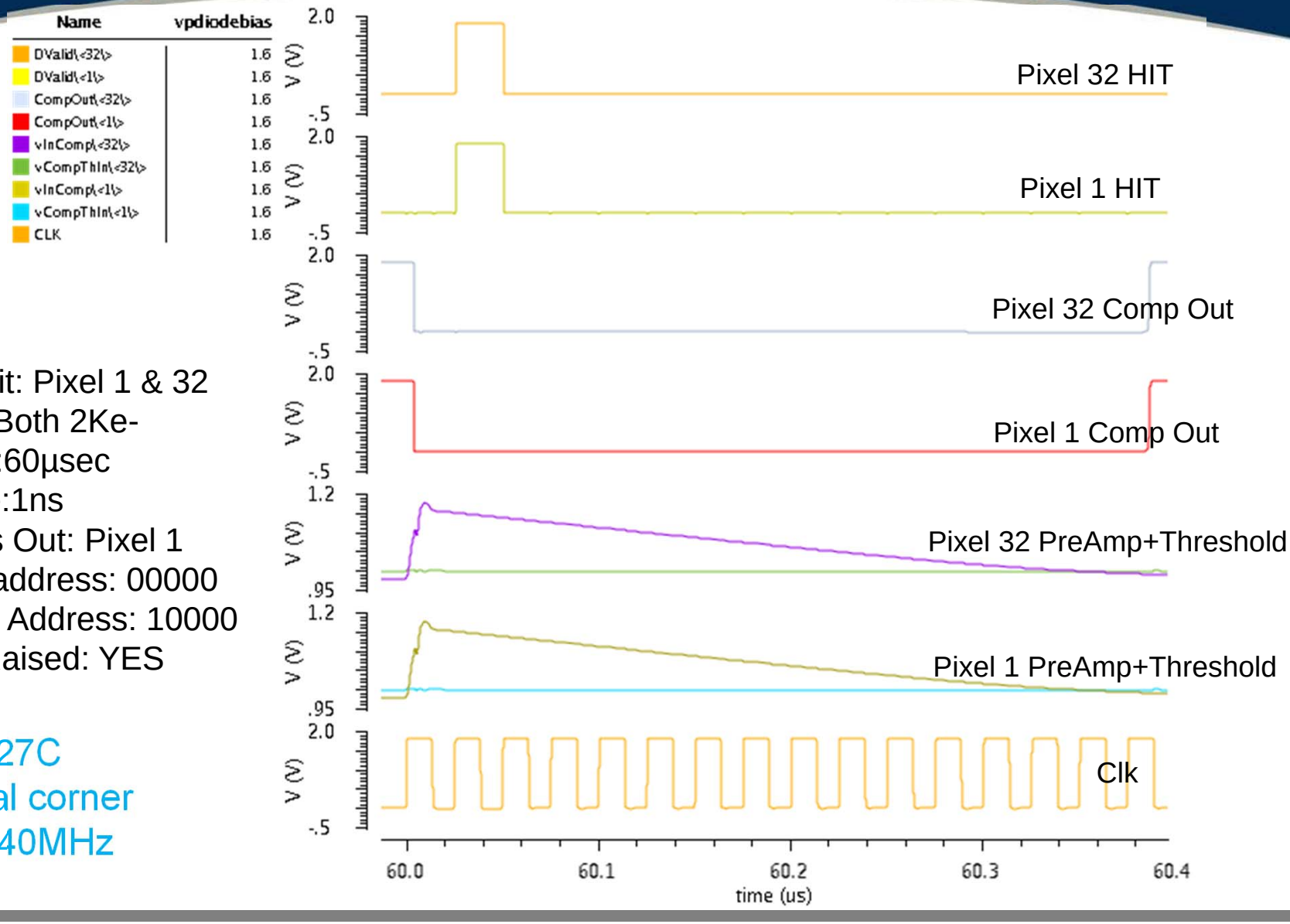
HIT encoding simulation (HIT detection)



Pixels hit: Pixel 1 & 32
Signal: Both 2Ke-
Hit time:60µsec
CC time:1ns
Address Out: Pixel 1
Pixel 1 address: 00000
Pixel 32 Address: 10000
FLAG Raised: YES

Temp=27C
Nominal corner
Clock=40MHz

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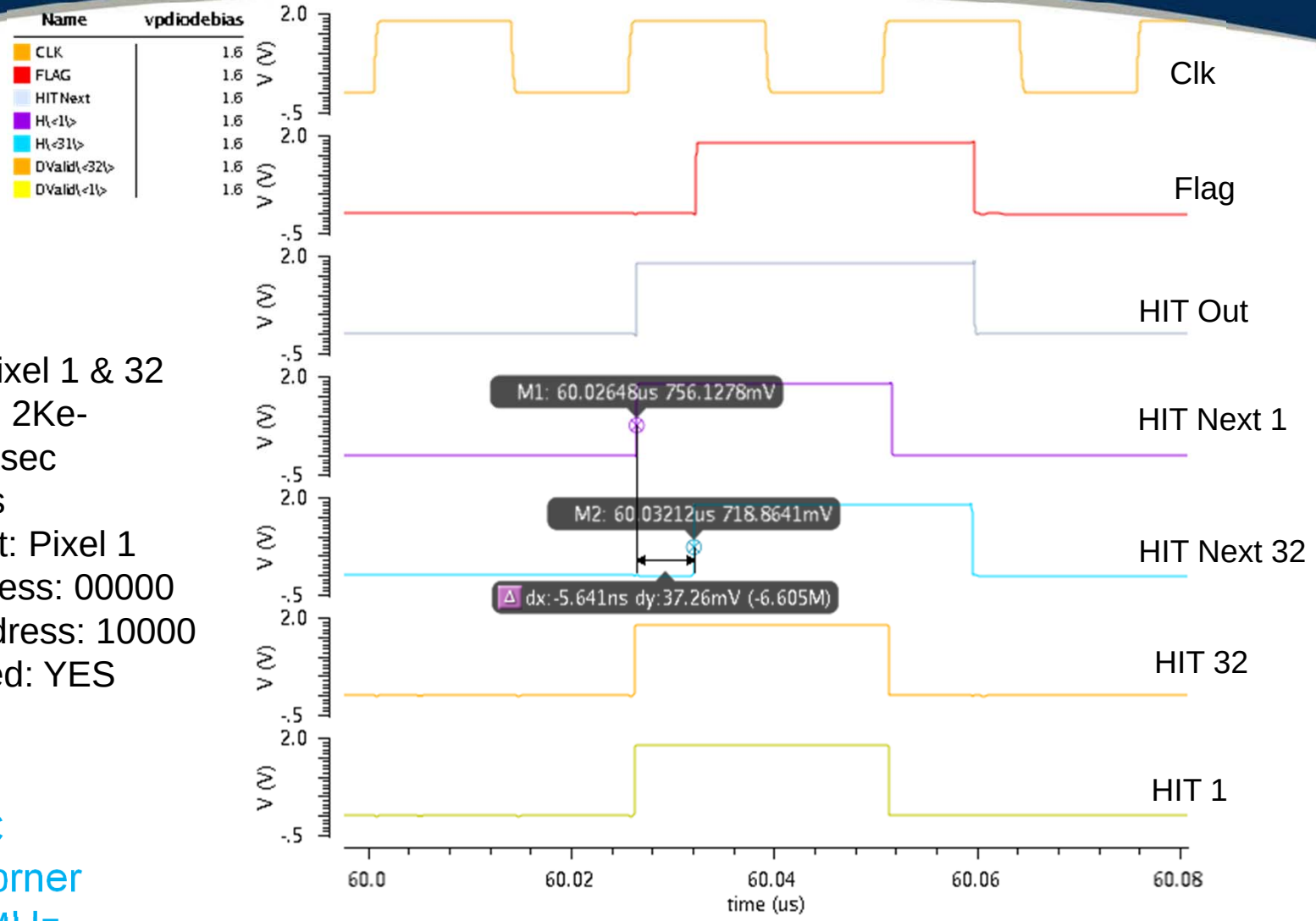
HIT encoding simulation (HIT propagation)



Pixels hit: Pixel 1 & 32
Signal: Both 2Ke-
Hit time:60µsec
CC time:1ns
Address Out: Pixel 1
Pixel 1 address: 00000
Pixel 32 Address: 10000
FLAG Raised: YES

Temp=27C
Nominal corner
Clock=40MHz

HIT Signal Propagation Time < 6ns from top to bottom of column

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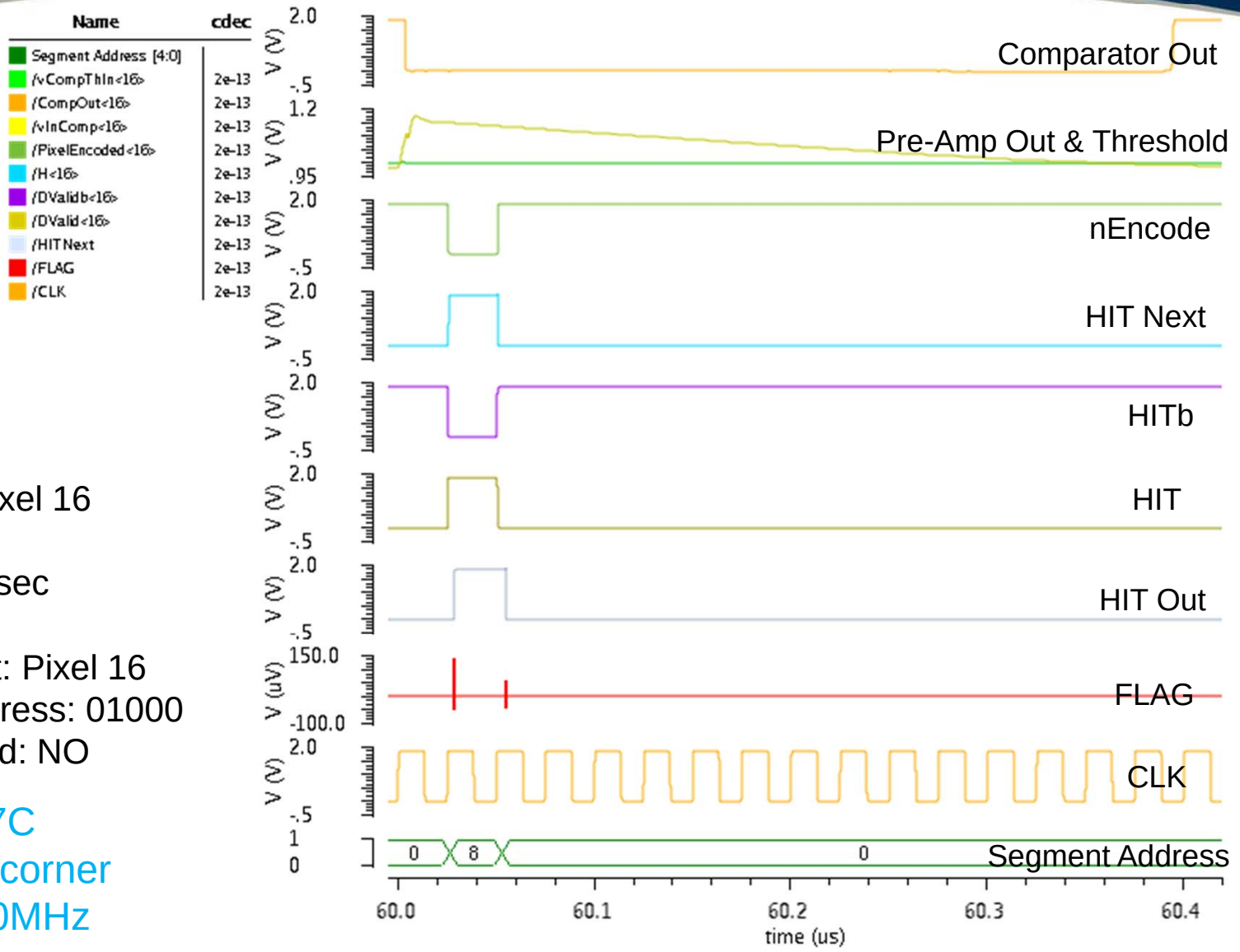
HIT encoding simulation
1 pixel in the middle hit



Pixels hit: Pixel 16
Signal: 2Ke-
Hit time:60µsec
CC time:1ns
Address Out: Pixel 16
Pixel 16 address: 01000
FLAG Raised: NO

Temp=27C
Nominal corner
Clock=40MHz

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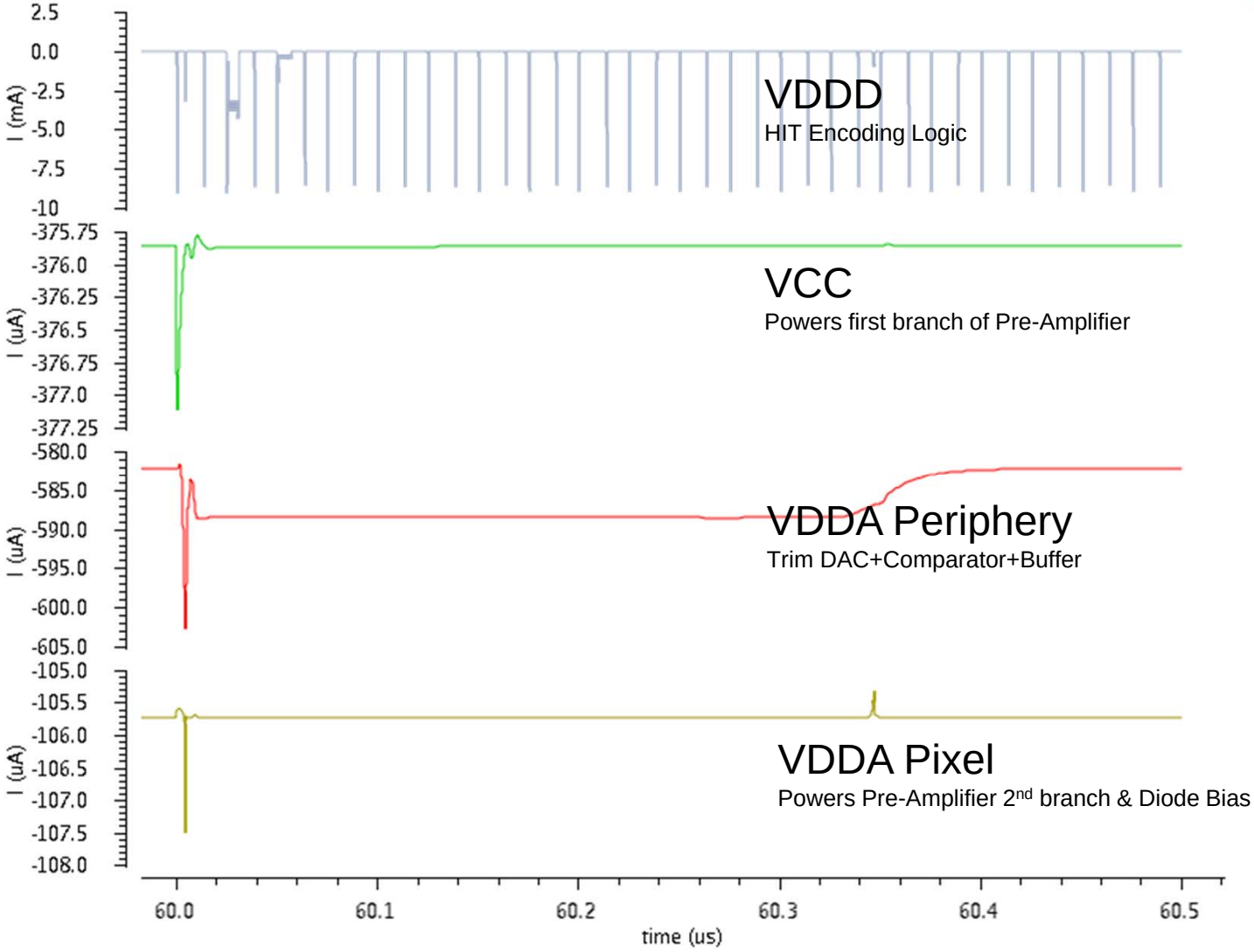
One complete column total power drawn

Rail	Irms
VDDD	67µA
VCC	376µA
VDDA Pixel	106µA
VDDA Periphery	582µA



Pixels hit: Pixel 1 & 32
Signal: Both 2Ke-
Hit time:60µsec
CC time:1ns

Temp=27C
Fast corner
Clock=40MHz