CALIBRATION

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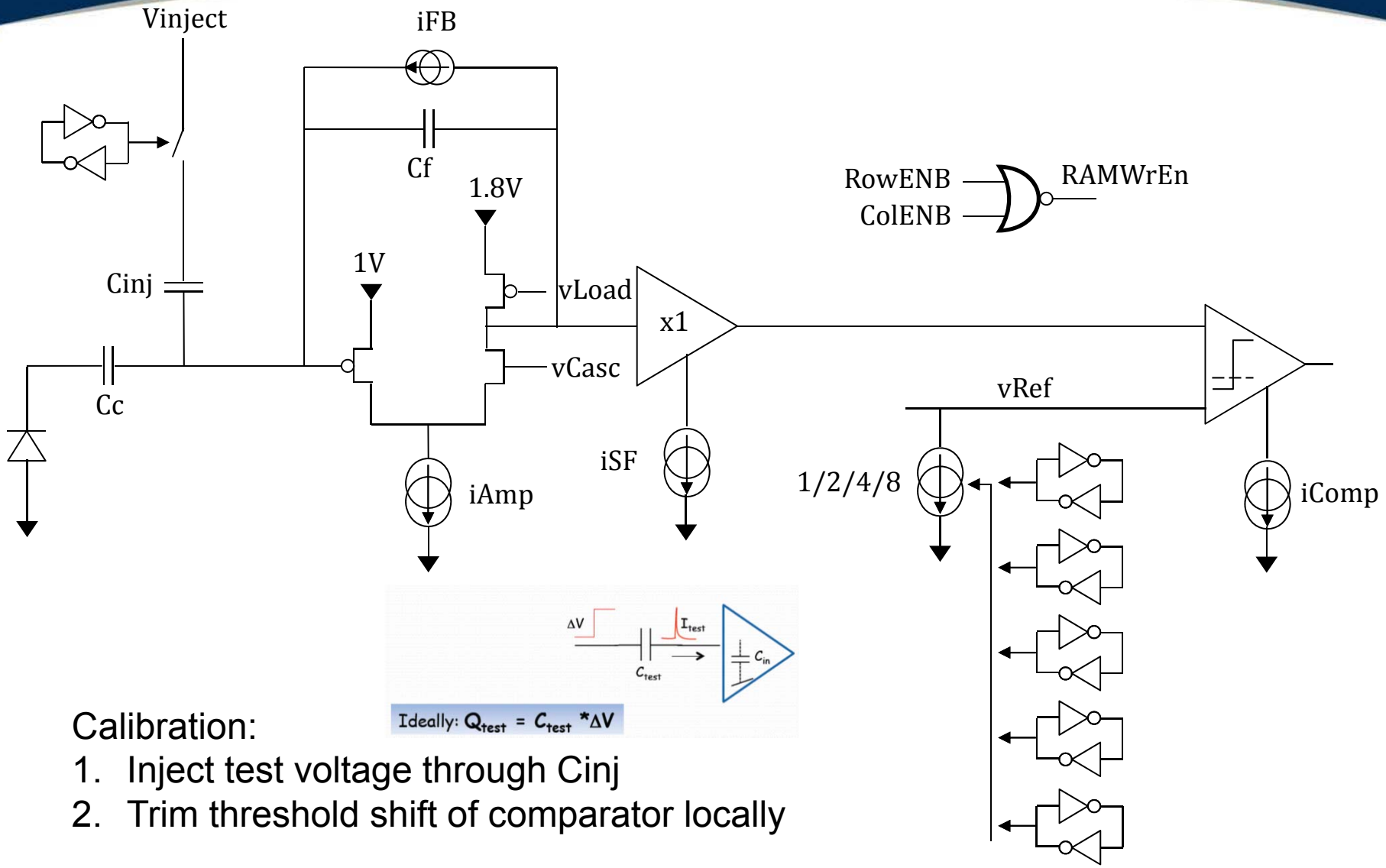
Analogue front-end conceptual block diagram



Calibration:

1. Inject test voltage through Cinj
2. Trim threshold shift of comparator locally

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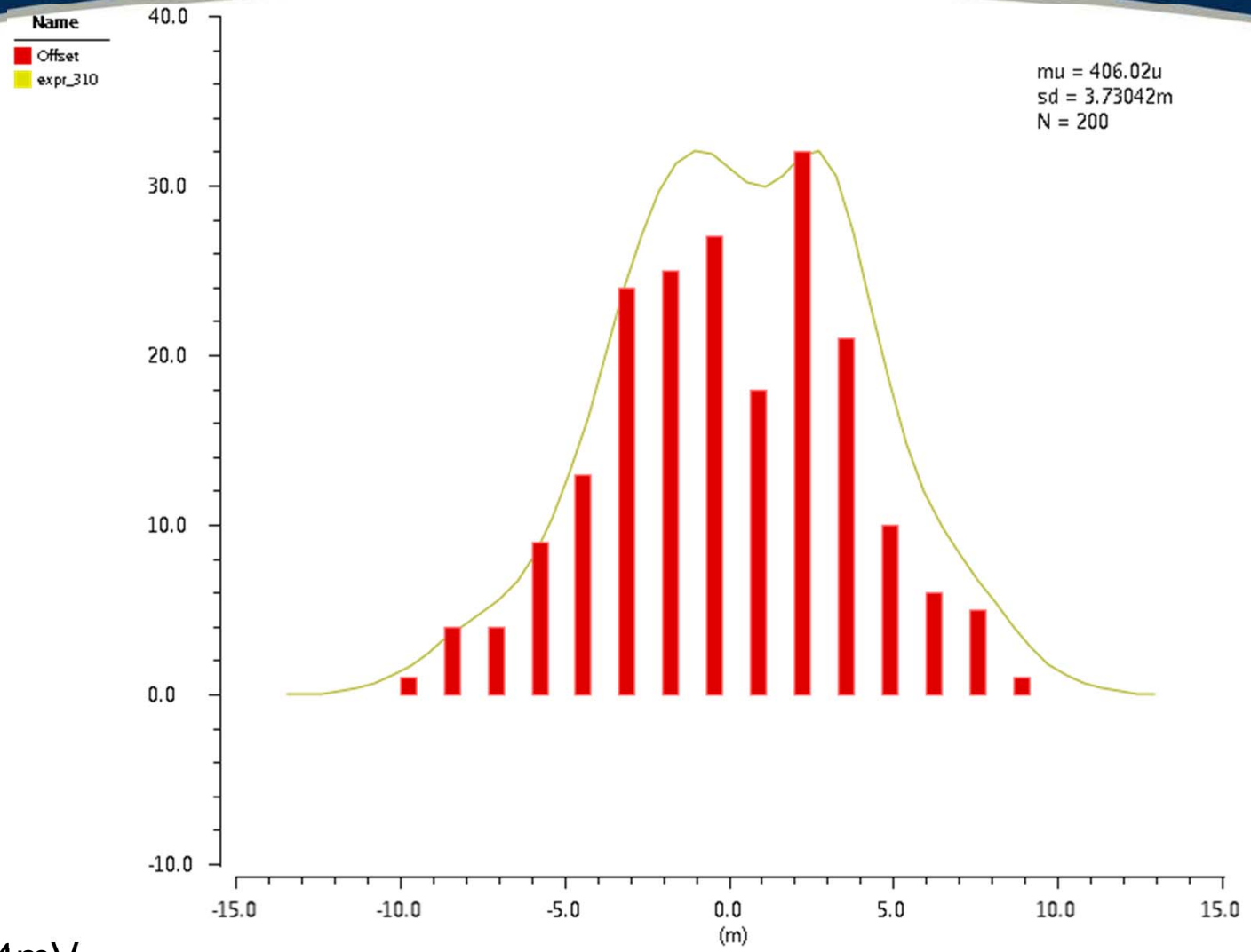
Comparator offset histogram



±3σ = 22.4mV

iTailStage1=15μA; iTailStage2=6μA;Temp=27°C

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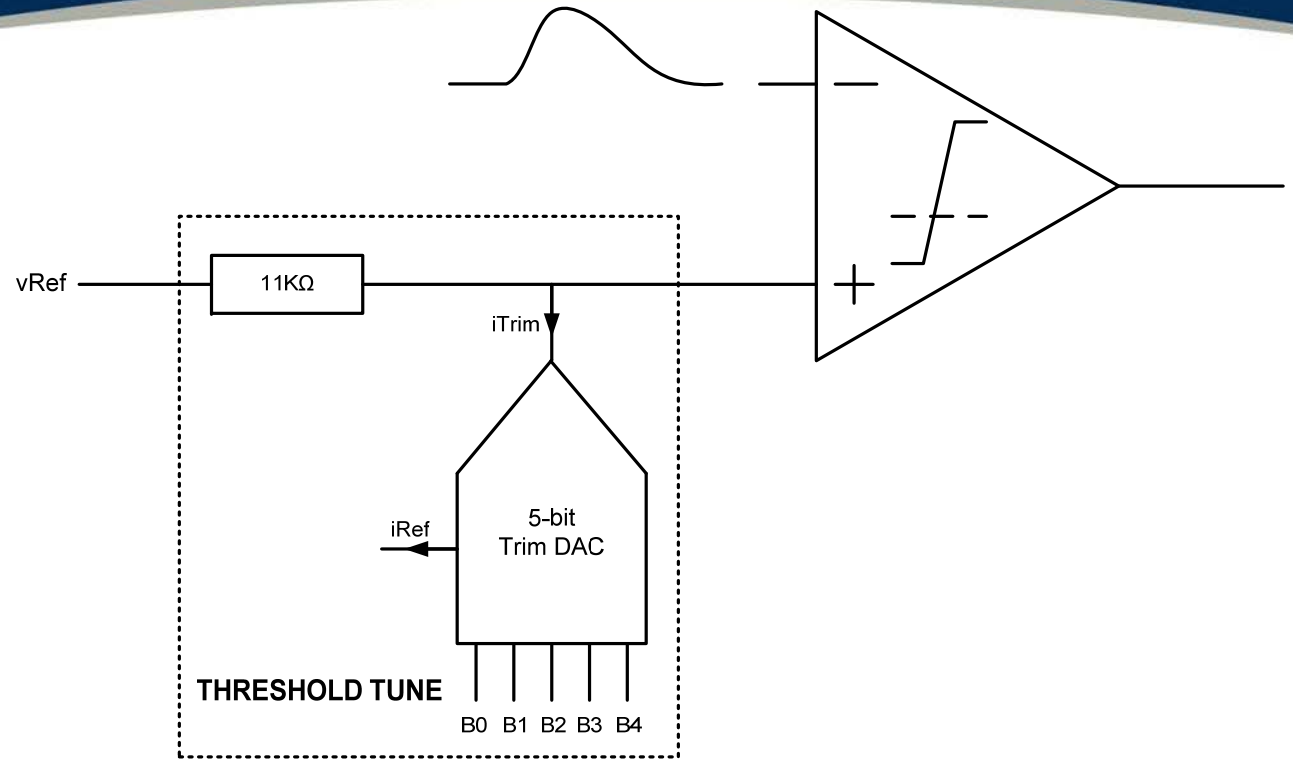
vRef/threshold calibration concept



- Global vRef provided externally; we can tune vRef locally using 5-bit Trim DAC
- Trim DAC sinks current; small voltage drop across 11KΩ poly resistor
- Tuning range needs to span ±3σ ≈ 25mV to correct for comparator threshold
- 5-bit to allow more range or better resolution
- LSB set by external reference current iRef
- Trim DAC output current iTrim is binary weighted
- Poly resistor has good linearity; low temp. and voltage coefficients; low parasitics

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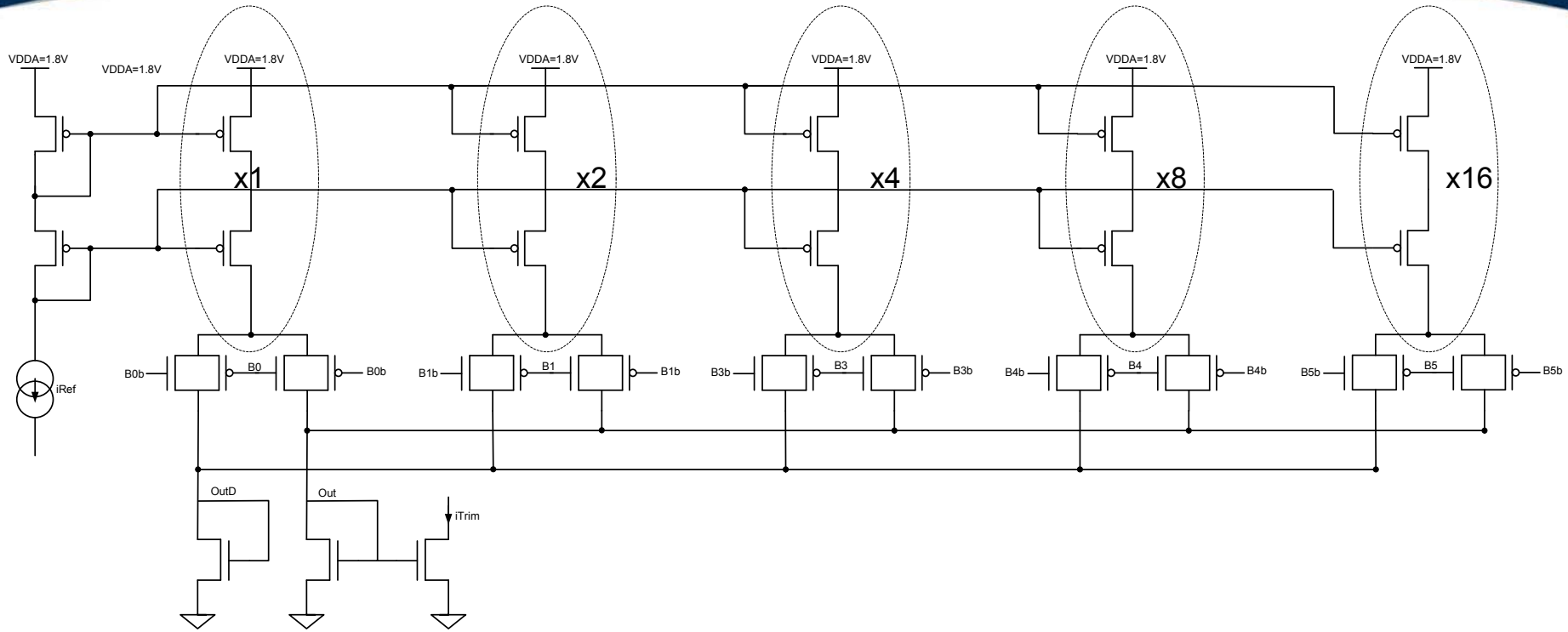
5-bit Trim DAC schematic



- 5-bit binary weighted current DAC; B0-B4 are configuration bits
- Each branch has PMOS cascode current mirrors for high linearity/accuracy
- Global reference current provided externally sets LSB
- Each branch has two transmission gates controlled by B0-B4 which divert current
- Two simple NMOS current mirror used as output stage
- Large enough device sizes in each branch ensures good matching

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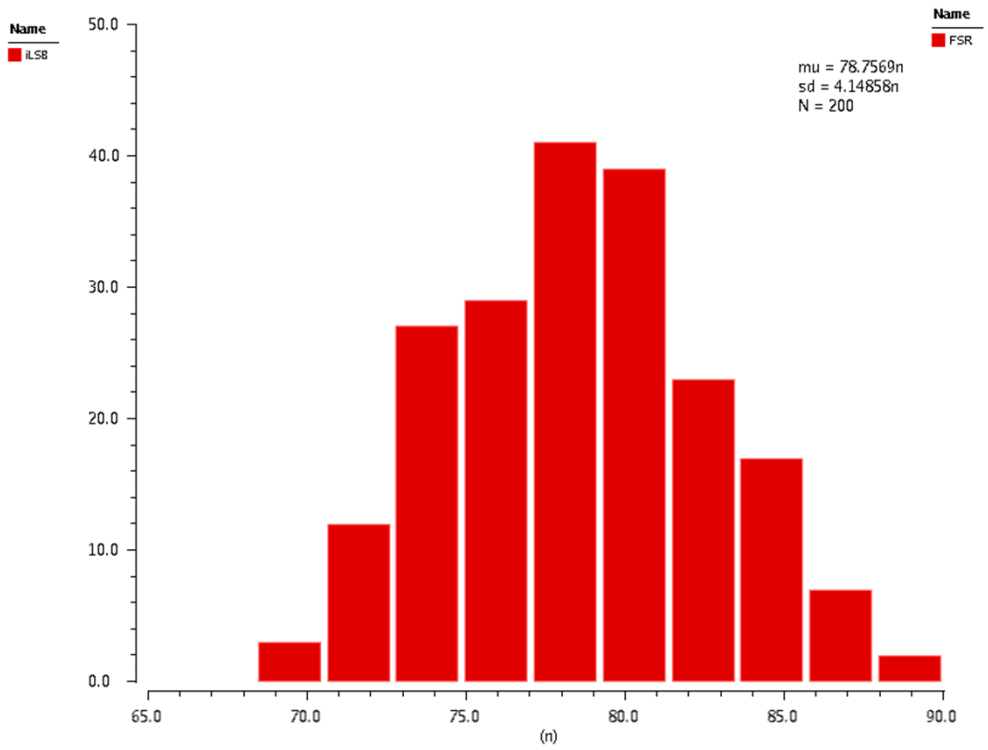
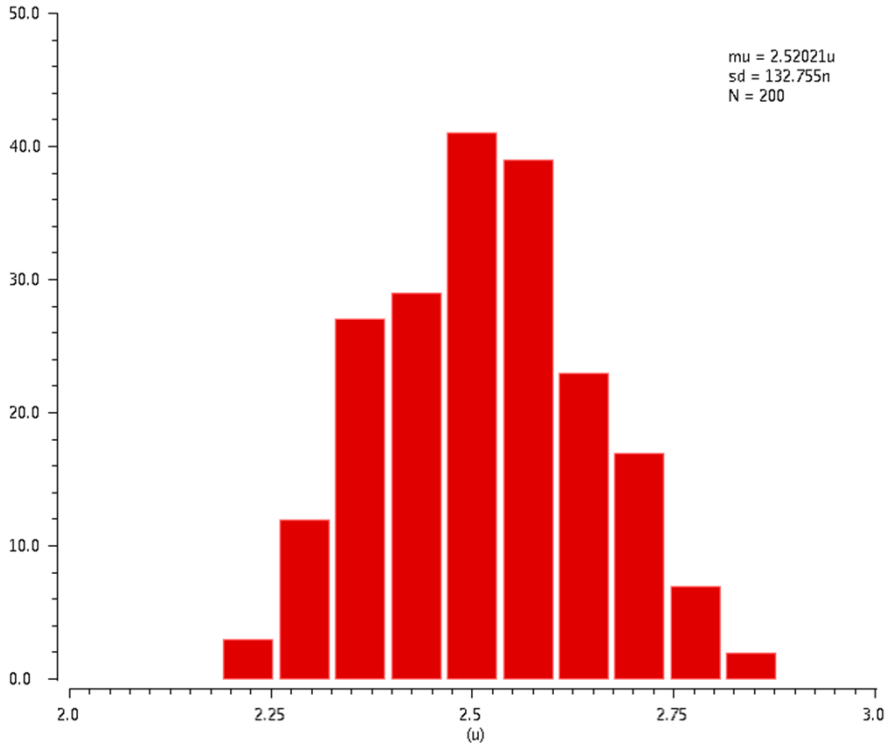
5-bit Trim DAC
iLSB & FSR Monte Carlo

T = 27°C
iRef=80nA



iLSB



FSR
(Full Scale Range)

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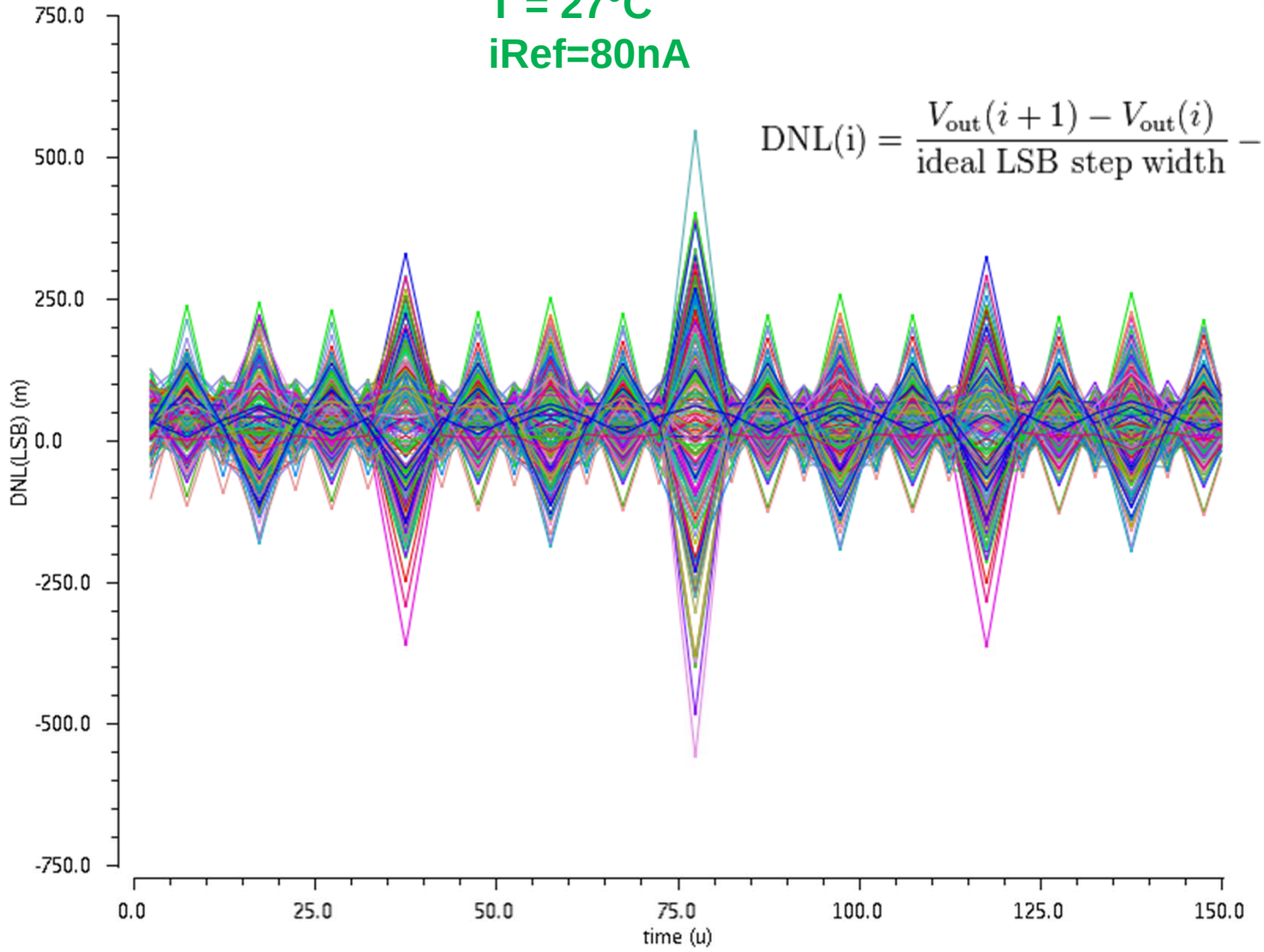
5-bit Trim DAC
DNL Monte Carlo

T = 27°C
iRef=80nA

$$\mathrm{DNL(i)} = \frac{V_{\mathrm{out}}(i+1) - V_{\mathrm{out}}(i)}{\text{ideal LSB step width}} - 1$$



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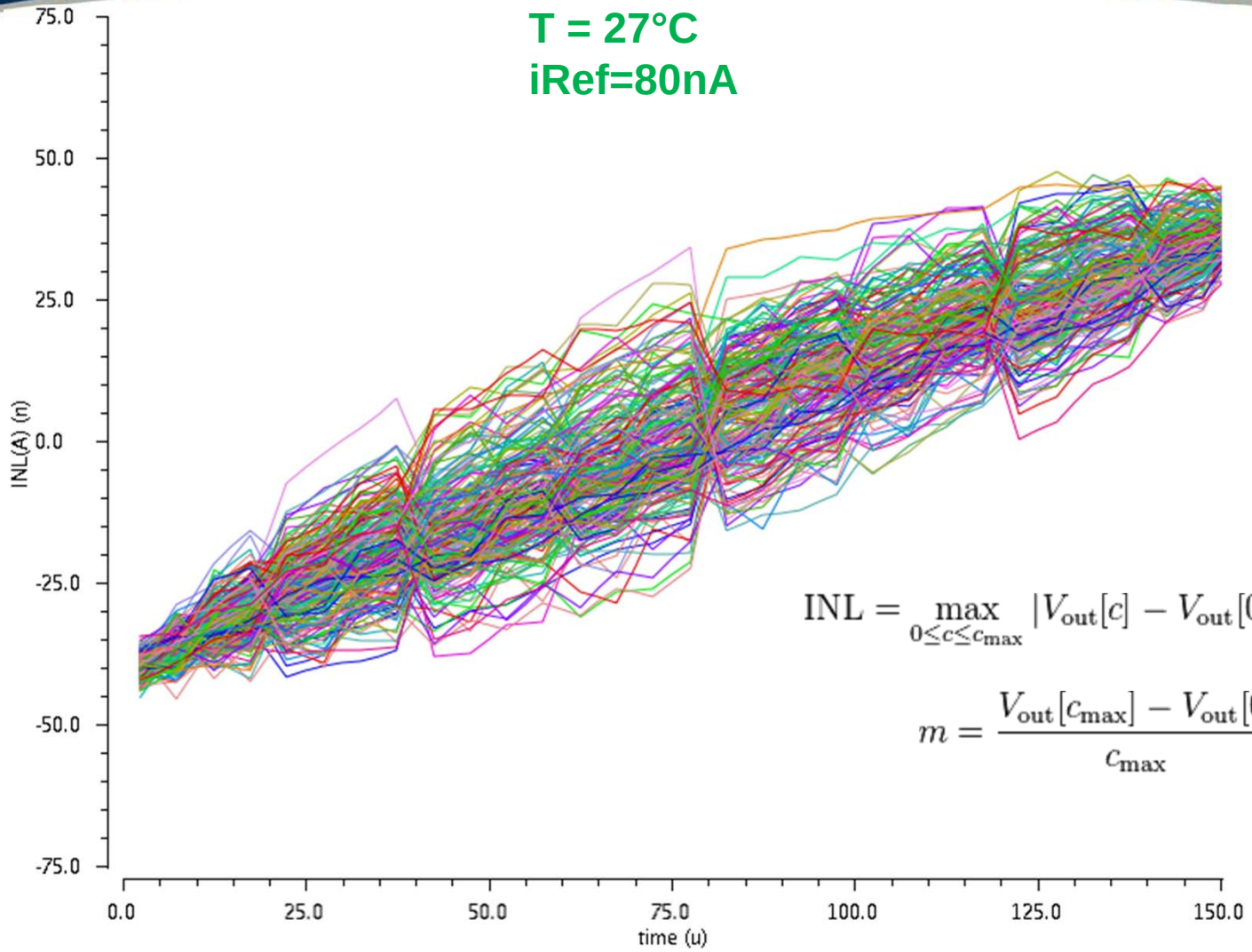
5-bit Trim DAC
INL Monte Carlo

T = 27°C
iRef=80nA



$$\mathrm{INL} = \max_{0 \le c \le c_{\max}} |V_{\mathrm{out}}[c] - V_{\mathrm{out}}[0] - c \cdot m|$$

$$m = \frac{V_{\mathrm{out}}[c_{\max}] - V_{\mathrm{out}}[0]}{c_{\max}}$$

Need to divide these values by iLSB to obtain values in terms of LSB

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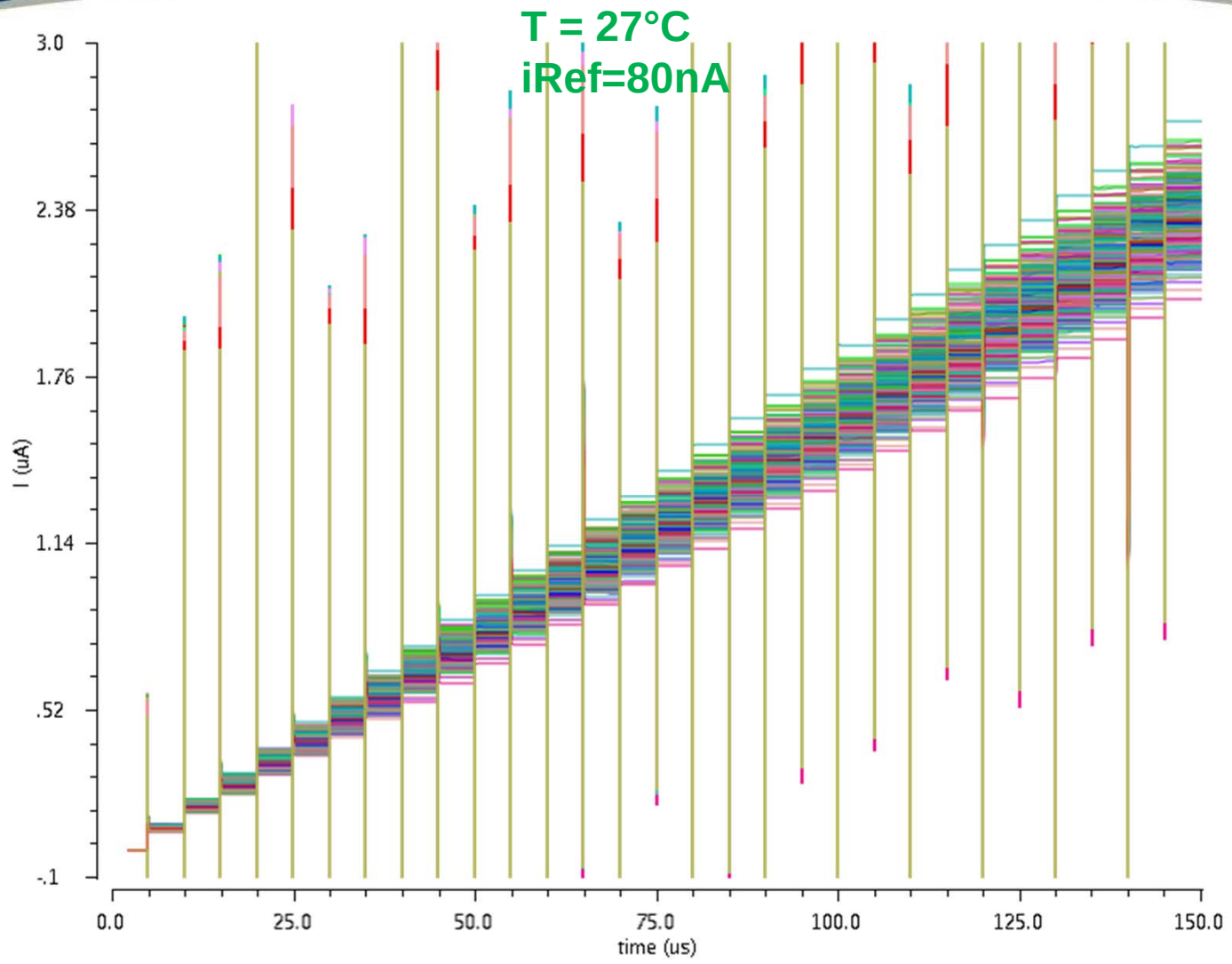
5-bit Trim DAC
iTrim Monte Carlo



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5-bit Trim DAC simulated specification

T = 27°C
iRef=80nA

5-bit Trim DAC (iRef=80nA)			
	Min	Max	Mean
LSB	68.59nA	90.09nA	78.76n
DNL	-0.561LSB	0.546LSB	
INL	-0.5LSB	0.6LSB	
FSR	2.19µA	2.89µA	2.52µA

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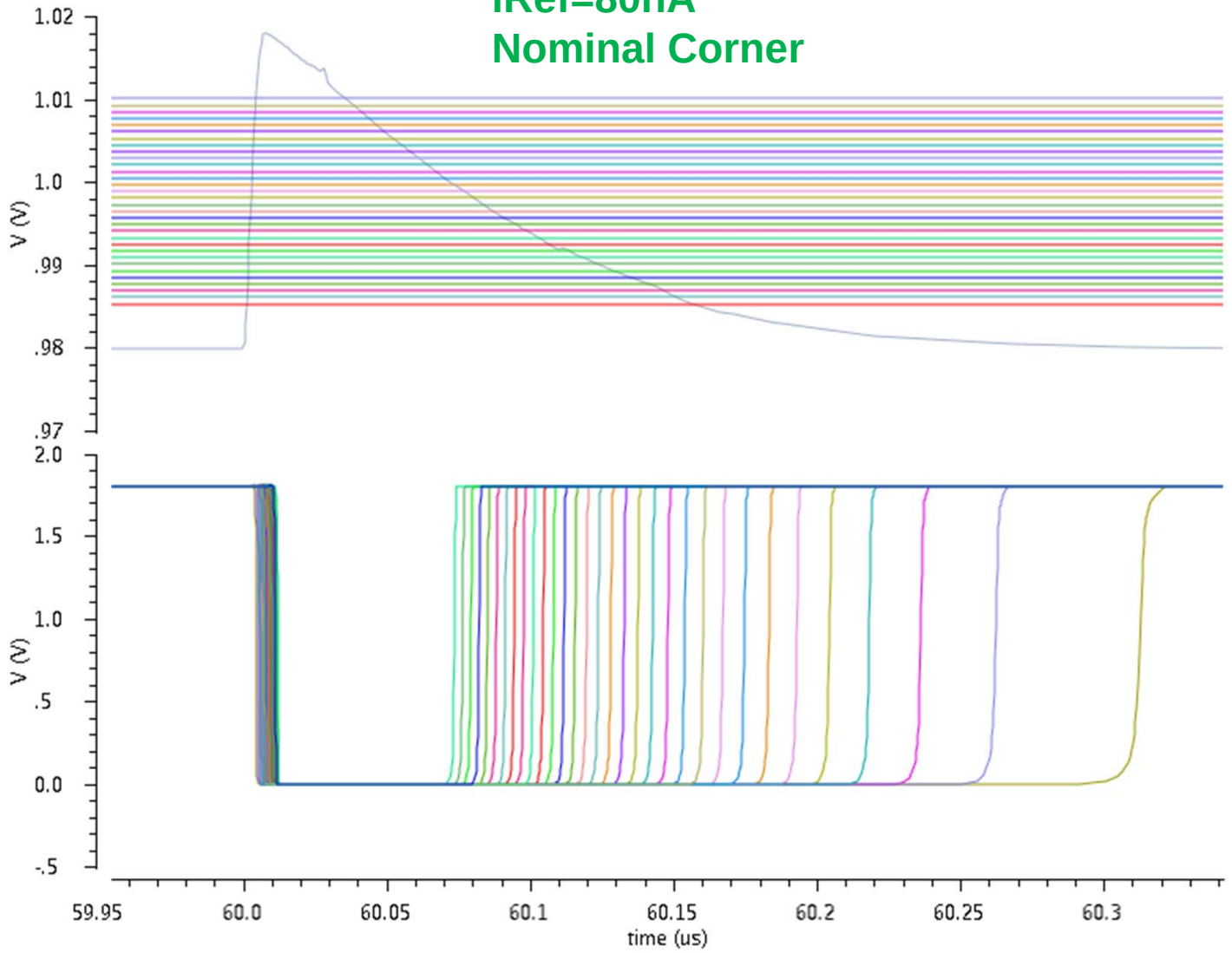
Full 5-bit Adjustment of Trim DAC

T = 27°C
iRef=80nA
Nominal Corner



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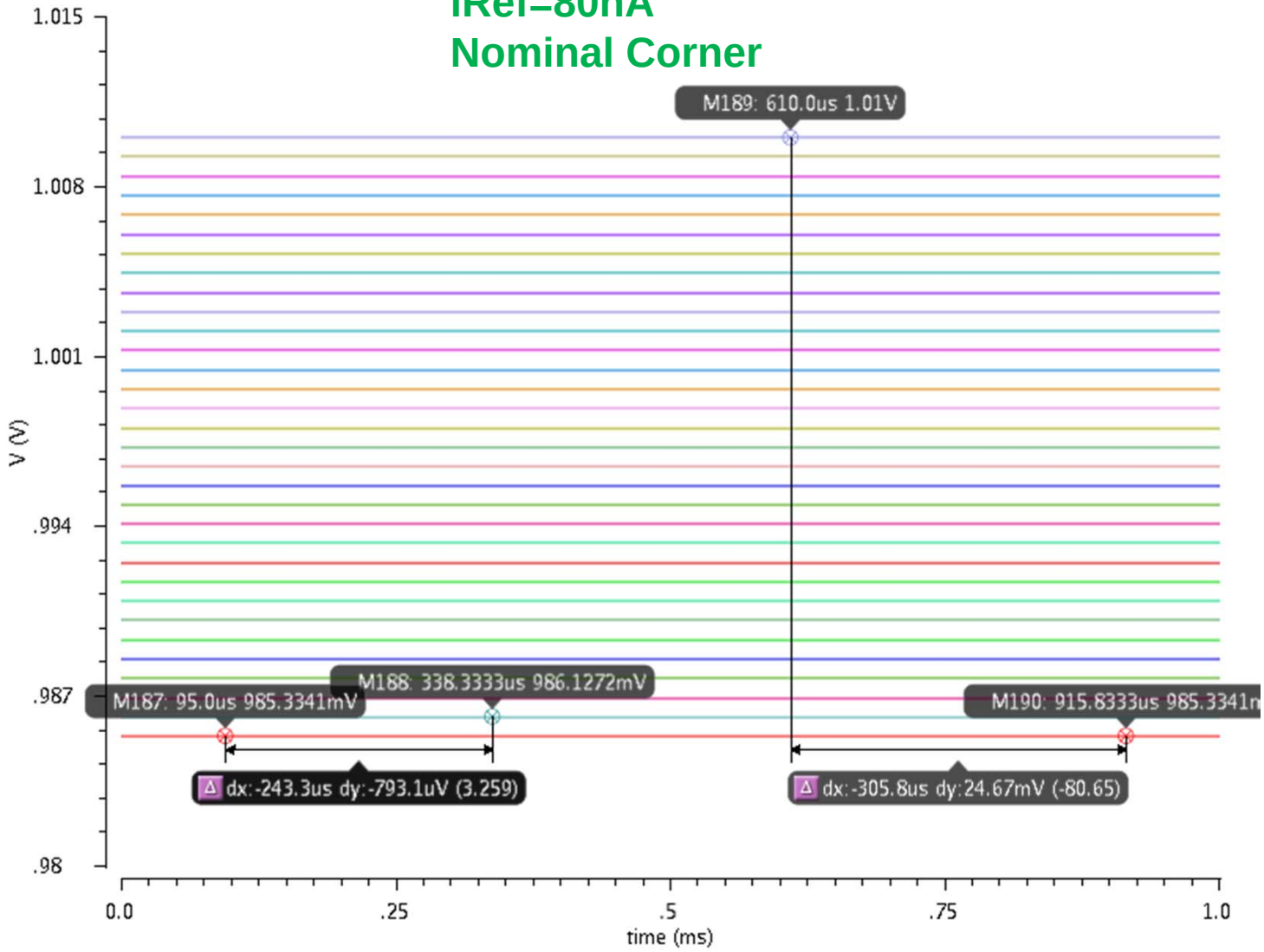
Full 5-bit sweep of vRef

T = 27°C
iRef=80nA
Nominal Corner



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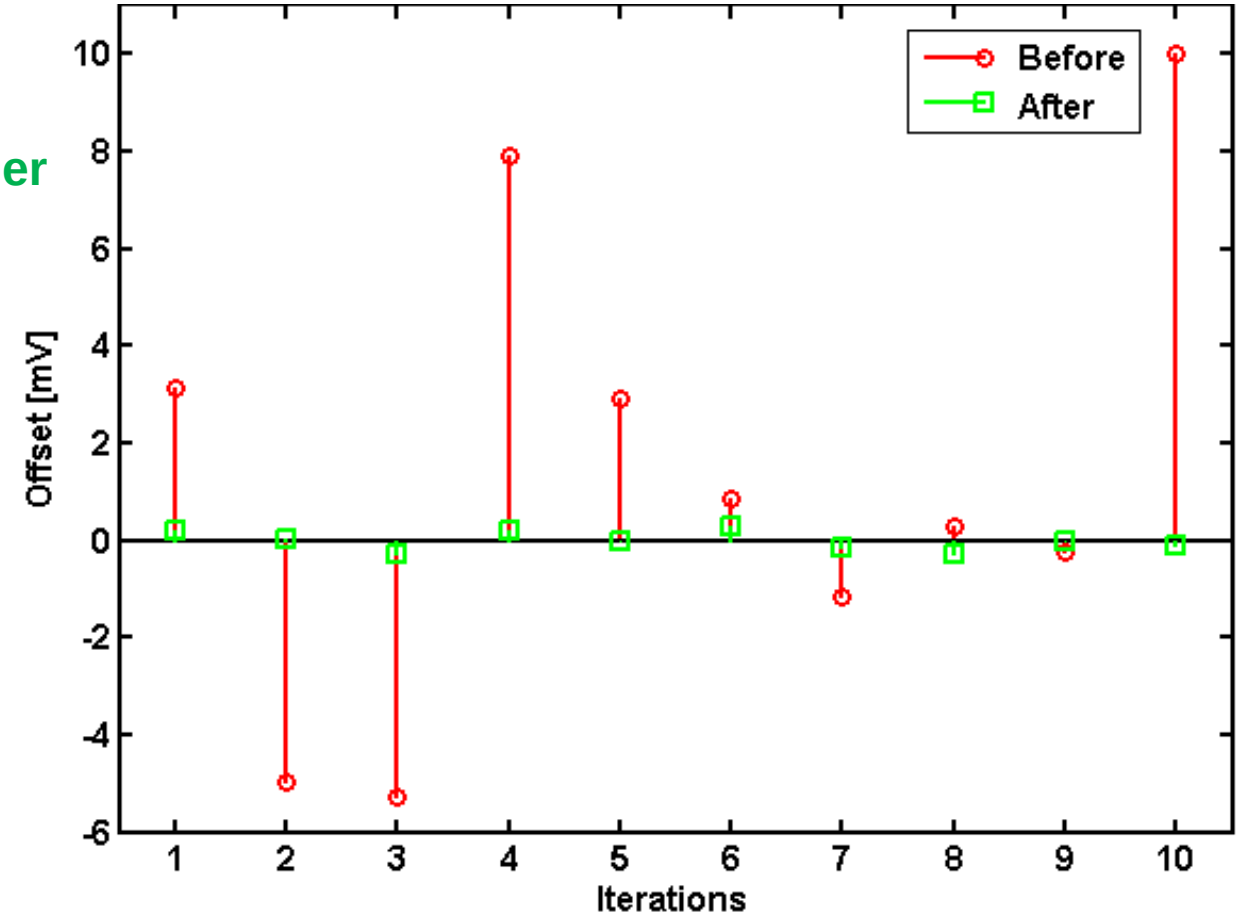
Offset trim simulation

T = 27°C
iRef=80nA
Nominal Corner



10 Monte Carlo runs to obtain comparator offset variation before and after trimming.
Offset variation before trim: 4.9mV or 50e-
Offset variation after trim (residual noise): 196µV or 2e-