CHESS-2 Test Interface/Carrier

# Testing requirements

* Can be detached for irradiation (no active components on carrier board?).
* Access for Edge TCT.
* Convenient mount for various test beam setups.
* Digital control/readout connection can serve all test setup scenarios. Test chain signal connection and drive design will hopefully not to stretch the CHESS-2 signal drive capability.
* AMS/TowerJazz version compatibility.
* Extension flexibility for incorporating ABCN’+HCC (FPGA emulation first) in the readout chain.
* Down-stream connection flexibility to allow easy switch between different backend test setups with ATLYS/HSIO etc.

# CHESS2-AMS Interface Signals

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Multiplicity**  **Per chip** | **Type** | **Description** |
| SELECT | 1 | CMOS | Shared between chips on module |
| RESET | 1 | CMOS | Shared between chips on module |
| SYNC | 1 | LVDS | Shared between chips on module |
| 320 MHz Clock | 1 | LVDS | Shared between chips on module |
| SACI clock | 1 | CMOS | Shared between chips on module |
| SACI command | 1 | CMOS |  |
| SACI response | 1 | CMOS |  |
| Data Output | 13 | LVDS |  |
| DAC Level Control ? | 1 | ? | How to inject ? Remote level control precision ? |
| LVDS voltage Control | 2 | Analog | Shared between chips on module |
| Pulser | 1 | Analog | Voltage range ? |
| HV | 1 | HV | 120-500V |
| 3.3V | 1 | LV |  |
| 2.5V | 1 | LV | Generate locally ? |
| 1.8V | 1 | LV | Generate locally ? |