Test Beam Measurements for the Upgrade of the CMS Phase I Pixel Detector

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on behalf of the CMS Collaboration

4th Beam Telescopes and Test Beams Workshop
February 4, 2016, Paris/Orsay, France

HELMHOLTZ | ASSOCIATION

DESY

CMS

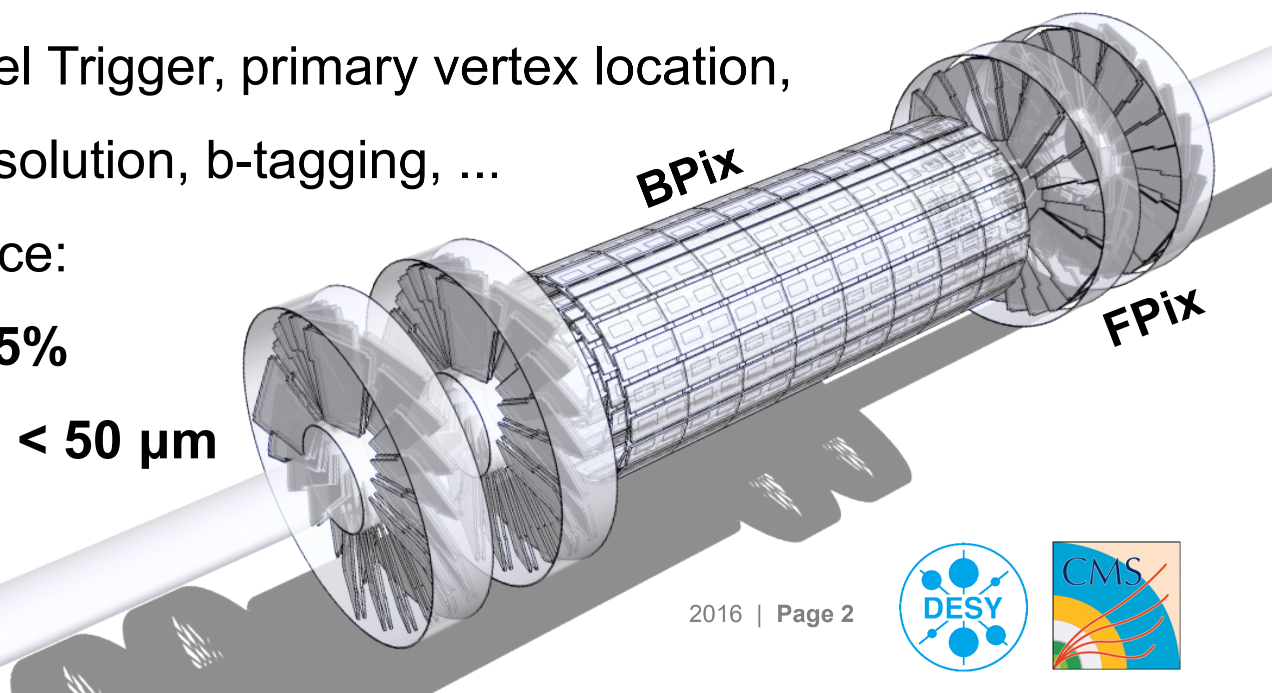
The current CMS Pixel Detector

- Innermost component of the CMS experiment
- **Hybrid silicon pixel detector**
- 3 barrel layers (**BPix**), 2x2 end disks (**FPix**)
- 66 M readout channels with 100x150 µm pixel pitch
- Designed for instantaneous luminosities of 1×10^{34} $cm^{-2}s^{-1}$

- Crucial for High Level Trigger, primary vertex location, secondary vertex resolution, b-tagging, ...
- Excellent performance:

  Single hit eff. > 99.5%

  Primary vertex res. < 50 µm
  (with > 15 tracks)



Phase I Upgrade - Motivation & Constraints

- Maintain and improve physics performance @ higher instantaneous luminosity of $\mathbf{2x10^{34}\ cm^{-2}s^{-1}}$, up to and exceeding 50 pile-up events

  → Requires **new front-end electronics**

- Smaller beam pipe in CMS (installed in LS1): **59 mm → 45 mm** (outer diameter)

- Same detector volume, constrained by the CMS tracker

- Same services from patch panel outwards, this requires

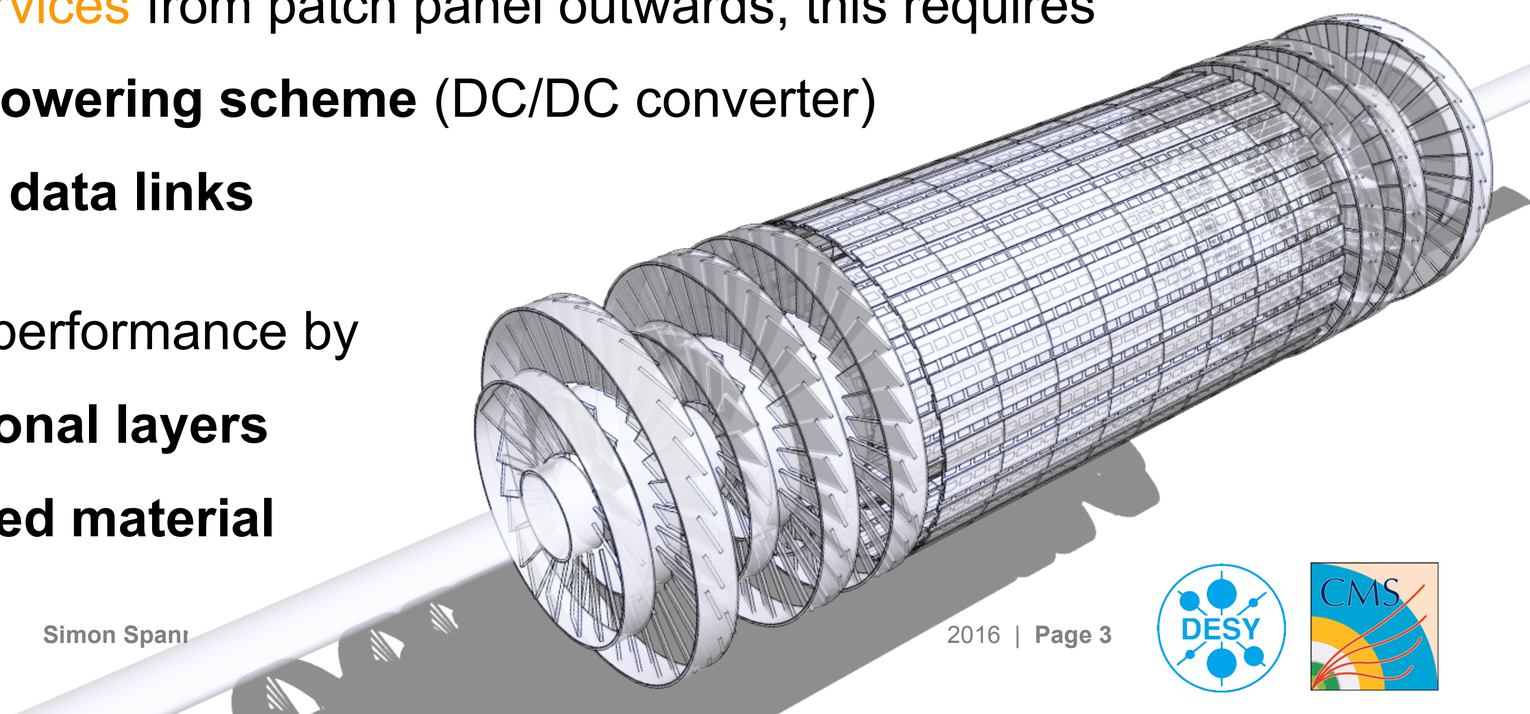
  → **new powering scheme** (DC/DC converter)

  → **faster data links**

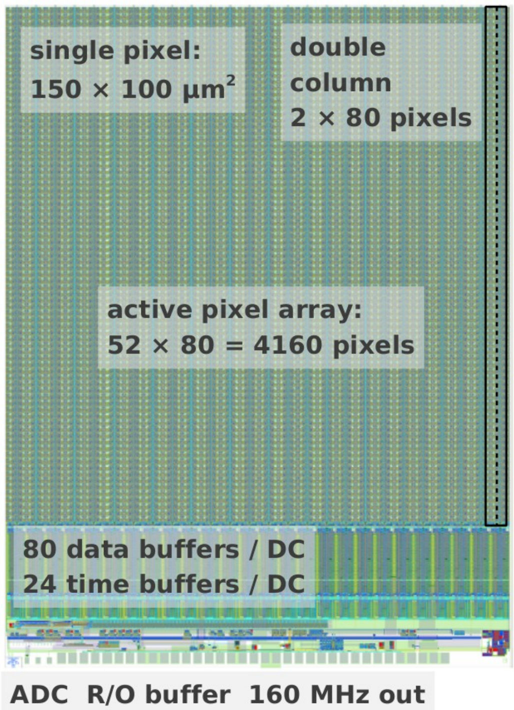
- Improve performance by

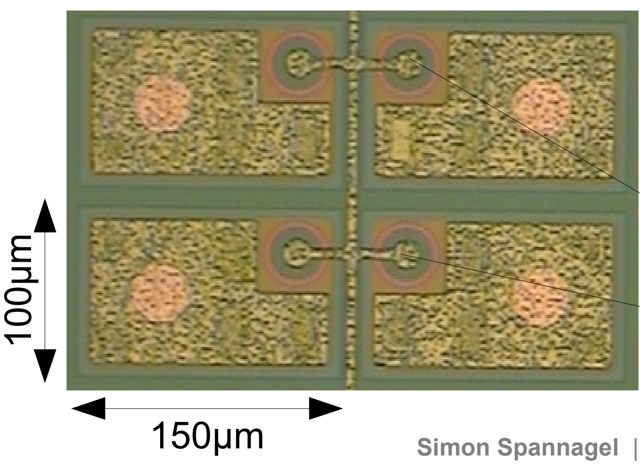
  → **additional layers**

  → **reduced material**



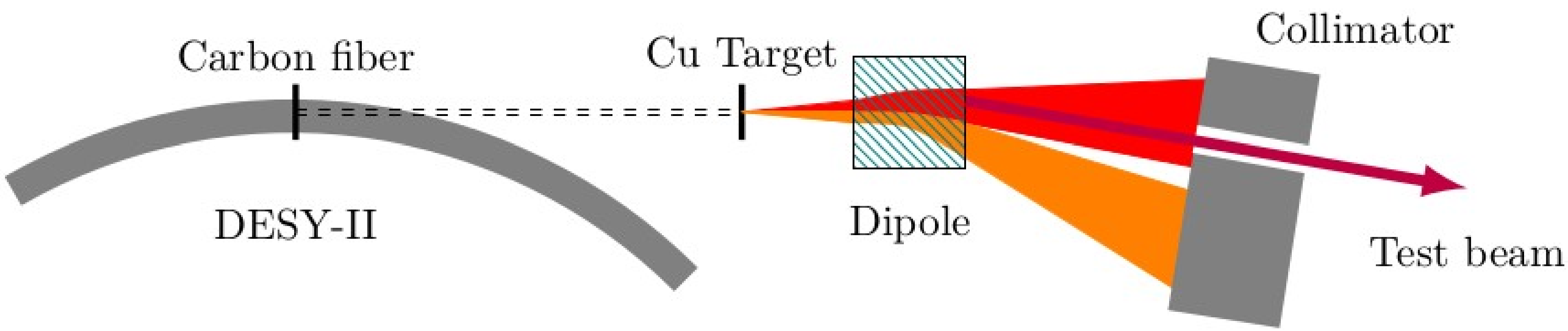
Sensor and Readout Chip





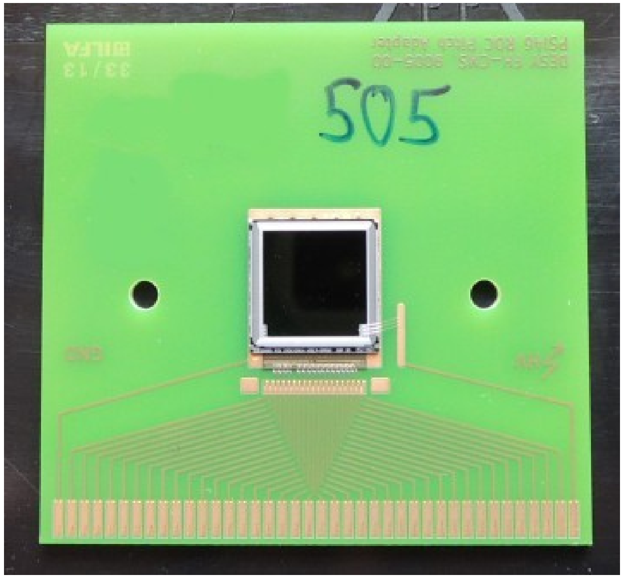
- 250nm analog CMOS ASIC
- High radiation tolerance
- Advancement of present front-end
  - Increased buffers to mitigate data loss
  - Global readout buffer to reduce dead time
  - Low threshold: **~1.5 ke**
  - 8bit on-chip ADC
  - 160 Mbit/s readout for higher bandwidth
- 240 production wafers, yield > 90%
- Dedicated L1 ROC, faster pixel readout
- Sensors
  - silicon **n^{+}-in-n**, p-spray/p-stop isolation
  - 150x100um pixel pitch, 285um thickness
  - Bias/grounding grid

Chip Qualification in the Test Beam



> DESY-II Synchrotron

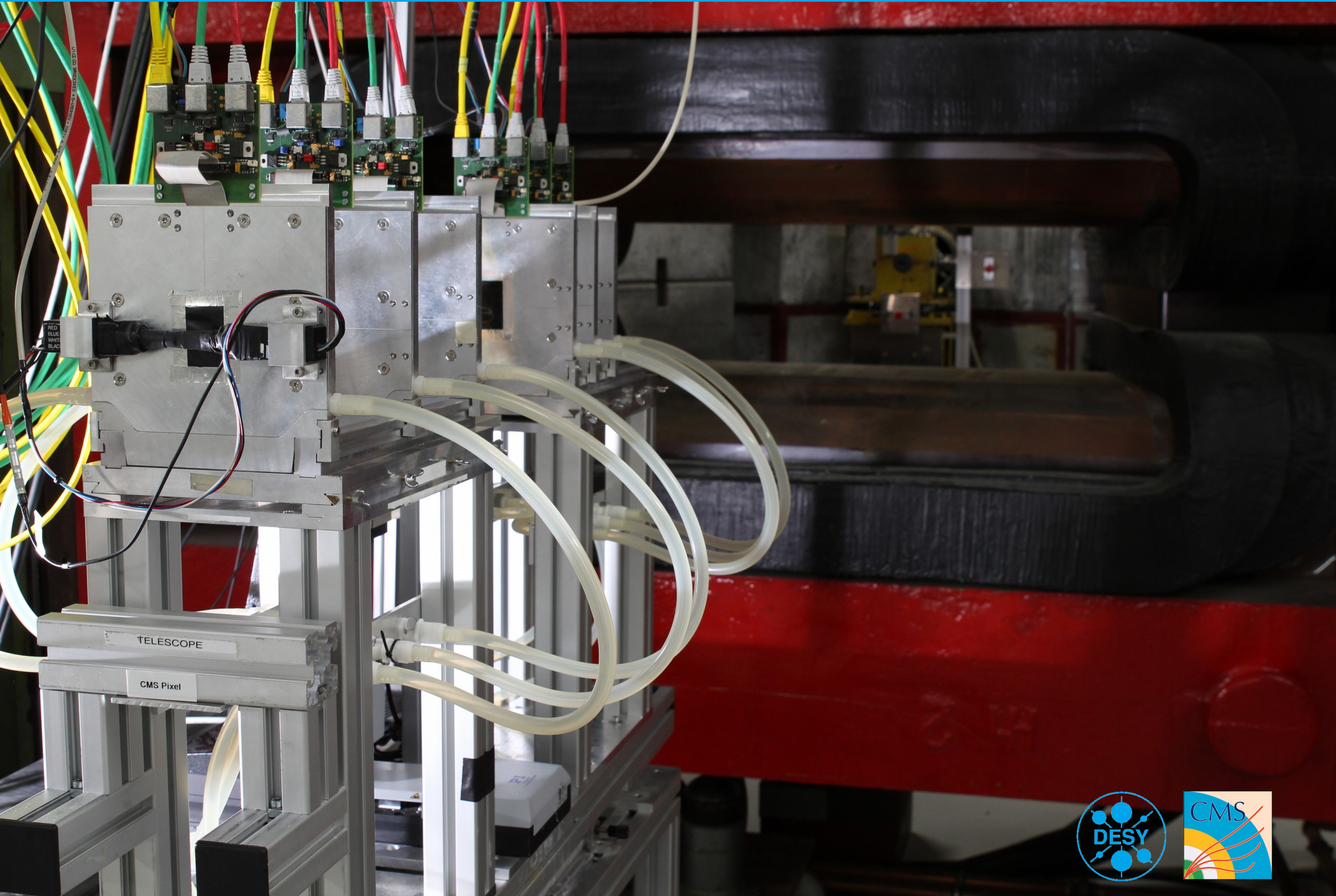
- 6.3 GeV e- primary beam
- 1 bunch at 1.024 MHz repetition rate
- Test beam generated via conversion



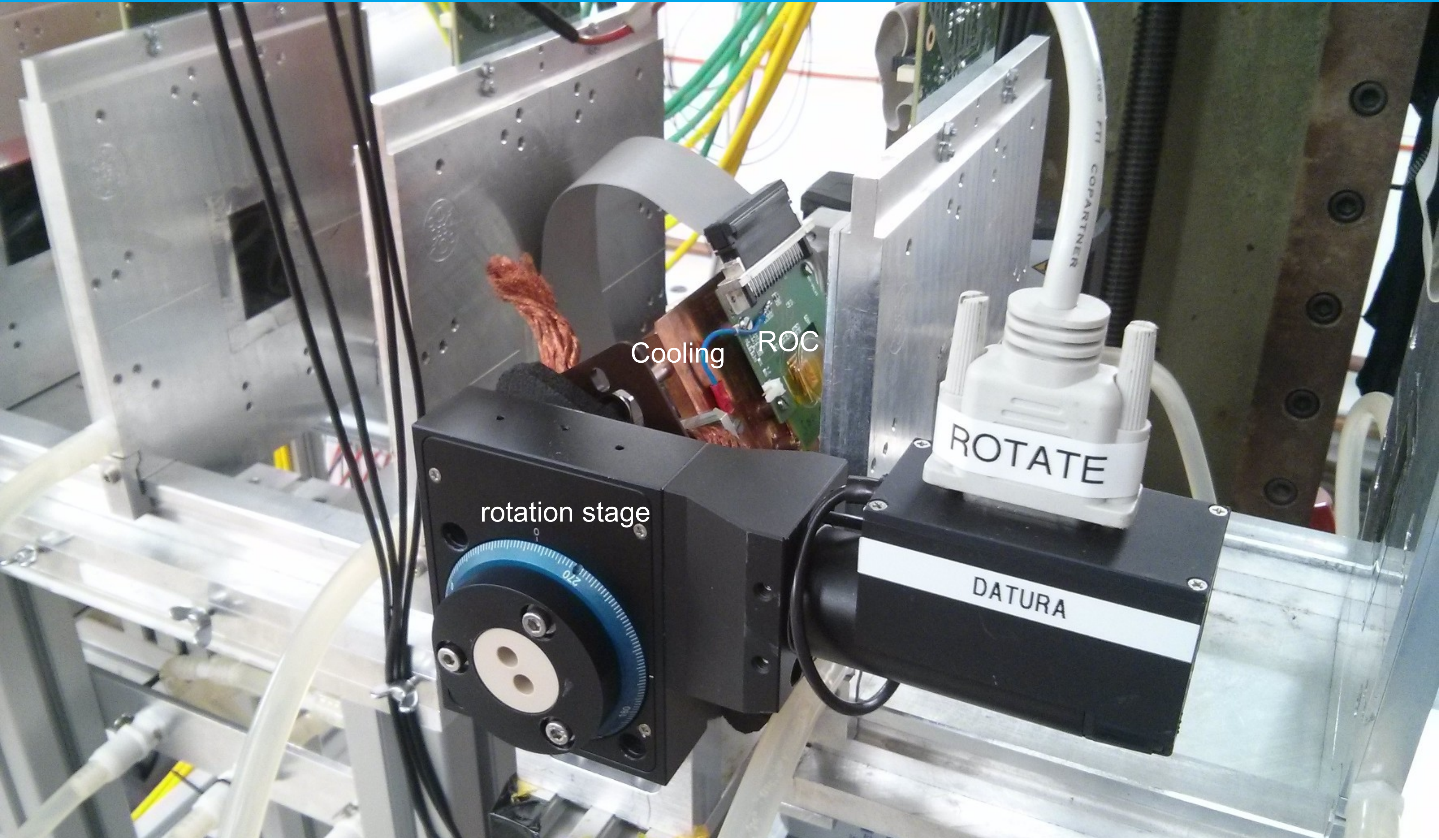
> Beam properties:

- 5% momentum spread
- 1 mrad angular spread, size ~10 mm
- Rate @ 2.4 GeV: 18 kHz
- Rate @ 5.6 Gev: 1.5 kHz

Beam Telescope: DATURA

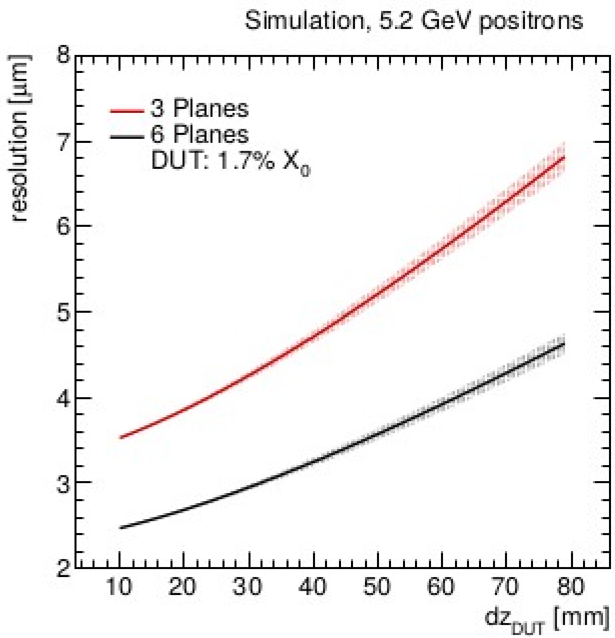


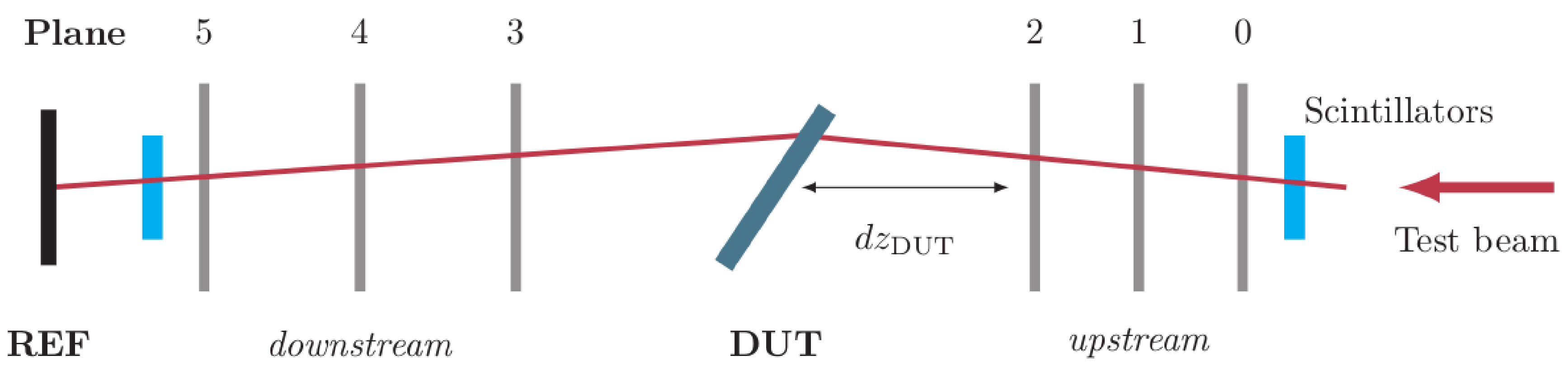
DUT Installation



Tracking and Alignment

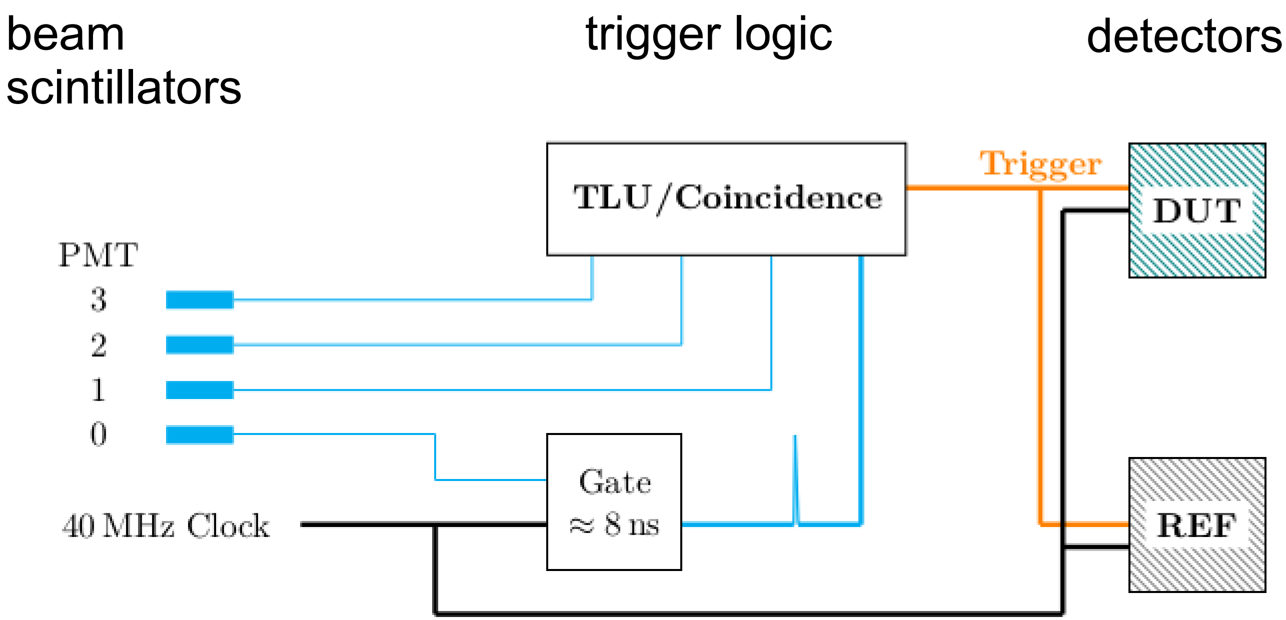
- DATURA telescope
  - 6 planes MIMOSA26, 600kPx each
  - Approx. 3.4 µm intrinsic resolution
  - Rolling shutter: 120 µs readout time
- Tracking: General Broken Lines
  - Take multiple scattering into account





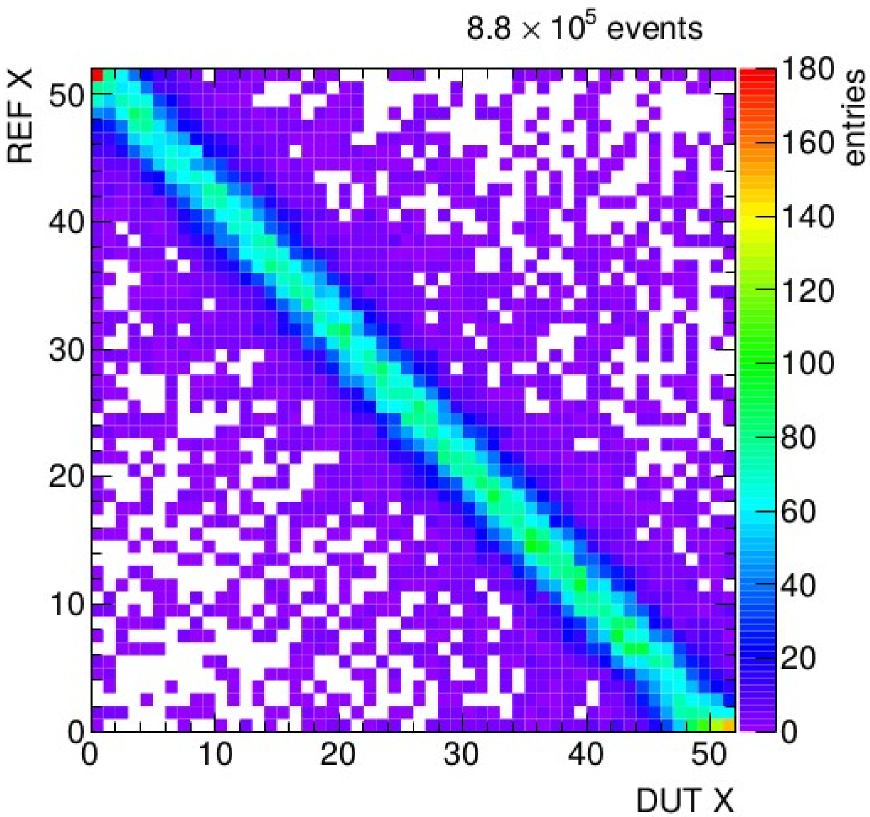
Triggering

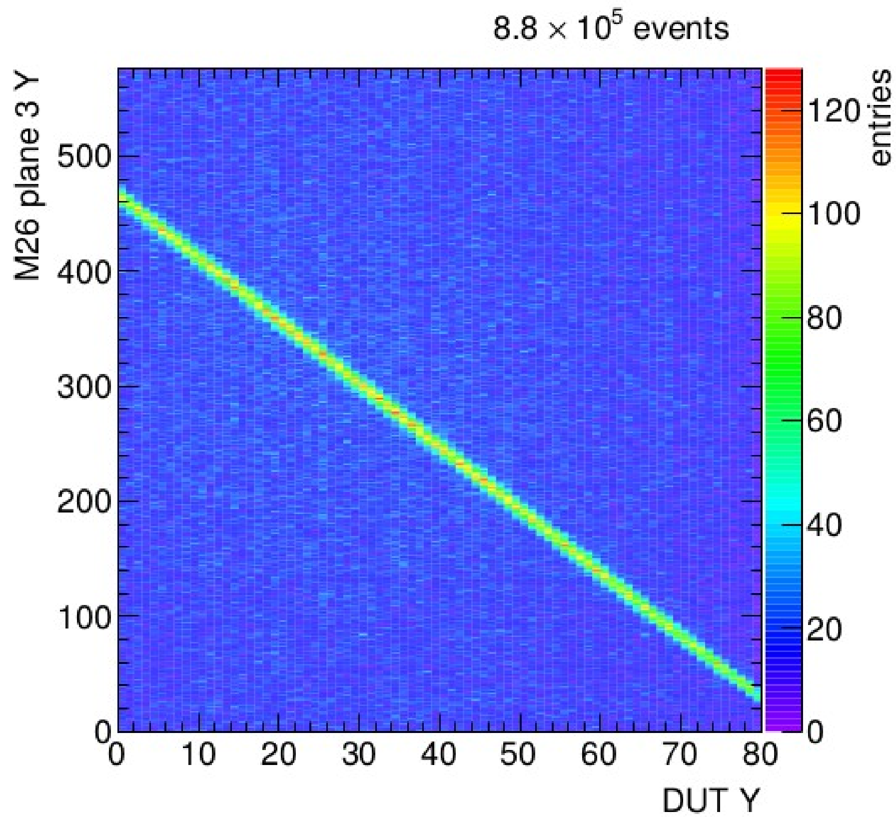
- No beam synchronous clock possible due to DESY-II re-syncs
  - No accelerator clock between fills, clock re-starts out of phase
- Using gate with independent 40 MHz clock
- Veto triggers arriving out-of-time



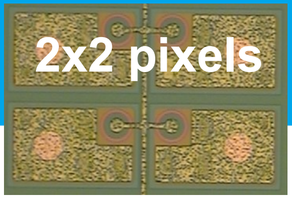
DAQ / Integration

- Fully integrated with EUDAQ
- Online monitoring available during data taking
- Correlations plots between CMS devices and telescope planes



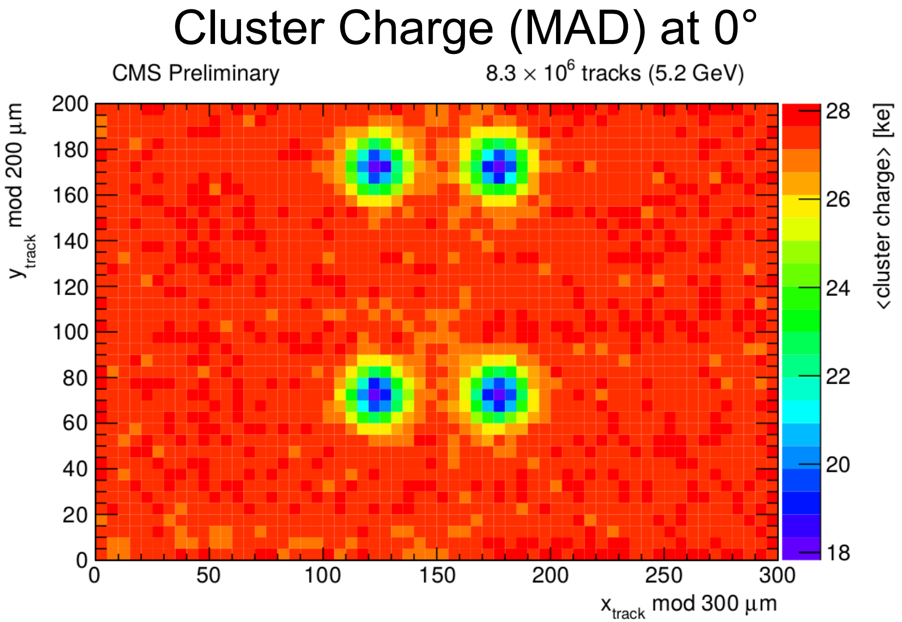


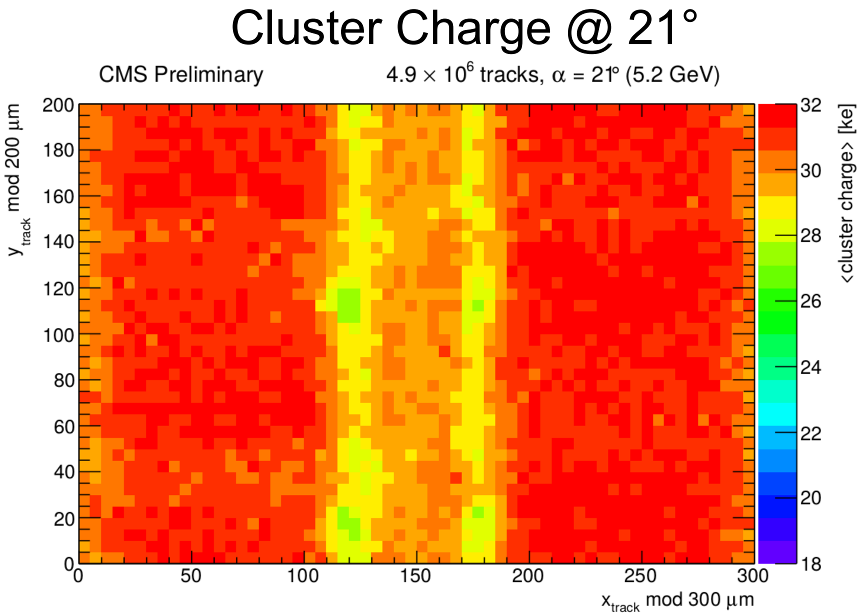
Charge Collection Efficiency



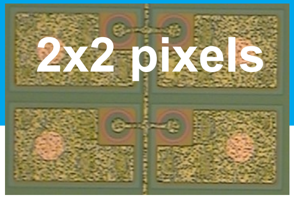
- Bias grid structure of the sensor visible at vertical incidence
- About 50% of the charge collected when “hitting the dot”

- In (more realistic) situation with Lorentz drift: track dip angle 21°
- Structure visible (smeared out), but only 10% charge lost

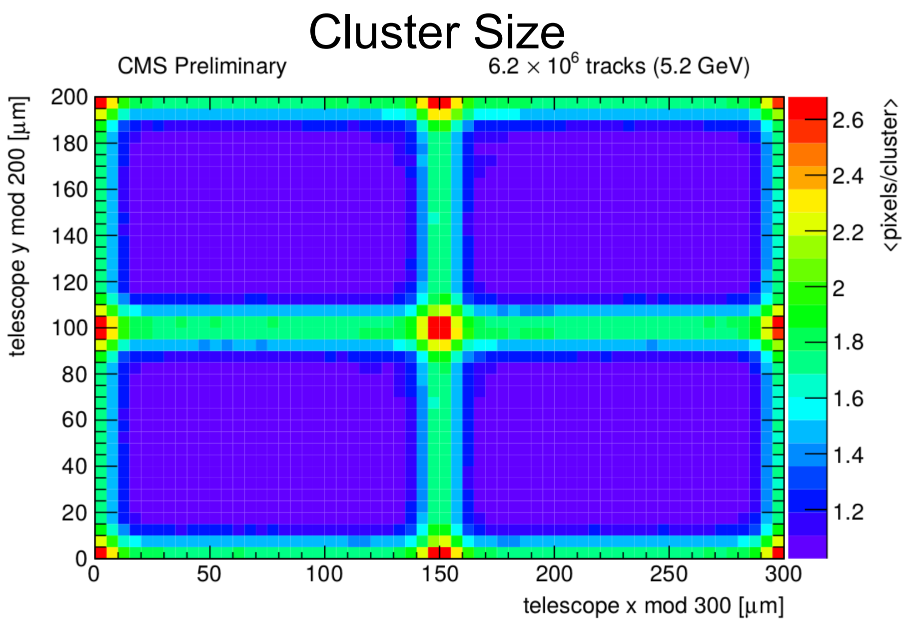


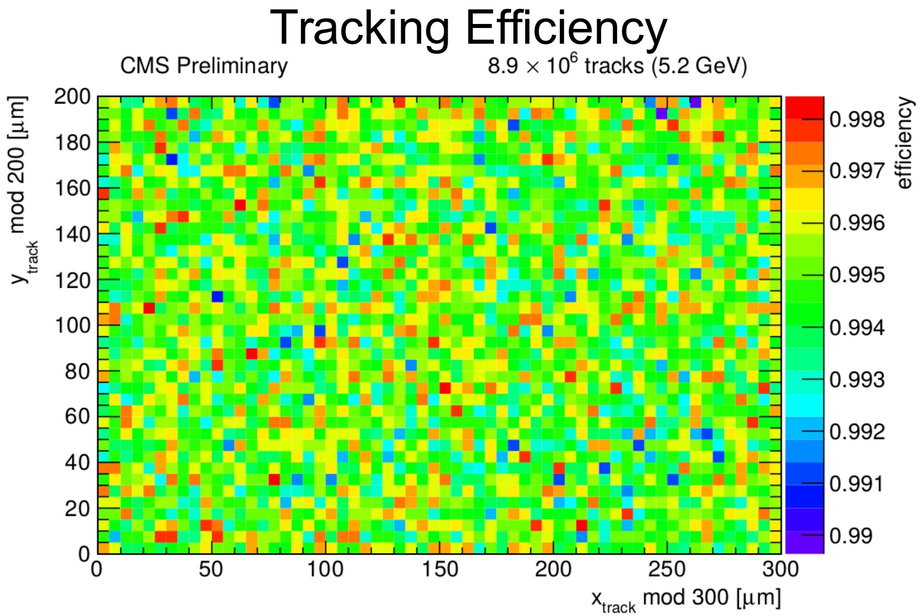


Cluster Size & Tracking Efficiency



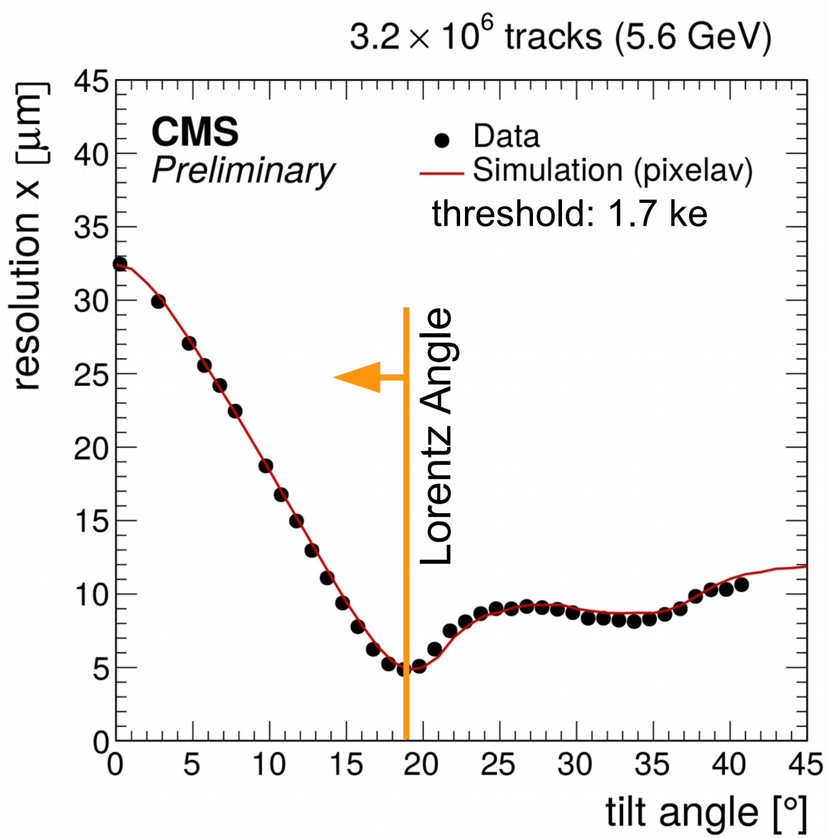
- Back to vertical incidence
- Cluster size maps the four pixel cells
- Tracking efficiency: **$99.7^{+0.3}_{-0.5}$ %**
- Even at vertical incidence no influence of charge deficiency visible

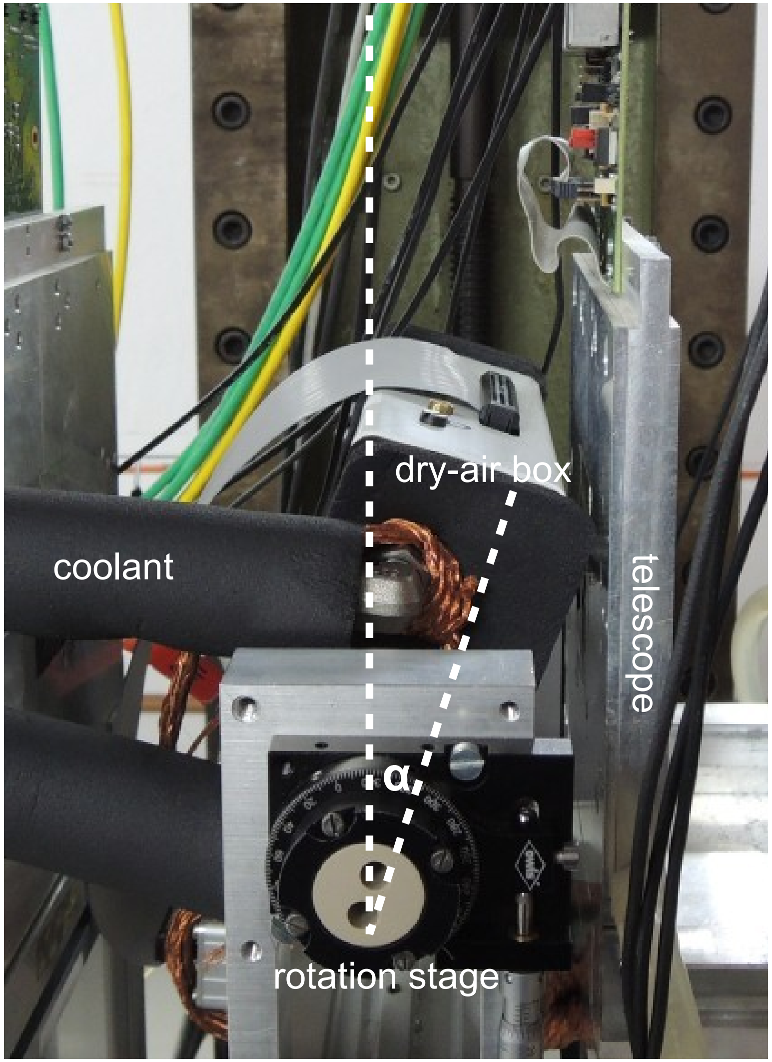




Spatial Resolution

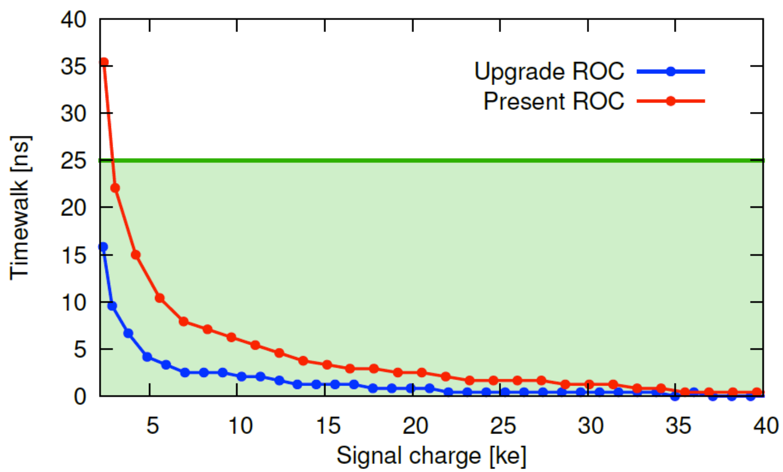
- Mimic Lorentz drift by rotating ROC
- Very good agreement with simulation
- Best resolution: **4.8 ± 0.3 µm**

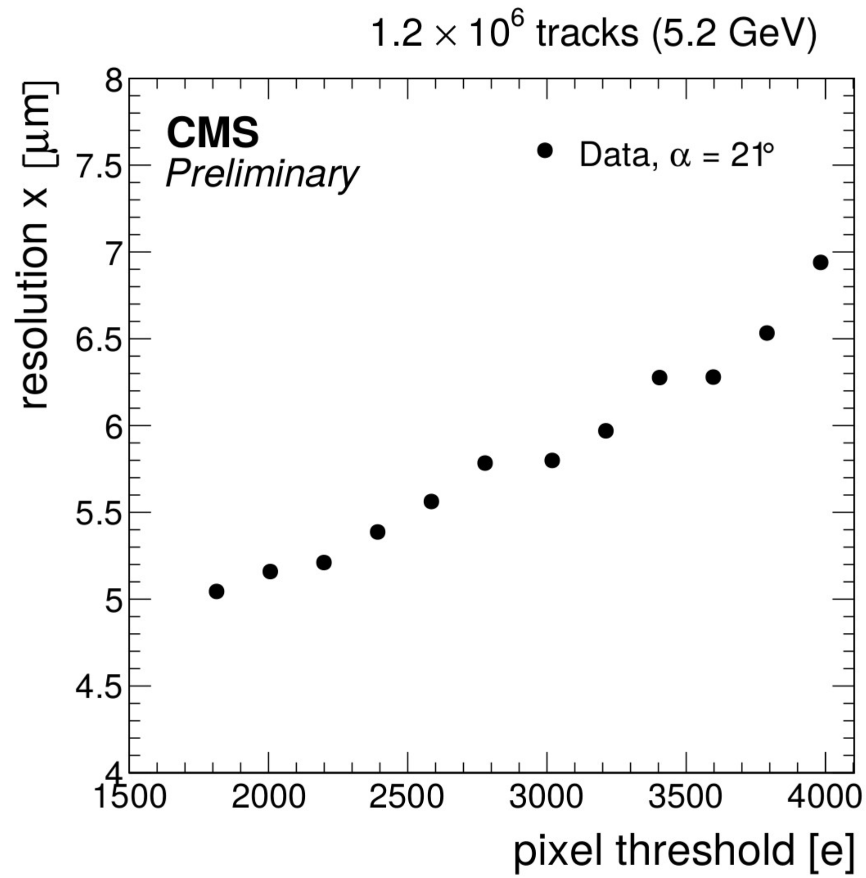




Analog Performance / Threshold

- Improved analog circuitry
- Lower absolute & in-time threshold **~1.5 ke**
- Current ROC:
  - 2.5 ke minimal threshold
  - 3.2 ke in-time threshold
- Reduced time walk due to faster comparator





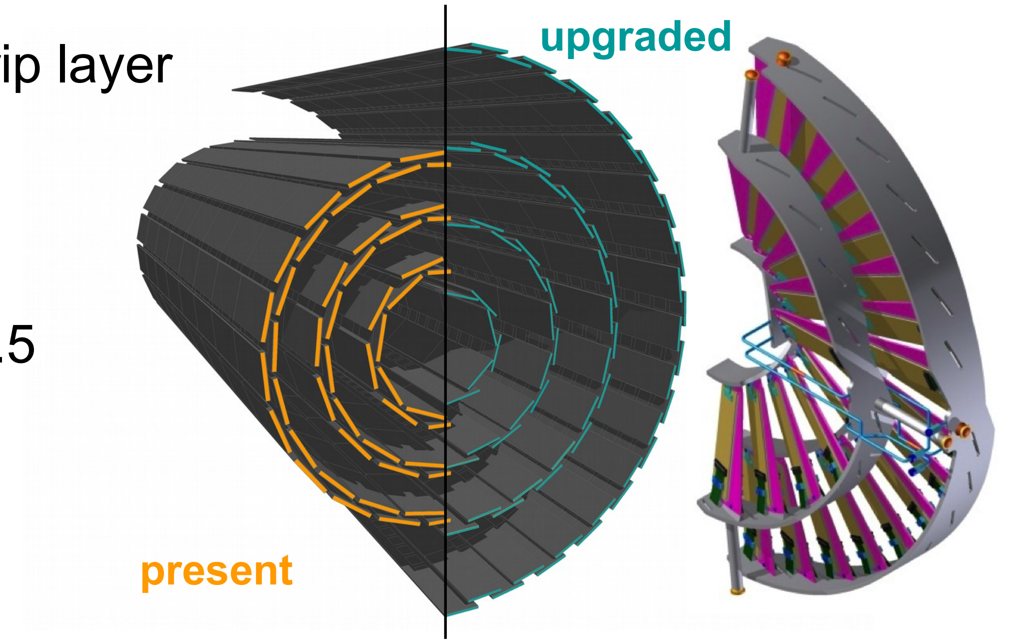
Summary

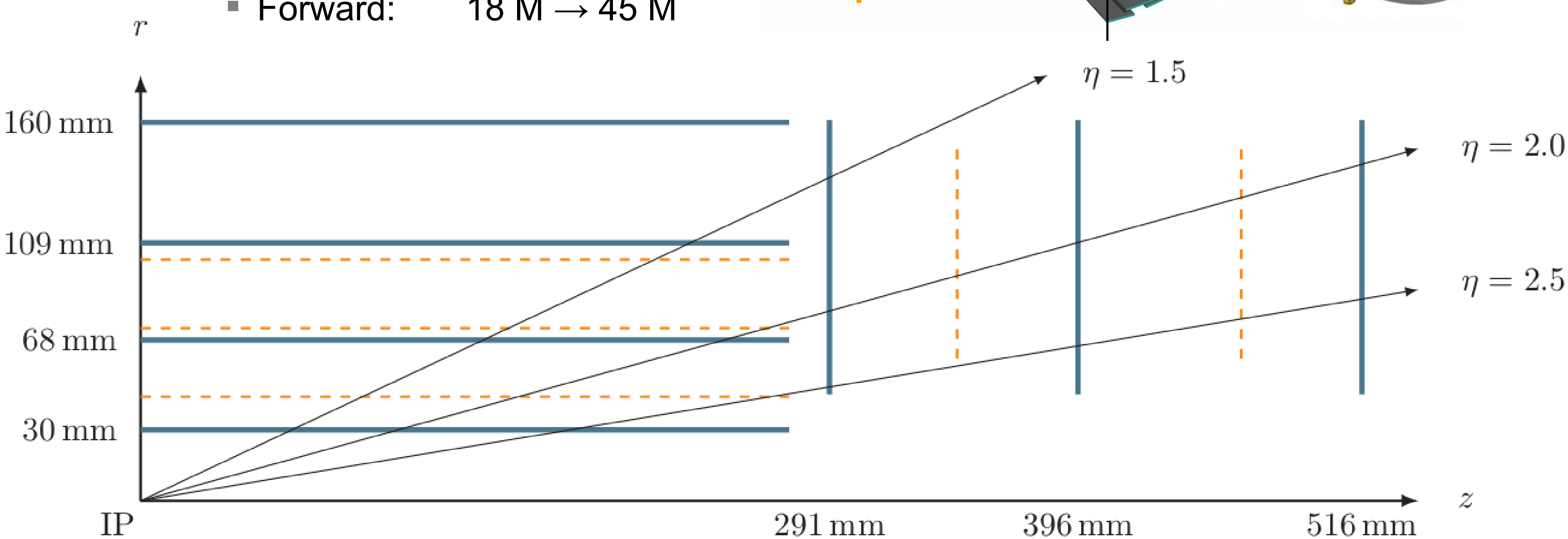
- Present CMS pixel detector will be replaced by Phase I pixel detector during extended LHC winter shutdown 2016/2017
- New front-end features
  - More data buffers
  - Faster data transmission
  - Lower in-time charge threshold
- Front-end design and performance verified in test beams
  - Position resolution: **4.8 ± 0.3 µm**
  - Tracking efficiency: **$99.7^{+0.3}_{-0.5}$ %**
- Detector module production ongoing
- Front-end for Layer 1 to be tested in the beam in March 2016

Backup.

From 3-hit to 4-hit tracking

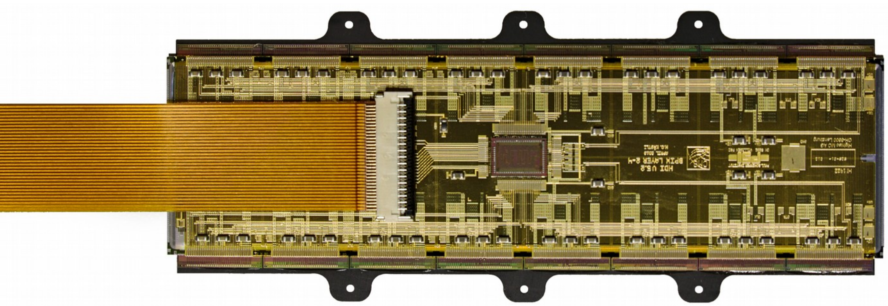
- Smaller extrapolation to first strip layer
- More robust 3-of-4 hit seeding
  - → **4 barrel layers, 2x3 disks**
  - → **4-hit coverage** up to |η| < 2.5
- Double number of channels:
  - Barrel: 48 M → 79 M
  - Forward: 18 M → 45 M



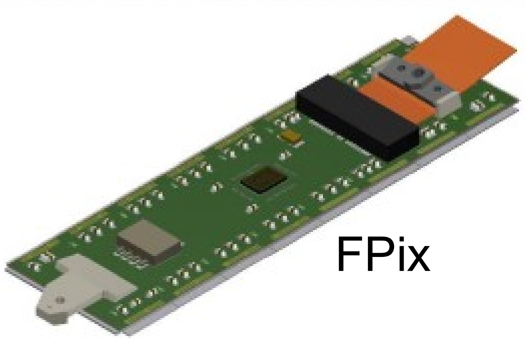


Detector Modules

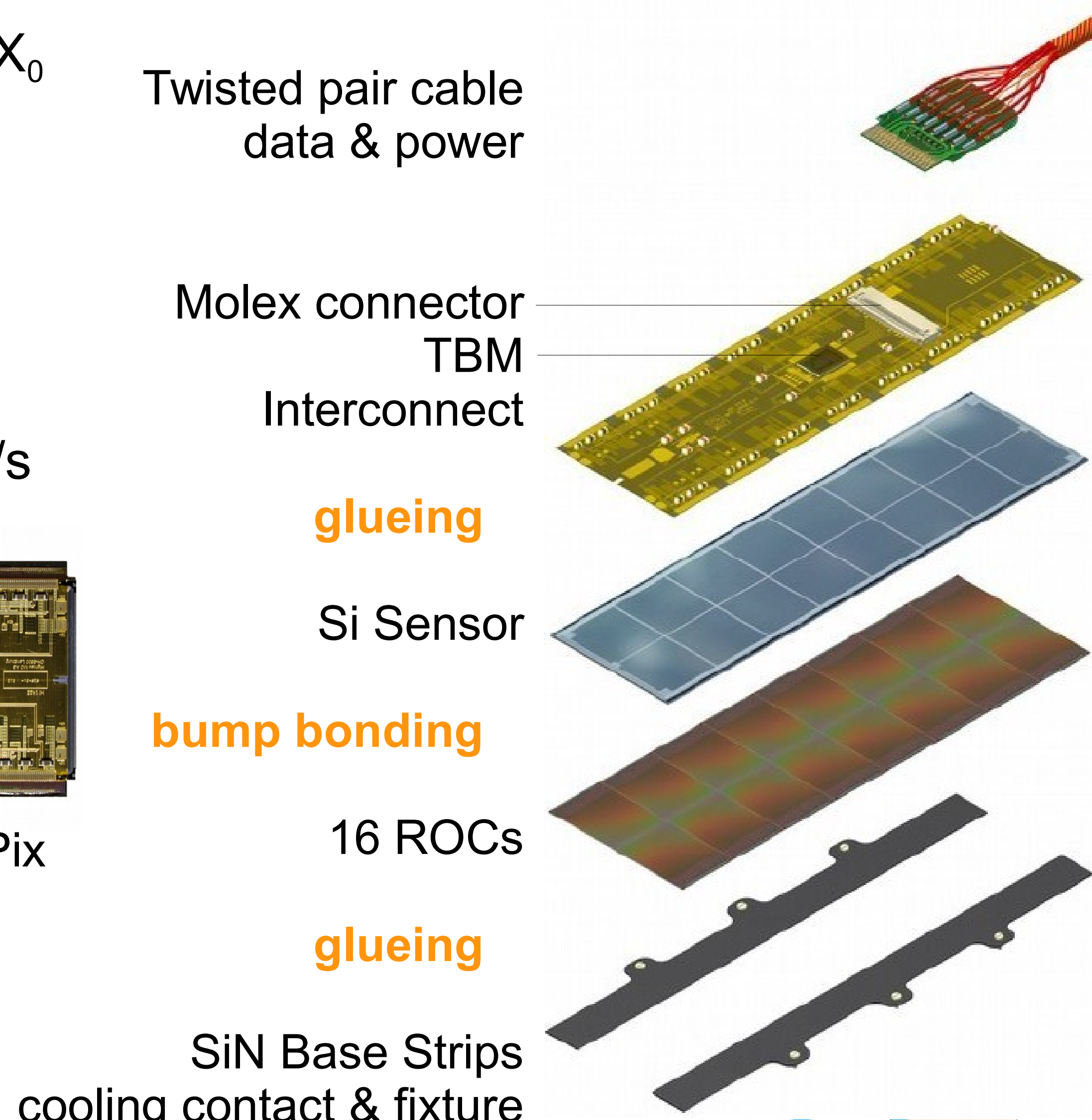
- Flex print interconnect, low X_0
- 16 Readout Chips (ROC)
- Token Bit Manager ASIC
  - Trigger & token control, readout coordination
- Module readout at 400 Mbit/s



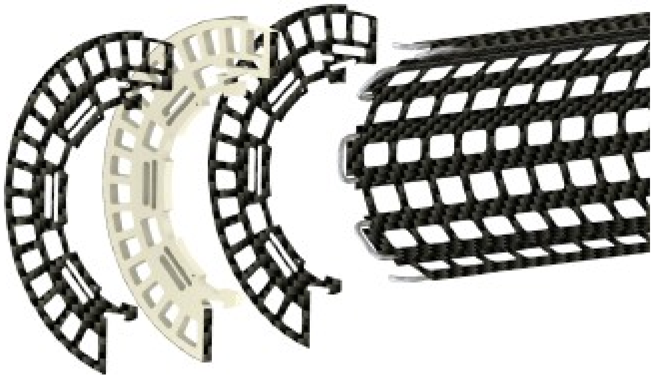
BPix



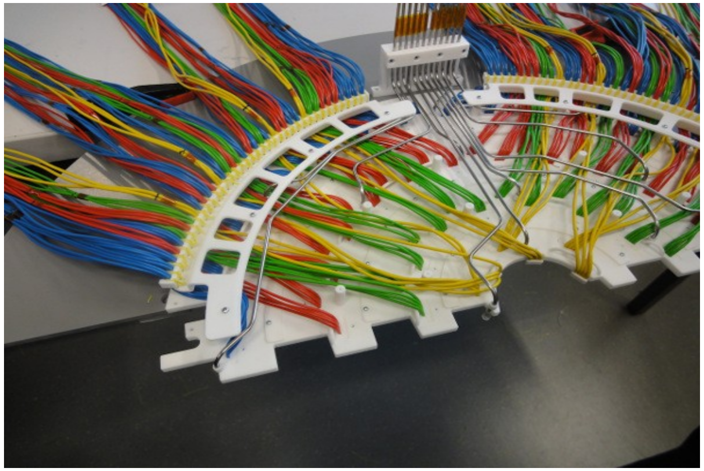
FPix



BPix Mechanics

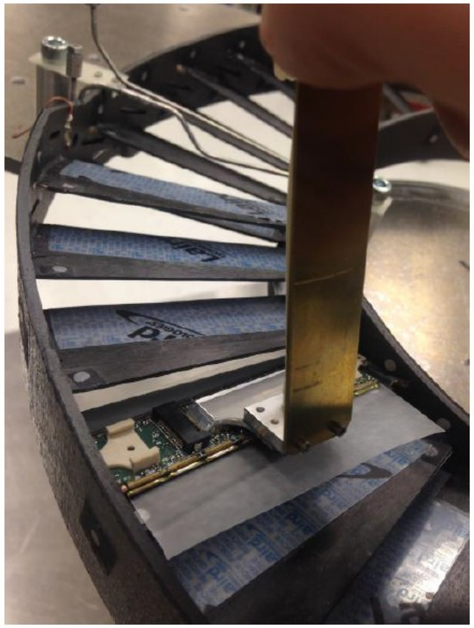


- Mechanics from Airex foam with carbon fiber sheets
- Stainless steel tubes, 50μm wall thickness
- Cabling mockup for routing of twisted-pair cables



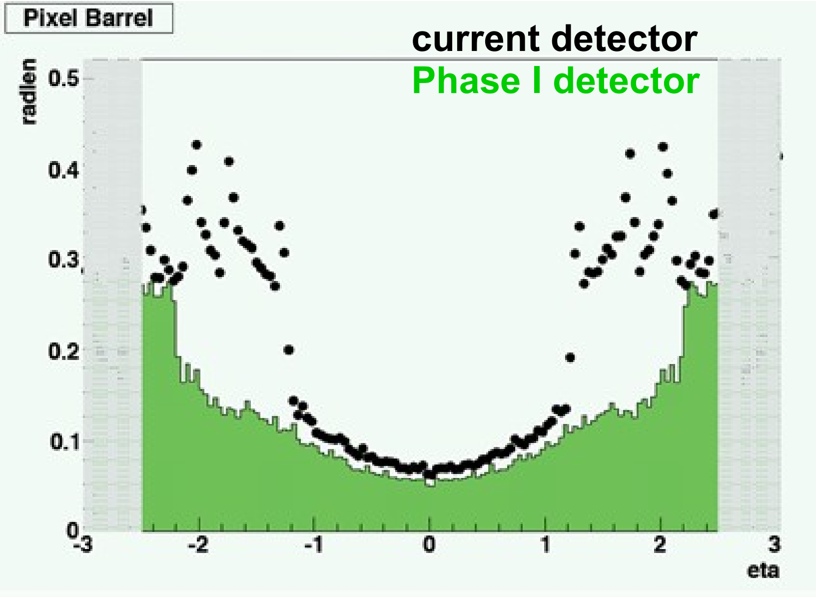
FPix Mechanics

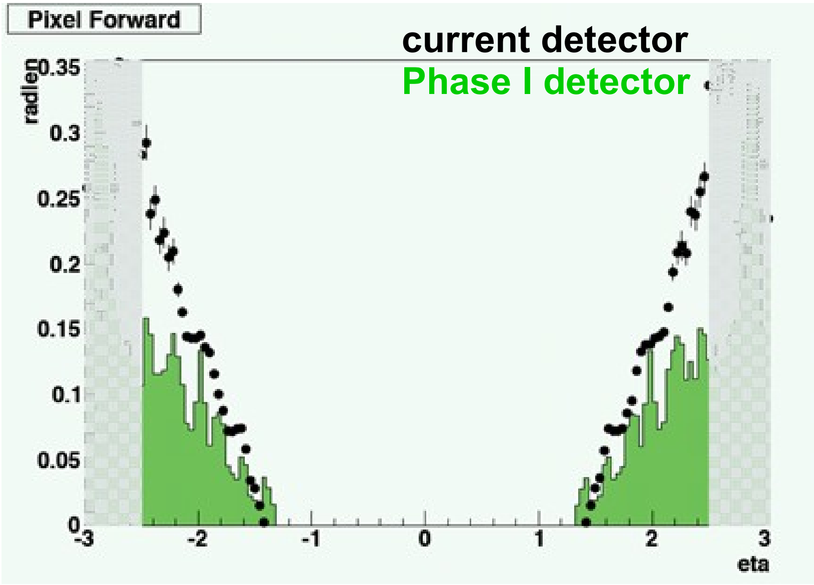
- Half disks consist of inner/outer blade assemblies
- Thermal Pyrolytic Graphite (TPG) blades
- Graphite ring with embedded cooling loops
- Prototypes produced, mounting exercised



Material Budget & Cooling

- Reduced mass (multiple scattering)
  - Better vertex resolution
- Lightweight carbon/graphite support
- 2-phase CO_2 cooling @ T = -20°C
  - Low coolant mass
  - Smaller cooling pipes (d = 1.6 mm)

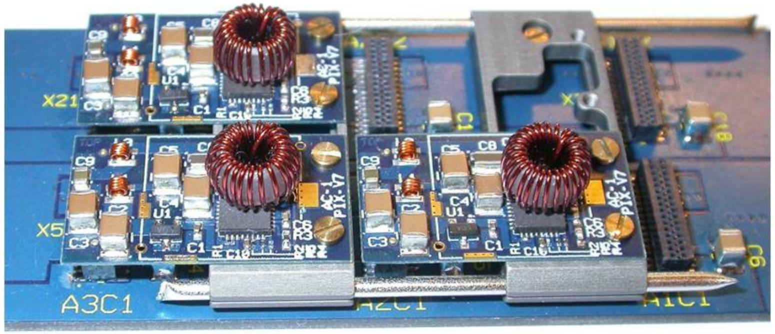


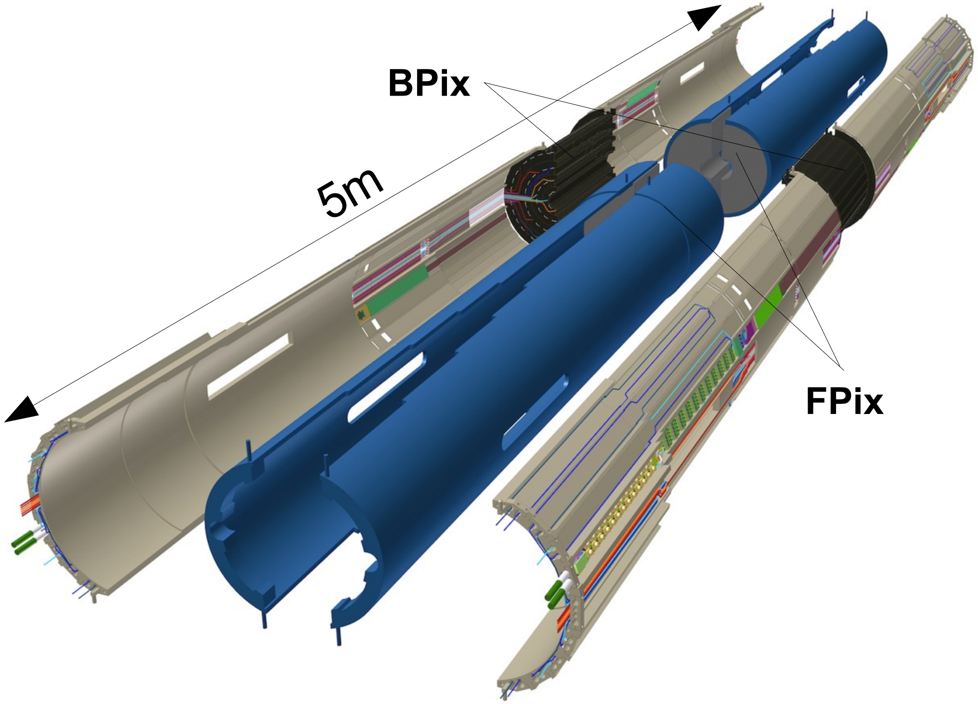


- Optimization of module rad. length X_0
  - Less passive SMD components
- Move service electronics out of tracking volume
- **Reduced mass despite add. layers**

Powering and Service Electronics

- Hosted on supply tubes, outside of the tracking volume
- Power distribution, optical converters, trigger and clock distribution
- **Poster by S. Hasegawa**

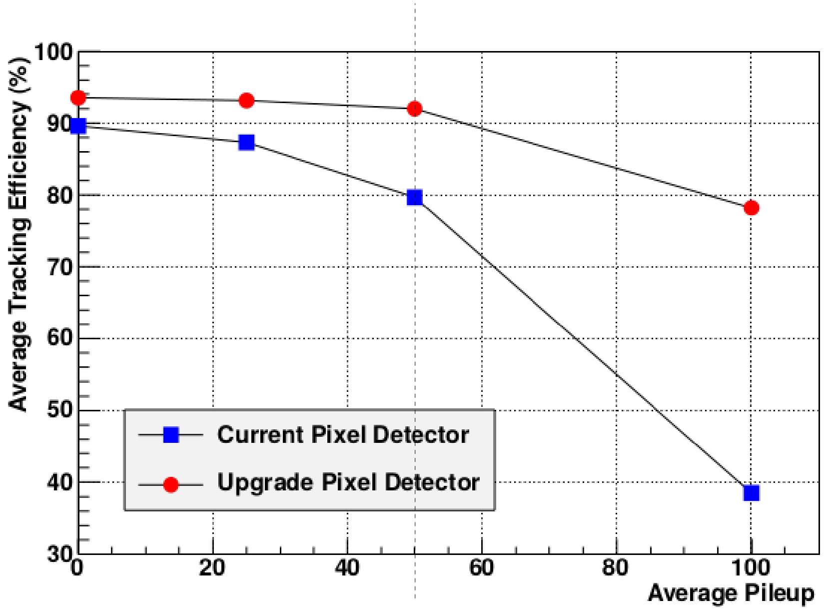


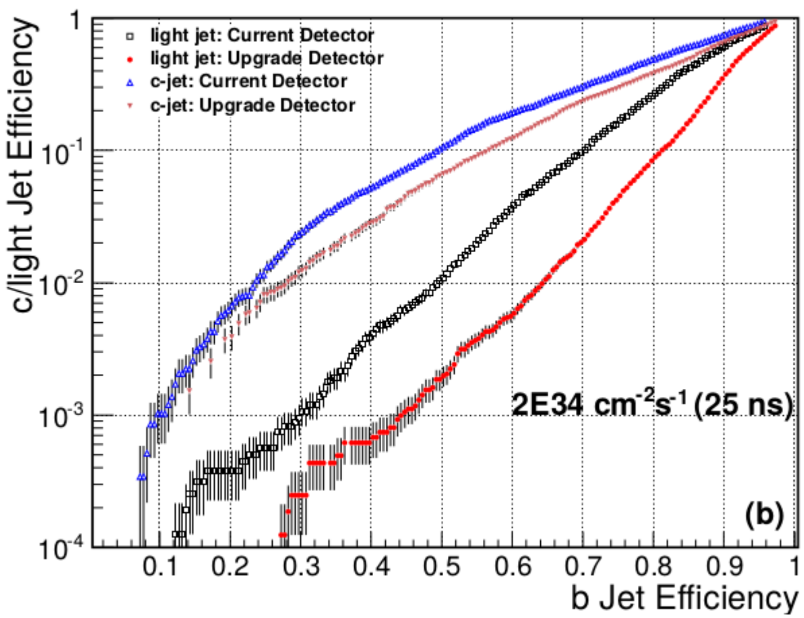


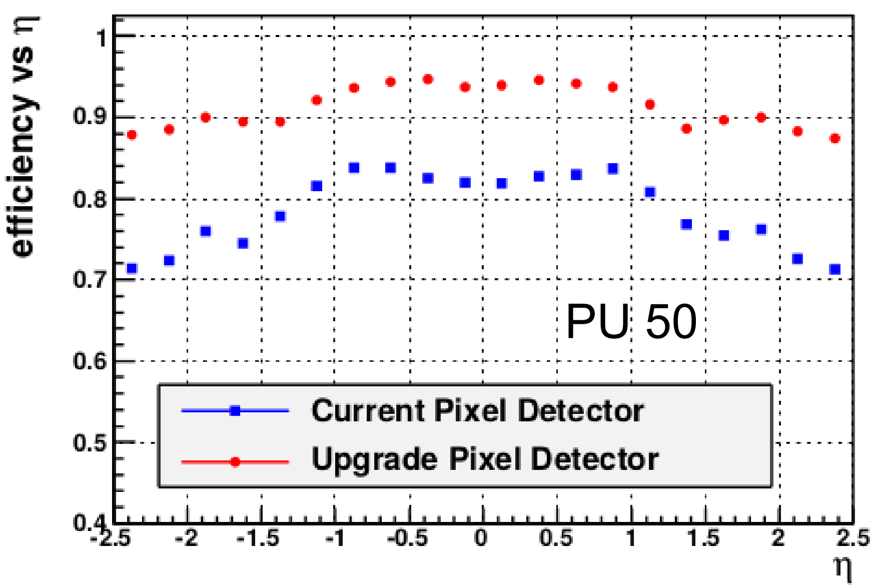
- Power distribution: **DC-DC converters**
- Generate analog & digital supply voltage on supply tube
- Allows to reuse existing power cables at higher voltage

Performance of the Phase I Pixel Detector

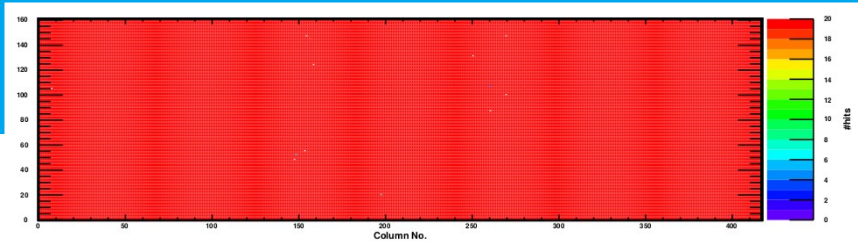
- Simulations based on expected data loss in the ROC
  - Inclusive $t\bar{t}$ sample @ 14 TeV
  - CSV algorithm
- Average tracking efficiency in η
- Tracking efficiency @ PU 50
- b-Tagging Efficiency



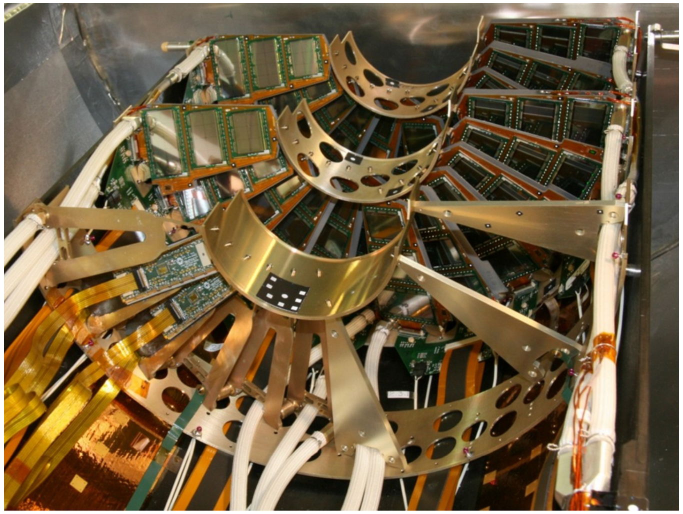




Module Production Status



- Five production centers
  - BPix detector: Switzerland, CERN/Taiwan/Finland, Italy, Germany
  - FPix detector: U.S. consortium
- Module Qualification: **Poster by M. Miñano Moya**
- Module production started Q2 2015, Layer 1 in summer 2016



- Pilot Blade operating in CMS

  → gain experience with system
- Integration starts end of 2015
- Commissioning & testing throughout 2016
- Installation in extended year-end shutdown 2016/2017

Phase I DAQ

- New uTCA-based DAQ system
- High-speed signal links with up to 10 Gbits/sec bandwidth

- Front-end drivers: 56 modules
- Slow control: 2 modules
- Detector control: 10 modules
- Clock&Trigger distr.: 6 modules

- Hardware development advanced, prototypes available
- Firmware development ongoing