AIDA 2020

Advanced European Infrastructures for Detectors at Accelerators

Status of AIDA-2020 Trigger/Timing Logic Unit (TLU)

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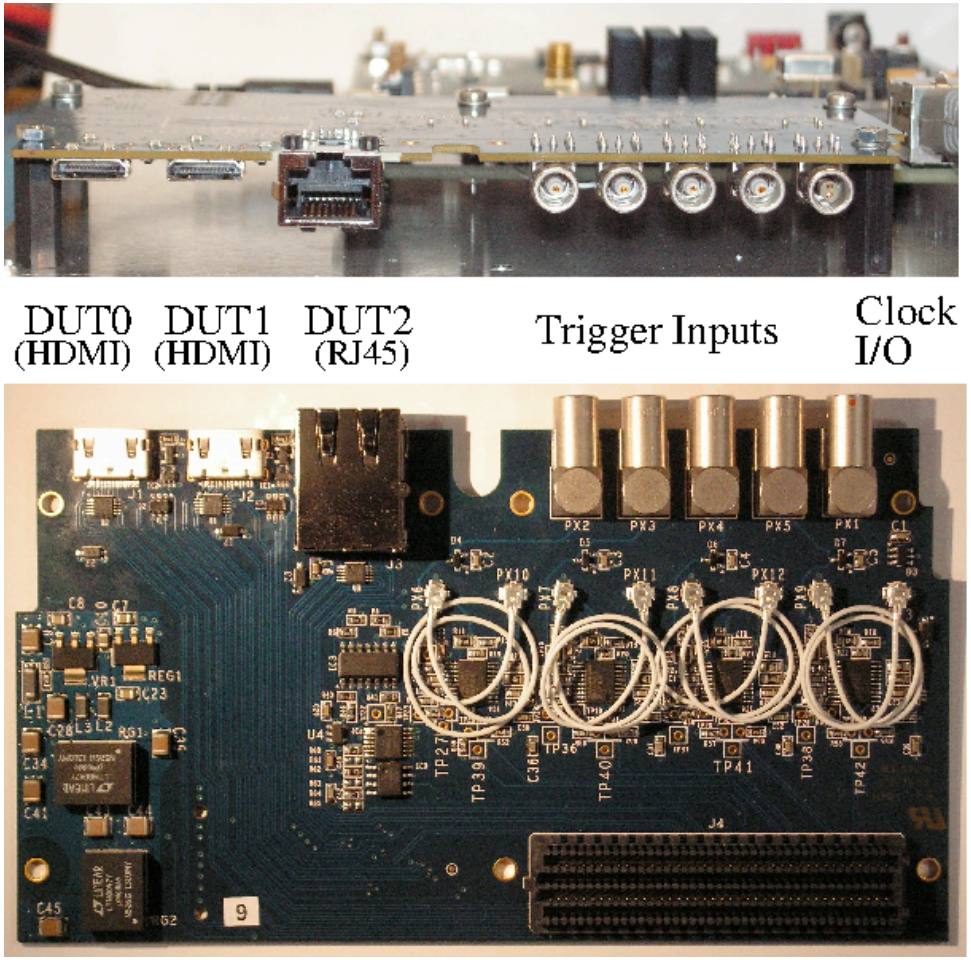
This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168.

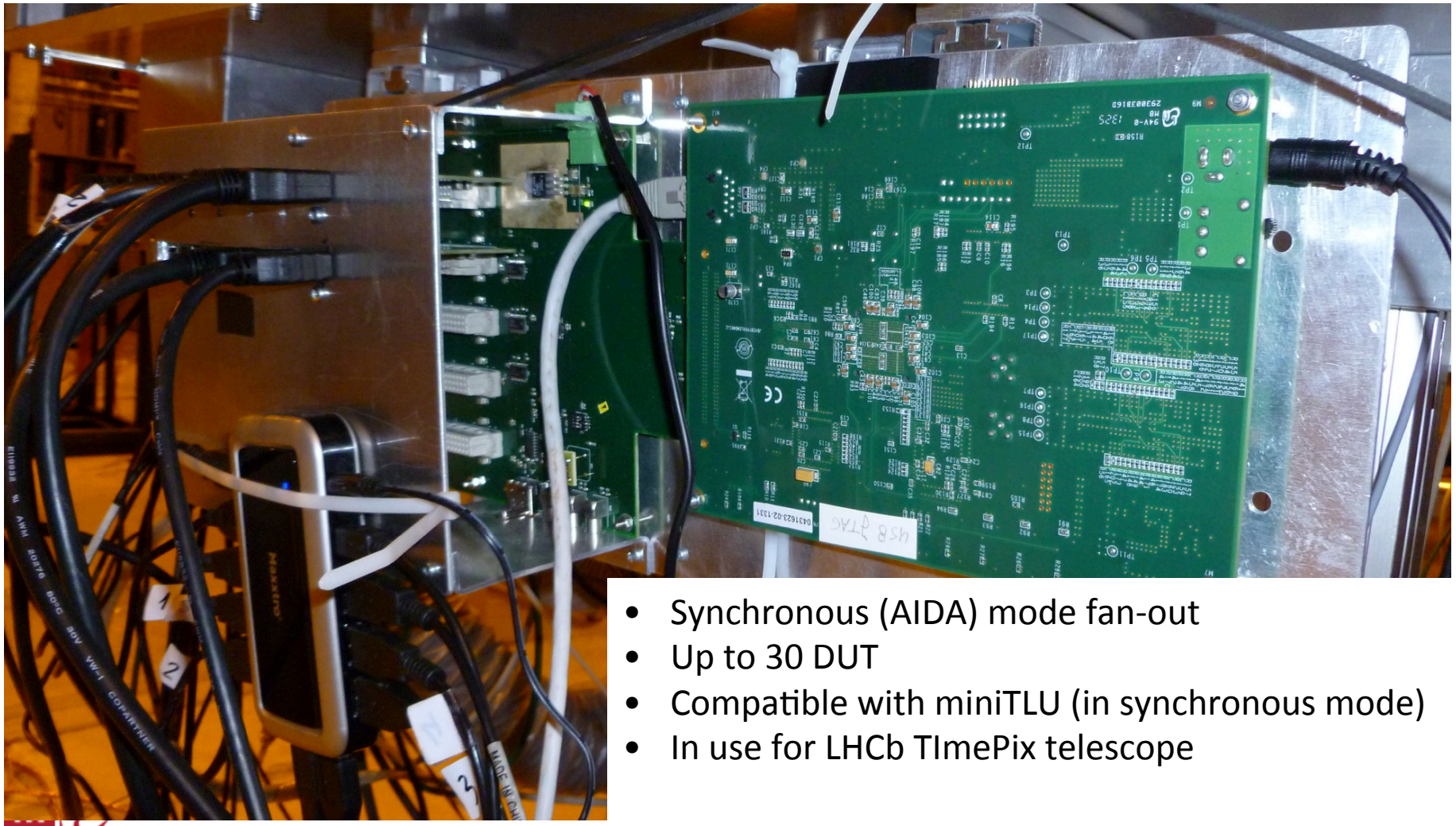
- **TLU Aims:**
  - Provide a hardware mechanism for synchronising multiple devices in a common beam test.
  - Provide easy interface to beam scintillators.
    - Simple easy to use
  - Backwards compatible (at interface level) with EUDET TLU.
- **TLU Status:**
  - ~30-45 EUDET TLUs in use and no spares left. 10 AIDA mini-TLUs made for testing.
  - Issues:
    - "Bug" in mini-HDMI connector pin-out
    - mini-HDMI has proven unreliable in use.

TLU Documentation

- **TLU Documentation**
  http://www.ohwr.org/projects/fmc-mtlu/
  - Hardware design
  - Firmware
  - Test scripts
  - (EUDAQ producer in EUDAQ source tree)



TLU Fanout



- Synchronous (AIDA) mode fan-out
- Up to 30 DUT
- Compatible with miniTLU (in synchronous mode)
- In use for LHCb TImePix telescope

Plans

- **Progress initially limited by available staff effort**
- **Effort is now increasing:**
  - ~20% of engineer at UCL started working January 2016 (Samer Kilani)
  - Recruiting physicist/engineer at Bristol to work 50% on AIDA-2020 (interviews 3/Feb/16)
- **Gather requests for AIDA-2020 mini-TLU.**
- **Produce batch of bug-fixed mini-TLUs for distribution Q2/2016.**
  - Cost basis to be decided. WP5 has funds for "full" TLUs installed in beam-lines as AIDA-2020 deliverable, but not mini-TLU.
- **Tests to perform:**
  - Chain CALICE CCC and one or more mini-TLU to check for stability of clock ("jitter peaking")
  - Test timing precision of TDCs with beam particles.
- **Design and produce full TLU—more trigger inputs for DUT interfaces (AIDA-2020 WP5 deliverable)**

mini-TLU Likely Changes

- **Abandon strict conformity with FMC standard outline.**
  - Existing mini-TLU a double-height FMC. Described in standard, but didn't fit on many low cost FPGA carrier boards.
  - Following FMC standard outline limits use of full-size connectors.
  - Can still use a uTCA AMC format FPGA board, just not plug it into a crate
    - E.g. Many CERN GLIB boards used on bench as FMC carrier boards.
- **Full-size (more robust) HDMI connectors rather than mini-HDMI.**
  - Have heard that micro-HDMI acceptable
  - Many need to add cable supports to front of mini-TLU enclosure if using full size cables.

mini-TLU Likely Changes

- **Ability to accept clock from CALICE CCC or LHCb Timepix clock/sync fan-out on standard HDMI cable**
  - Instead of hand-made custom cables with clock separated from trigger/busy/sync
- **Use jitter–reducing PLL chip (Si53xx) to generate/receive clocks**
  - Sophisticated PLL circuit with adjustable parameters should reduce likelihood of clock instability if chaining TLUs or using TLU as slave from high-jitter clock.
- **Move from Spartan-6 to Artix-7 as default host FPGA**
  - Avoid risk that Spartan-6 becomes difficult to obtain towards end of AIDA-2020
  - Better performance of TDC

Firmware status

- **Switch between synchronous (AIDA) and asynchronous (EUDET) interface modes implemented.**
  - Not tested
- **Asynchronous mode:**
  - Trigger (TLU→DUT)
    - Fixed latency from scintillators to trigger. Jitter ~ 3ns sigma (cf. 20ps from EUDET TLU).
  - Busy (DUT→TLU)
  - Optional clock from DUT to clock out trigger number
  - No common clock between systems
- **Synchronous mode:**
  - Trigger (TLU→DUT)
    - Synchronous with clock
  - Clock (TLU→DUT)
    - Typically 80MHz, 40MHz, 20MHz, 10MHz or 5MHz
  - Busy (DUT→TLU)

Mini-TLU production

- **AIDA-2020 covers cost of supplying "full" TLUs to beam test areas.**
  - Assumption - One per AIDA-2020 supported telescope.
- **Cost of Mini-TLU not covered by AIDA-2020**
  - Production of first mini-TLU under AIDA programme funded by DESY, not AIDA
- **Plan to produce mini-TLU "at cost"**
  - Negotiating with our administration to see if we have to add staff-effort
- **Cost likely to be ~ €1000 - €2000**
- **Design and firmware are (and will remain) Open**
  - You are welcome to make one or more yourself if you wish…..
- **Aiming for production end of Spring 2016**
- **Please let me know if you are interested in first batch.**