Freiburg Lectures 2016

Graduiertenkolleg "Mass and Symmetries after the Discovery of the Higgs Particle at the LHC"

Tracking and Tracking Detectors

Norbert Wermes
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Outline

Lecture 1

Tracking

- momentum measurement
- vertex measurement
- influence of multiple scattering
- errors and what to do …

Lectures 2 & 3 & 4

Tracking Detectors

- the signal and the noise
- spatial resolution with structured electrodes
- gaseous detectors
- semiconductor detectors
- pixel detectors ... status and future

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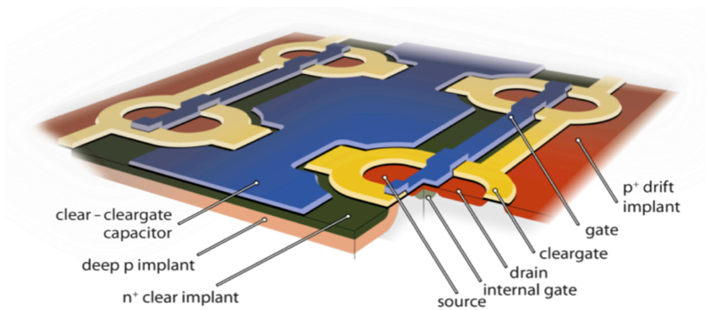
Lecture 4

Tracking Detectors (Pixels: Status and Future)



Norbert Wermes
University of Bonn

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SI LAB
Silizium Labor Bonn

Content Lecture 4

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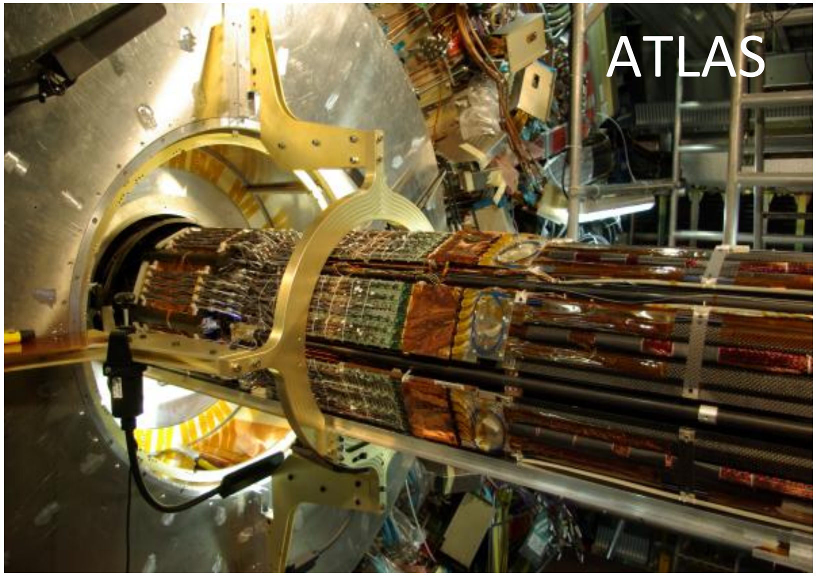
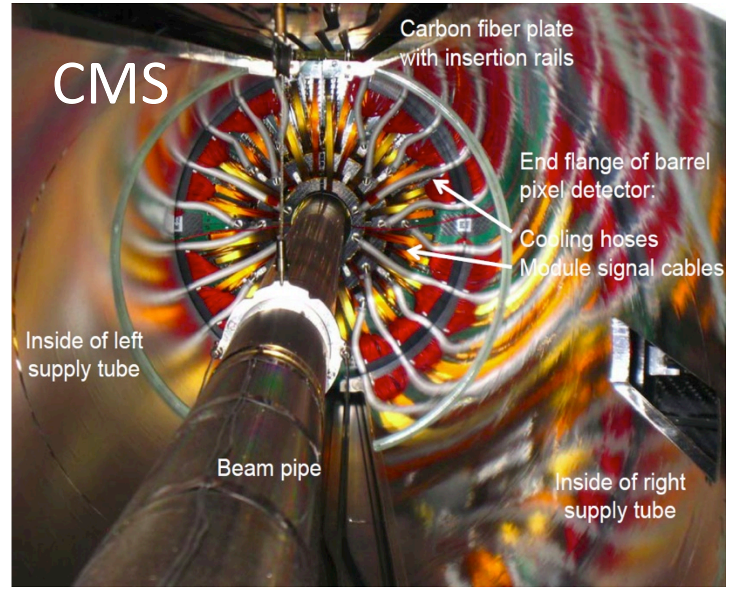
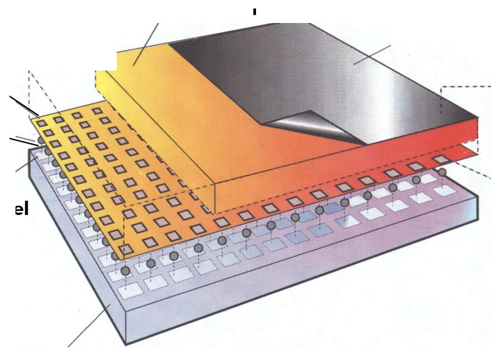
- Other semiconductor materials
- Hybrid Pixel Detectors
- What the Readout Chip has to do?
- From parts to modules (bump bonding)
- New sensor types 3D-Si, Diamond
- Noise in ionization detectors
  - Don't be afraid about noise theory!
  - When to care about noise?
  - Noise sources in a typical detector system
  - Calculating the noise of a detector (pixel/strip) system
- How to make things better?
  - Radiation hard sensors and electronics
- Monolithic Pixel Detectors
  - DEPFET Pixels
  - MAPS
  - Depleted CMOS Pixels (DMAPS)
- 4D – Timing resolution with Silicon Detectors

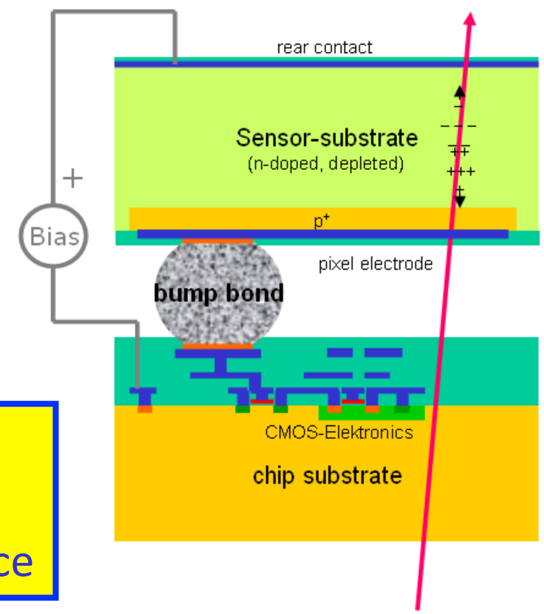
Today's "state of the art" of running detectors



all based on
"Hybrid Pixels"





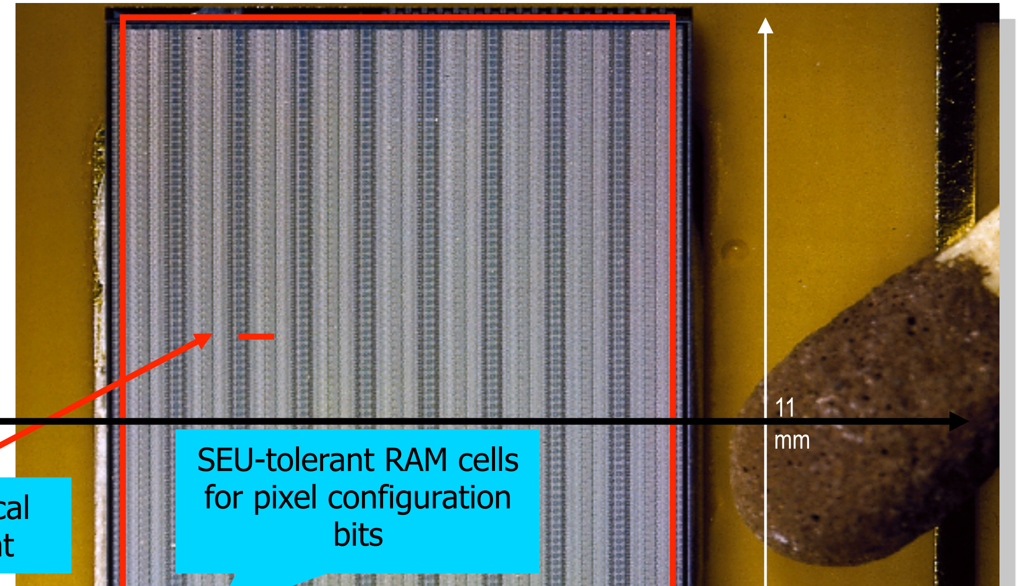


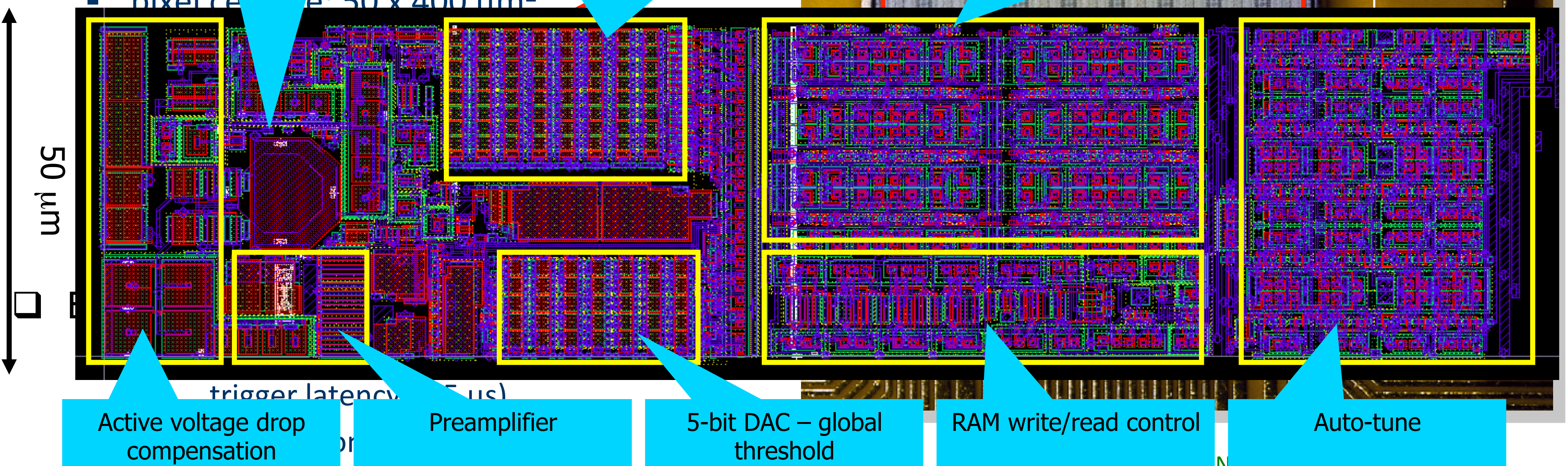
- amplification by a dedicated R/O chip
- 1-1 cell correspondence

Important: Readout Chips (ASICs)

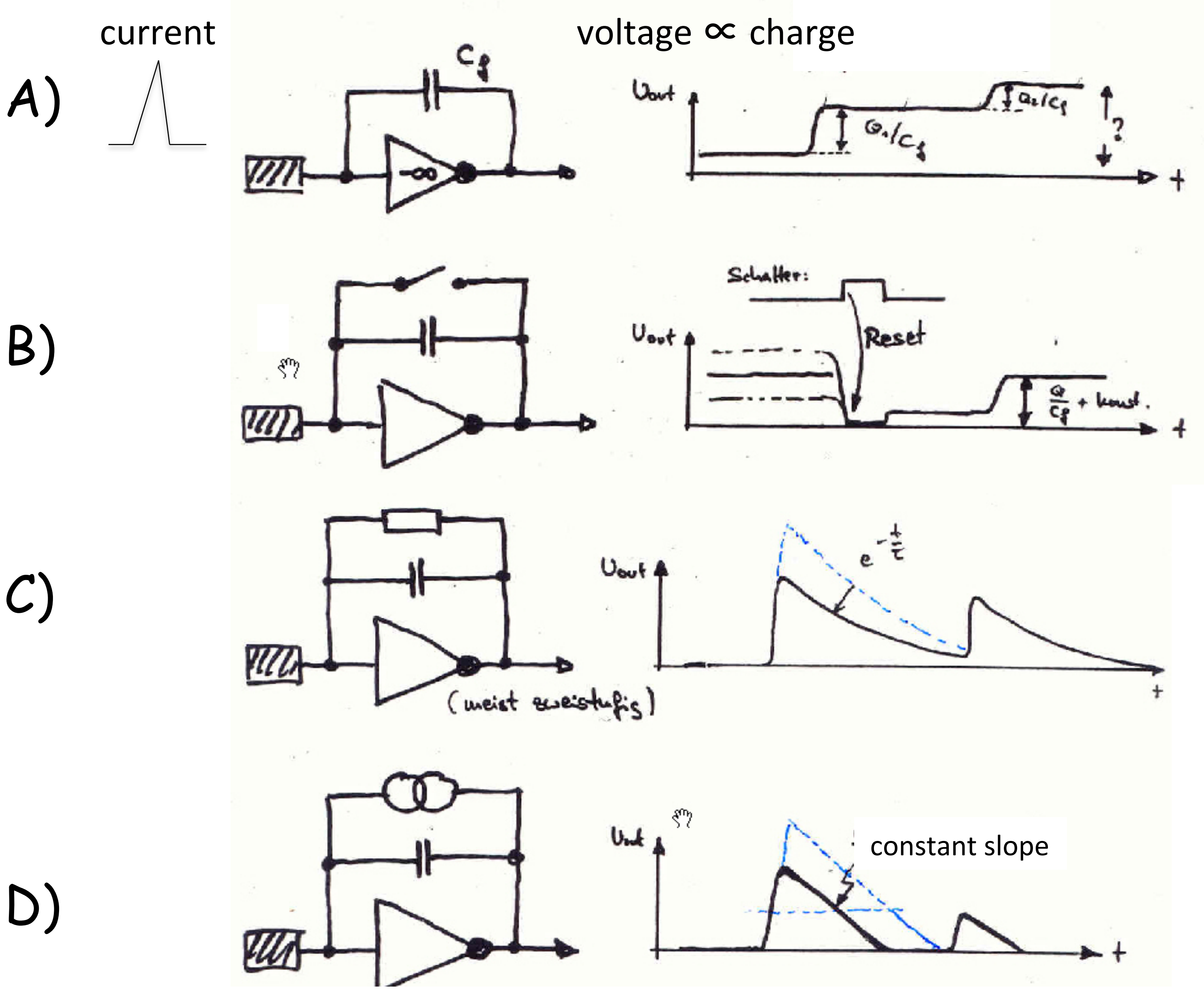
- becomes integral part of the detector
  - micro electronics
  - up to 700 million transistors so far
  - development takes typ. 10 man years

- ATLAS FE-I3
  - 0.25 µm CMOS technology

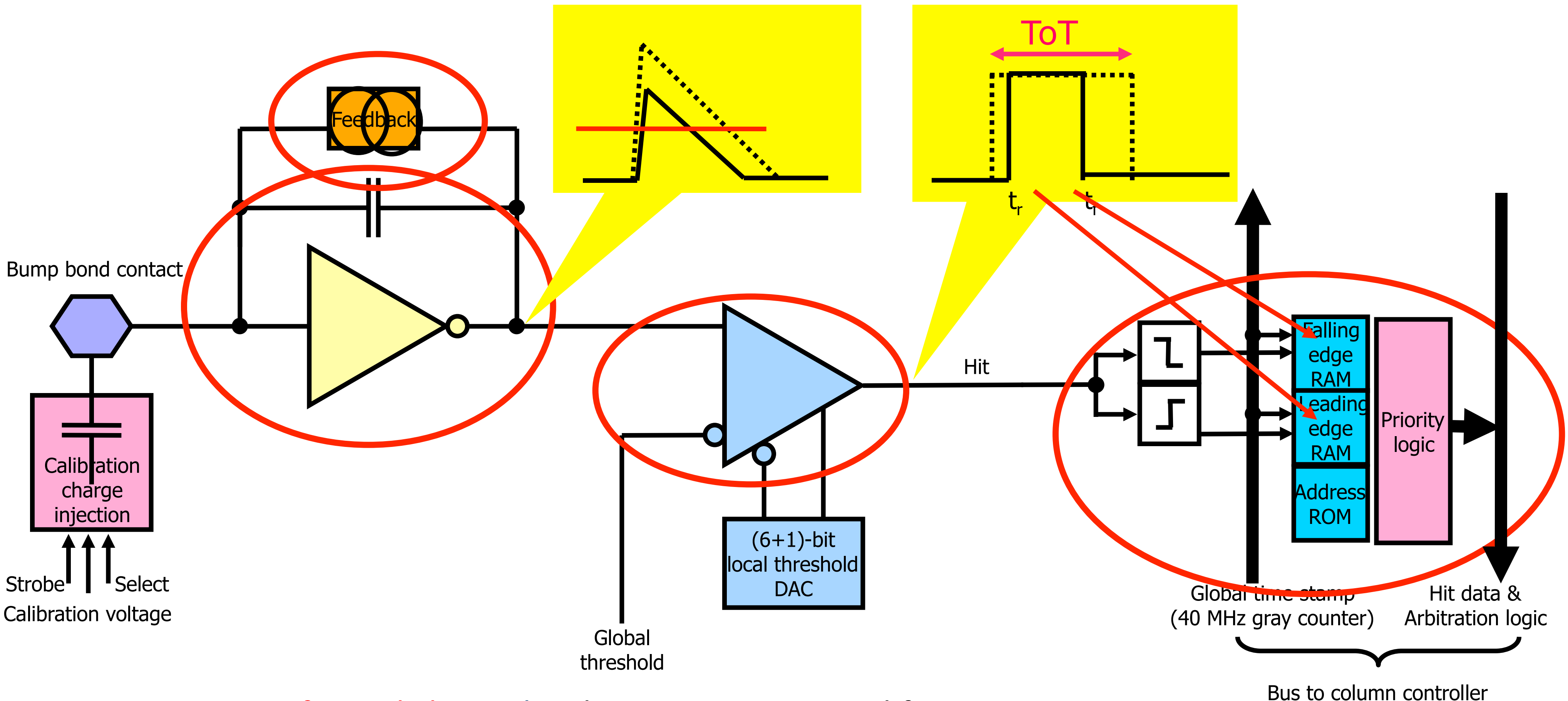




Charge Sensitive (Pre)-Amplifiers



Functions in the cell (binary readout + „poor man's" analog)

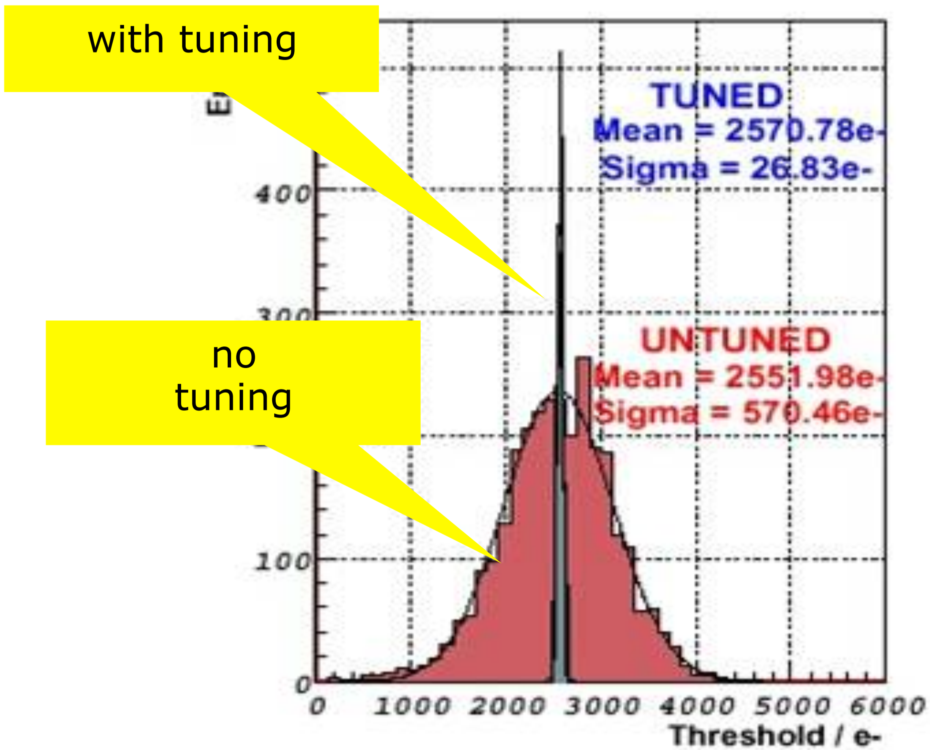


- Integration of signal charge by charge sensitive amplifier
- Pulse shaping by feedback circuit with constant current feed back
- Hit detection by comparator
- ~5 bit analog information via „time over threshold"
- storage of address and time stamps in RAM at the periphery

L. Blanquart et al., NIM-A565:178-187, 2006

Requirements on the electronics performance

- small noise hit rate → low noise and small threshold dispersion
- $\sigma_{noise} \oplus \sigma_{threshold}$ < ~ 600 e^- @ a threshold of 3000 e^-
- time stamp < 20 ns after BX for all signal heights



Distribution of pixel cell thresholds

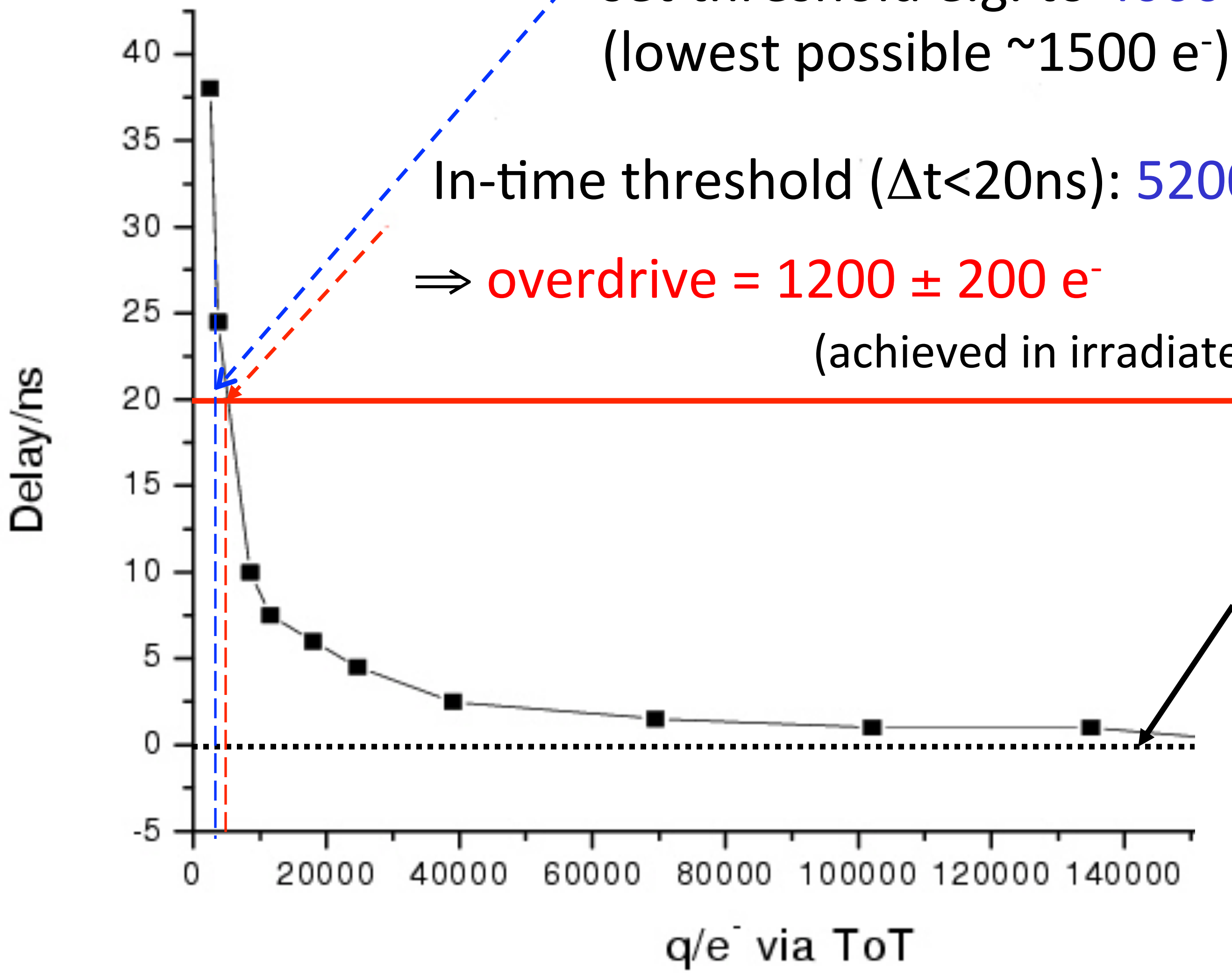
Important / in-time threshold & efficiency

set threshold e.g. to 4000 ± 200 e^-
(lowest possible ~1500 e^-)

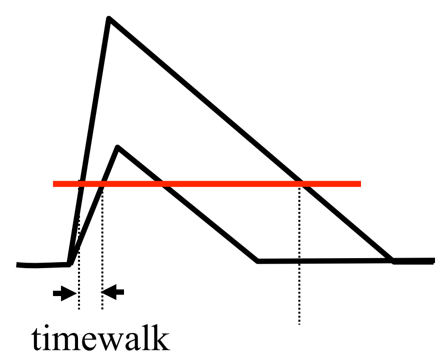
In-time threshold (Δt<20ns): 5200 ± 200 e^-

⇒ overdrive = 1200 ± 200 e^-

(achieved in irradiated assemblies)



zero time walk line for large signals



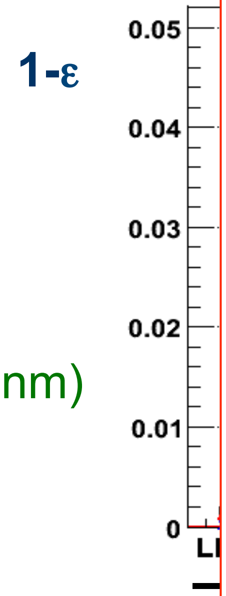
➔ in-time efficiency ~99% wanted and achieved !

HL-LHC data rates

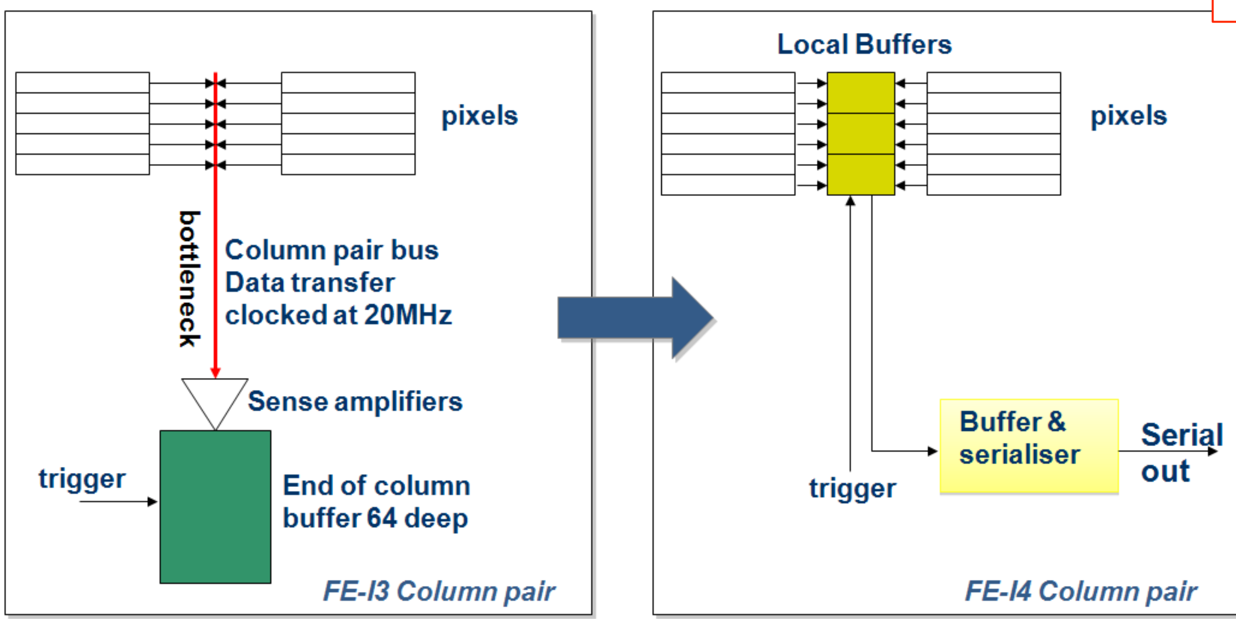
Hit inefficiency rises steeply with the hit rate

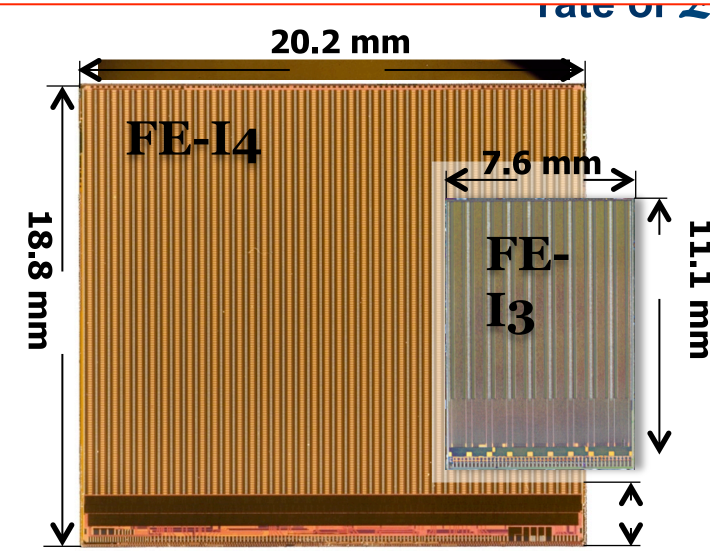
Bottleneck: congestion in (double) column readout

⇒**more local in-pixel storage** (250nm -> 130nm)
>99% of hits are not triggered
⇒ don't move them → no blocking



- IBM (130 nm)
- 87 Million transistors
- 26880 pixels (50 x 250 μm^2)
- lower noise than FE-I3
- operation at lower thresholds
- higher rate compatibility
- radiation hard to >250 Mrad
- 3+ years of design work w/ 8 designers
- working horse for current and future pixel R&D





Bonn, CPPM, Genova, LBNL, NIKHEF

M. Garcia-Sciveres et al, Nucl.Instrum.Meth. A636 (2011) 155-159

Hybrid Pixel assembly => called „hybridization“

Sensors

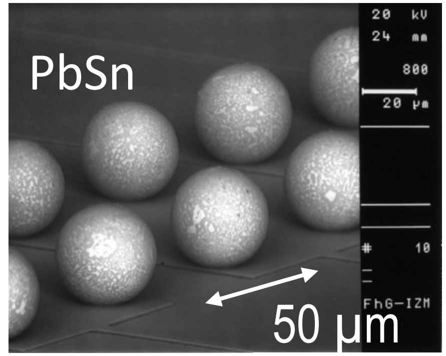
- n⁺ in n (oxygenated Si)
- wafer size (Ø 10 cm)
- ~200-250 µm thick

Electronics - Chip

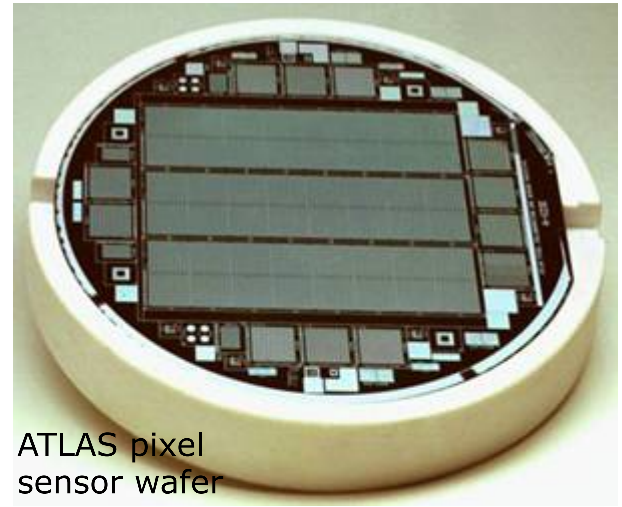
- chip size limited by yield ~1-2.5 cm^2
- wafer size (Ø 20 cm)

Hybridization

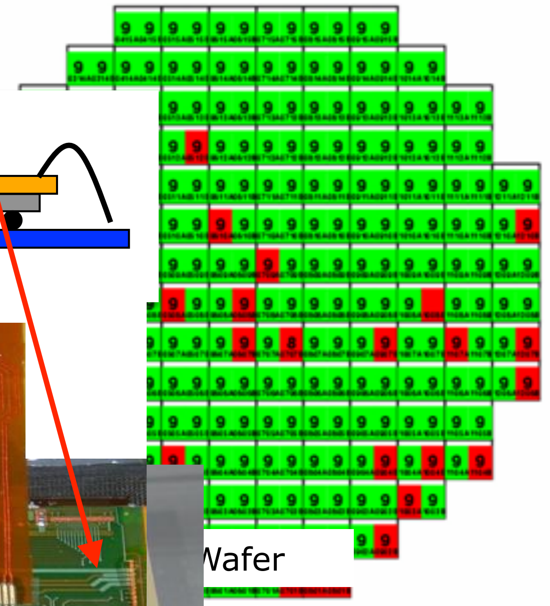
- PbSn or Indium bumps (wafer scale)
- IC wafers thinned after bumpin
- ‚flip-chip‘ to mate the parts
- ~3000 bumps/chip, ~50000 bur

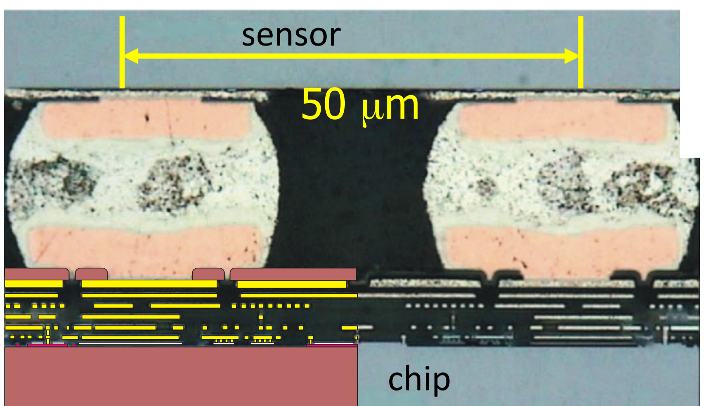


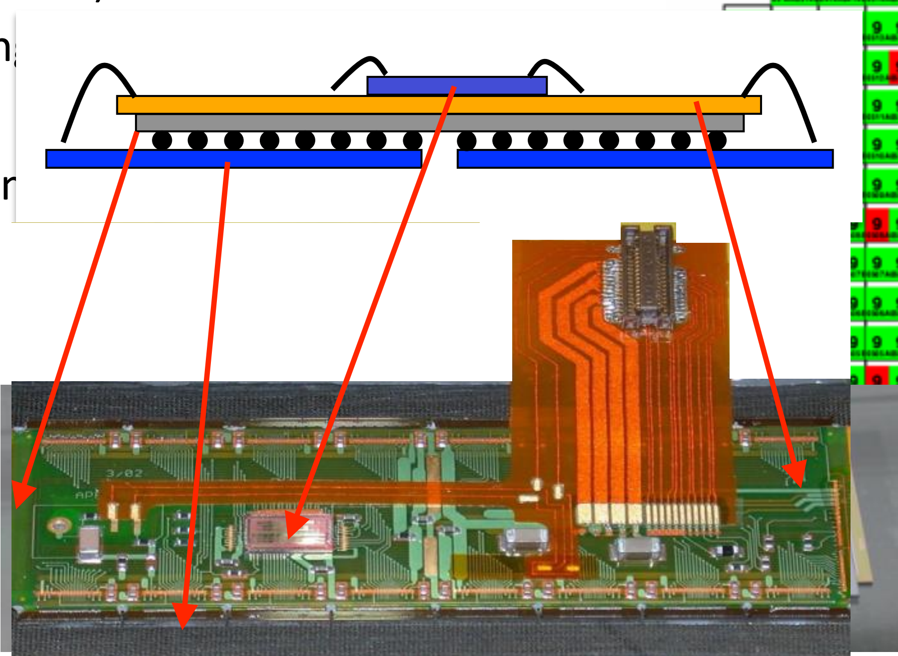
IZM,Berlin



ATLAS pixel sensor wafer

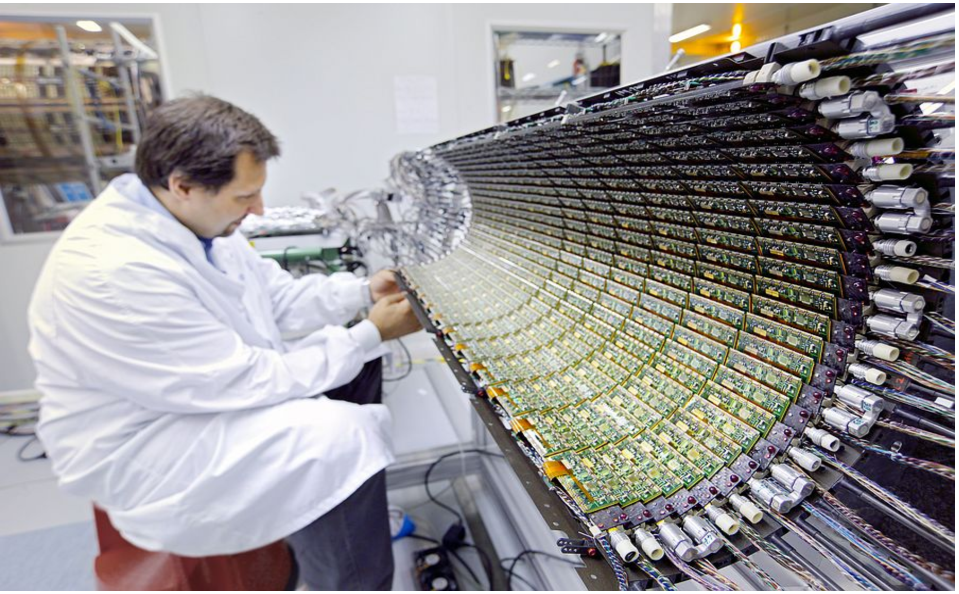


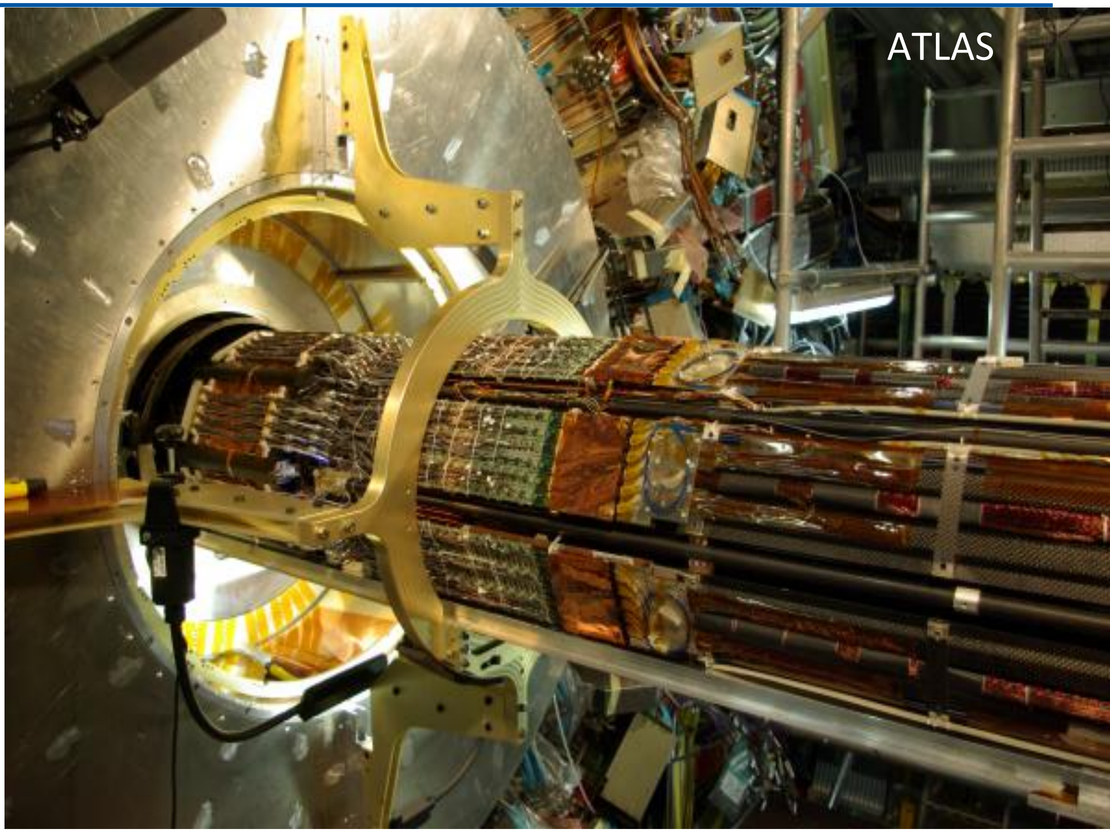


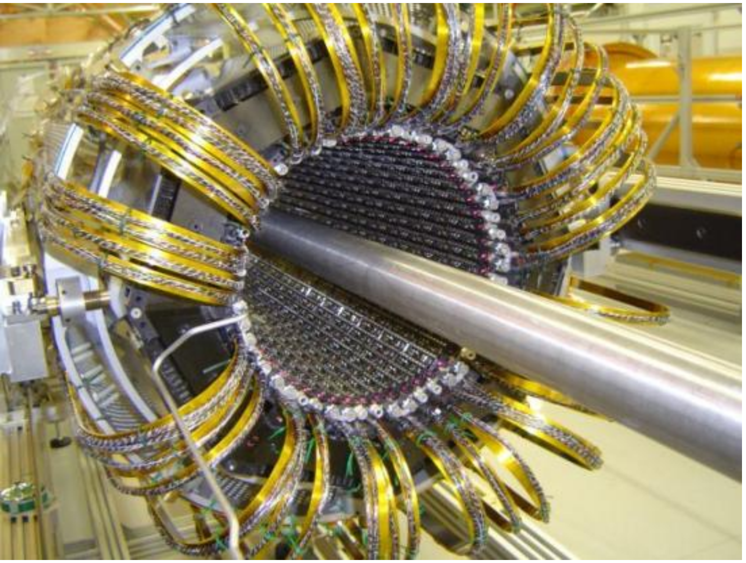


ATLAS Modul, Foto:IZM, Berlin

ATLAS Pixel Detector





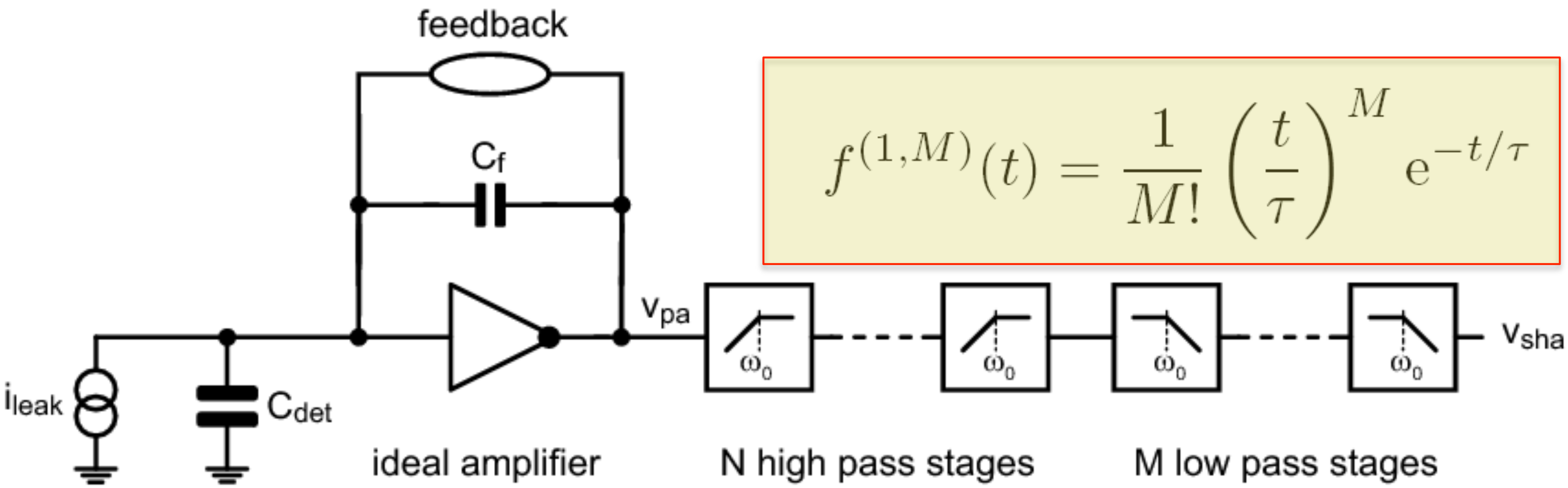


- light weight "carbon-carbon" structures
- cooling (pumped C_3F_8 : boiling point = -25^0)
- $T < -6^0$ C to limit damage from irradiation

Noise

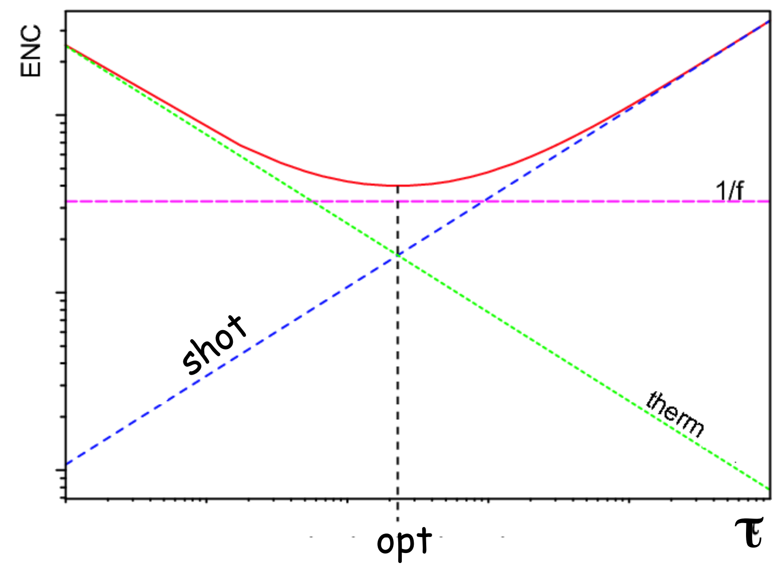
Noise in a pixel/strip detector (ionisation detector)

… with an additional filter amplifier (shaper) being the band width limiter



$$f^{(1,M)}(t) = \frac{1}{M!}\left(\frac{t}{\tau}\right)^M e^{-t/\tau}$$

$$\mathrm{ENC}^2(e^2) = 11\, I_0(\mathrm{nA})\,\tau(\mathrm{ns}) + 740\,\frac{1}{WL(\mu\mathrm{m}^2)}\,C_D^2(100\,\mathrm{fF}) + 4000\,\frac{1}{g_m(\mathrm{mS})}\,\frac{C_D^2(100\,\mathrm{fF})}{\tau(\mathrm{ns})}$$



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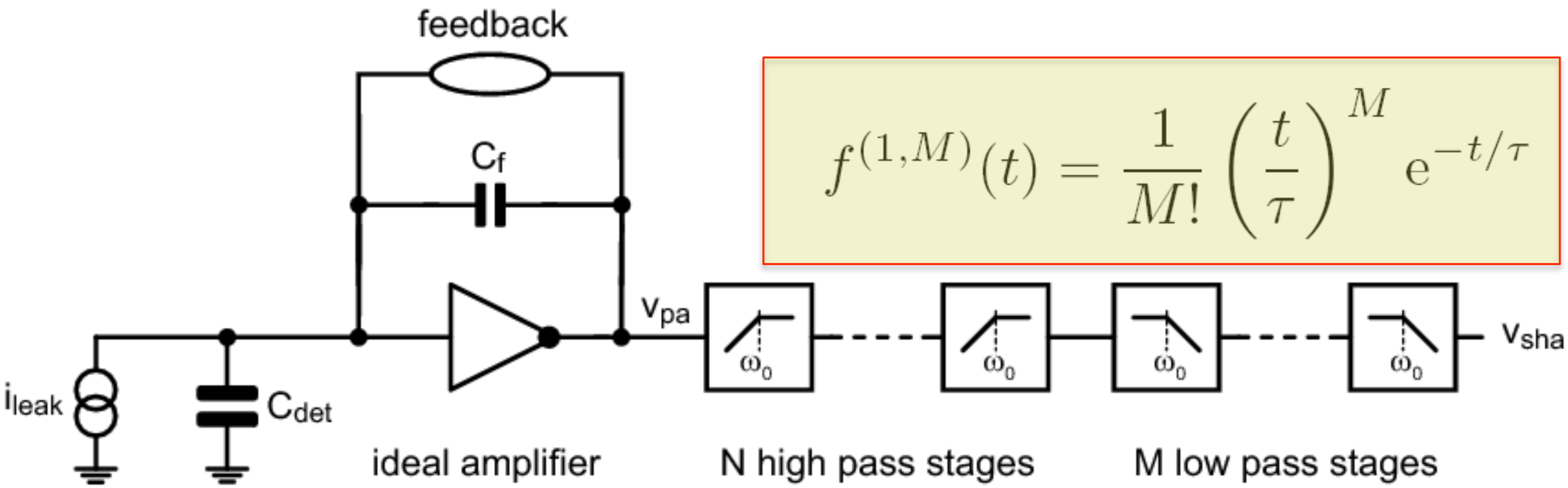
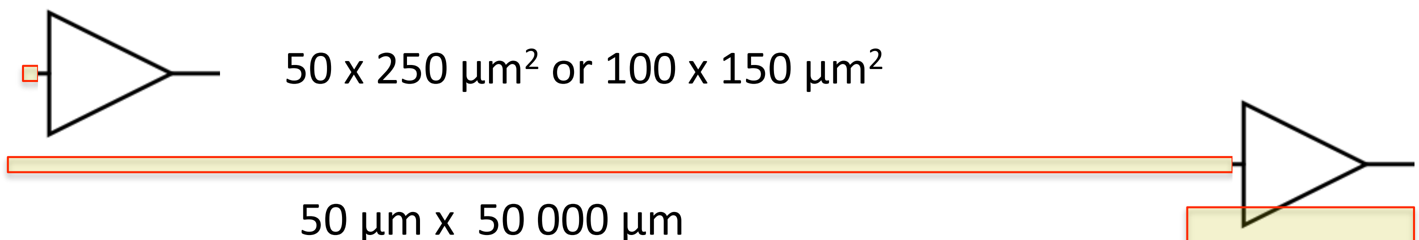


$$f^{(1,M)}(t) = \frac{1}{M!}\left(\frac{t}{\tau}\right)^M e^{-t/\tau}$$

comparing pixels and strips



	C_D	I_0	τ	W	L	g_m	ENC therm	ENC 1/f	ENC shot	ENC tot
pixel	200 fF	1 nA	50 ns	20 µm	0.5 µm	0.5 mS	25 e^-	17 e^-	24 e^-	**40 e^-**
strip	20 pF	1 µA	50 ns	2000 µm	0.4 µm	5 mS	800 e^-	200 e^-	750 e^-	**1100 e^-**

The typical S/N situation (... here ATLAS)

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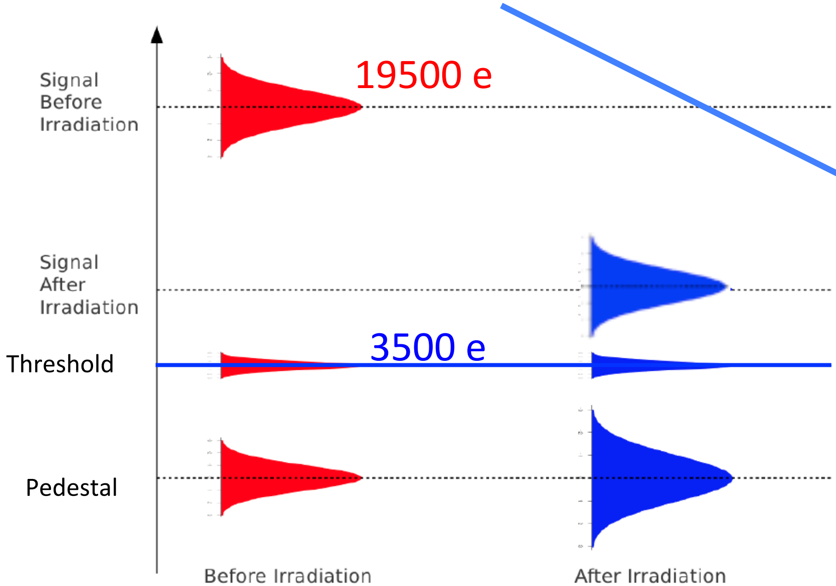
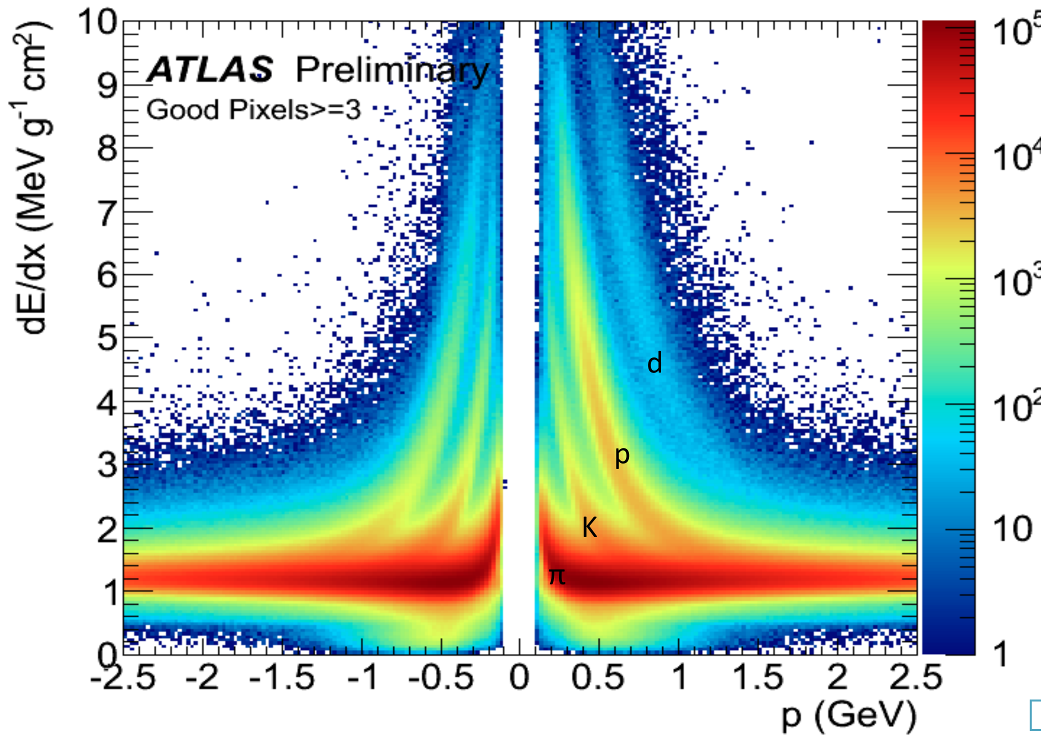
Signal of a high energy particle ≙ 19500 e^- → <10000 e^- after irradiation

Charge on more than 1 pixel => S/N > 30 → S/N ~ 10

- ❑ Discriminator thresholds = 3500 e, ~40 e spread, ~170 e noise
- ❑ 99.8% data taking efficiency
- ❑ 95.9% of detector operational
- ❑ ca. 10 µm x 100 µm resolution (track angle dependent)
- ❑ 12% dE/dx resolution





C. Gemme et al., ATLAS-CONF-2011-016

move to noise

skip dE/dx

How to make things better?

- sensors radiation hard
- (faster/better/lower power chips)
- avoid hybridization -> monolithic pixels

For very high fluences -> thin planar (pixel) sensors

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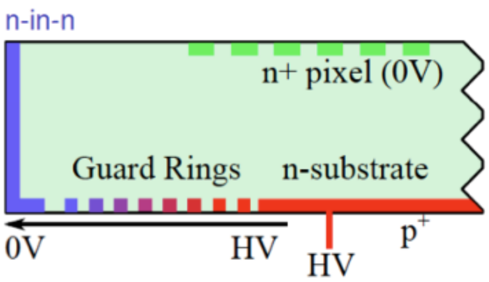
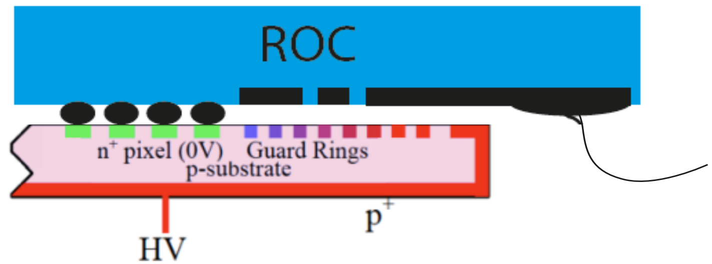
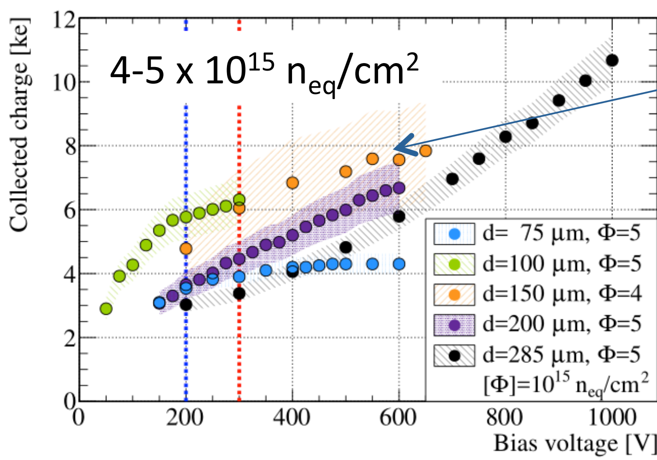
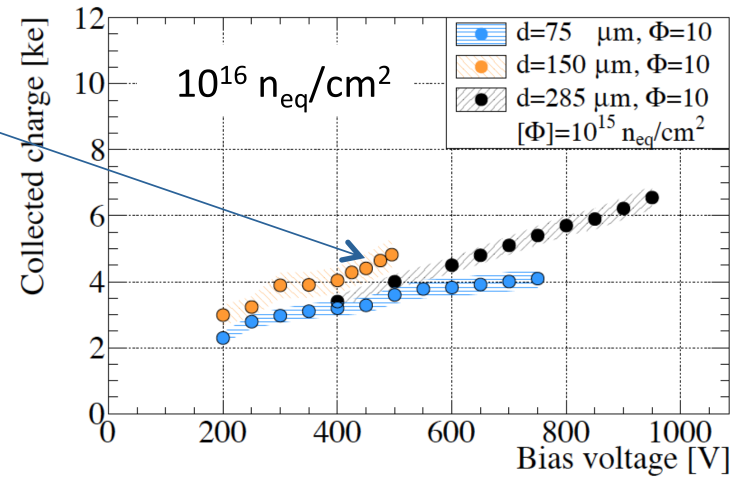




- thin n⁺ in p sensors after high fluences (neutrons)

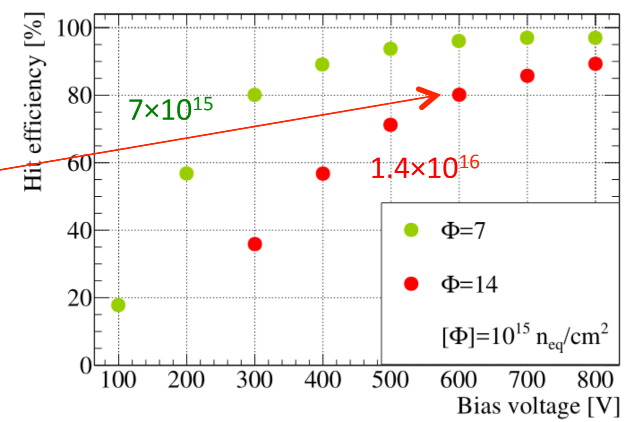
best (150 µm)





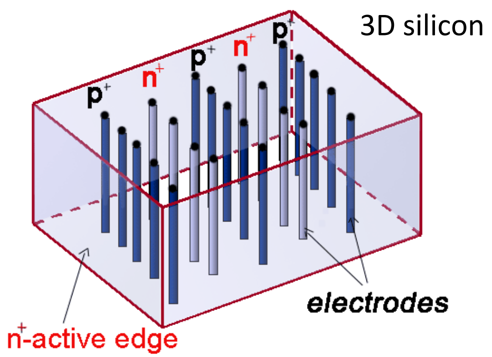
- **6000 – 7000 e-**
  for 100 - 200 µm sensors @ 300 V – 600 V bias

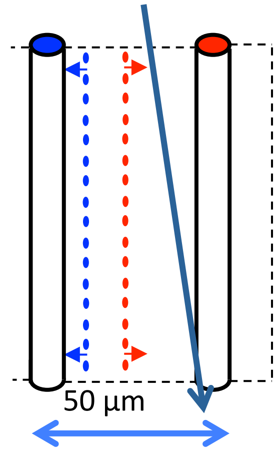
- hit efficiencies still reasonable at $\Phi > 10^{16}$

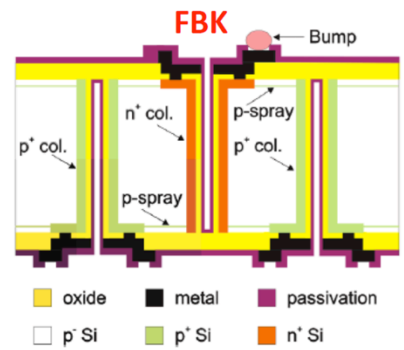


Terzo, Andricek, Macchiolo, Nisius et al, JINST 9 (2014) C05023

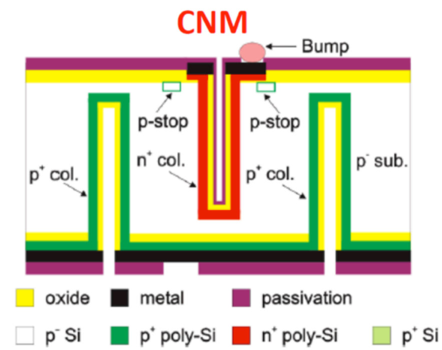
3D-Si sensors for the innermost pixel layer(s)







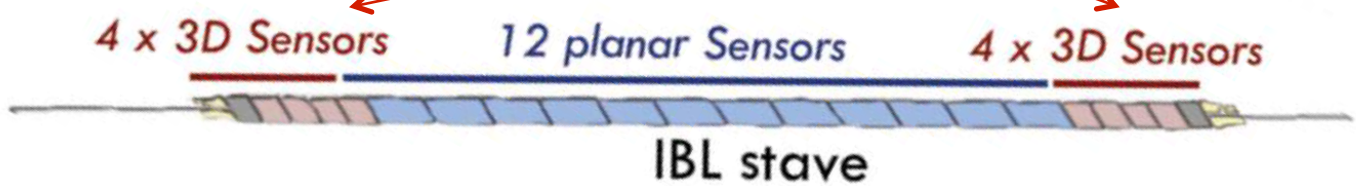
G.F. Della Betta et al., PoS Vertex2012 (2013) 014



G. Pellegrini et al.. NIM A731 (2013) 198-200

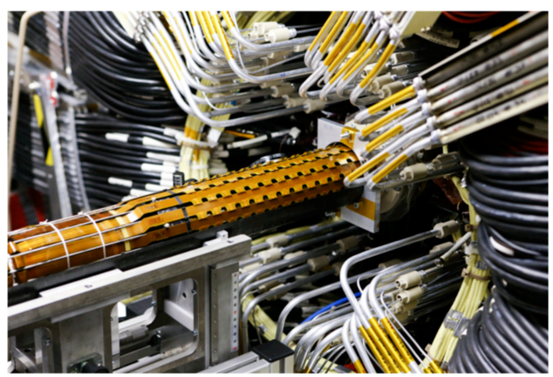
S. Parker, C. Kenney , J. Segal, ICFA Instrum.Bull. 14 (1997) 30-50
C. Da Via, et al., NIM A49 (2005) 122-125 and NIM A 699 (2013) 18

- particle path (signal) different from drift path
- high field w/ low voltage



-> radiation tolerance
-> Q still 50% @ 10^{16} cm^{-2}

- good for inclined tracks
- slightly larger C_{in} (noise)
- now also in diamond, CdTe



- 3D sensors have been put to reality
- in ATLAS IBL for one year
- perform as well as planar pixels

Hybrid Pixels @ LHC: PROs and CONs

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- complex signal processing already in pixel cells possible
  - zero suppression
  - temporary storage of hits during L1 latency
- radiation hard to $>10^{15}\ n_{eq}/cm^2$
- high rate capability (~MHz/mm^2)
- spatial resolution ~ 10 – 15 µm

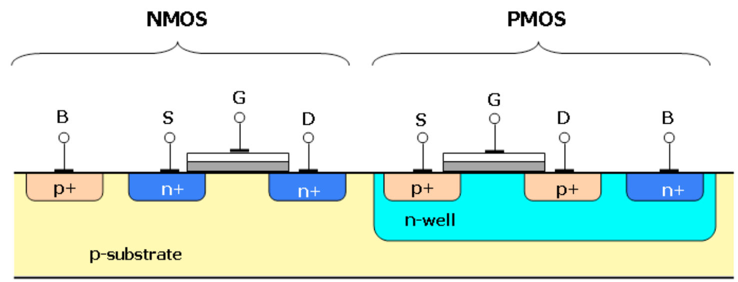
PRO

… but also

- relatively large material budget: **~3% X_0** per layer (1% X_0 @ ALICE)
  - sensor + chip + flex kapton + passive components
  - support, cooling (-10°C operation), services
- complex and laborious module production
  - bump-bonding / flip-chip
  - many production steps
  - expensive

CON

CMOS Pixels



- Use commercial CMOS technology
  - mature (world market)
  - cheap in comparison
- Monolithic (i.e. one sensor/chip entity)
  - avoids hybridization
  - wafer scale processes
  - large modules possible (employ stitching over reticules)
- Small pixels (at least in principle)
  - o (25 x 25 µm²)

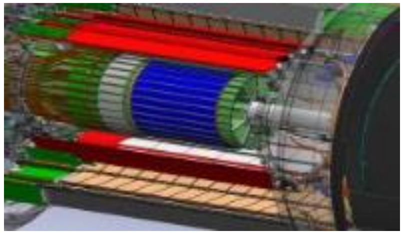
BUT

- Industry does not care much about particle physics
  - they use cheap low resistive substrate Si (not depletable) … Q-coll by diffusion (slow)
  - some (CMOS camera) technology have relatively thick epitaxial layer (~15 µm)

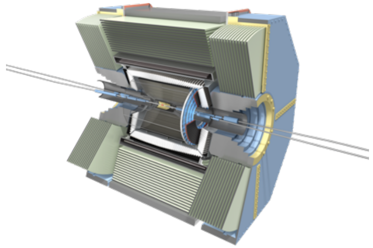
⇒ try to exploit special technology features to make detectors
multiple wells, some (thin) depletion layer, backside contacts => optimize Q-coll.

Rate and Radiation Levels

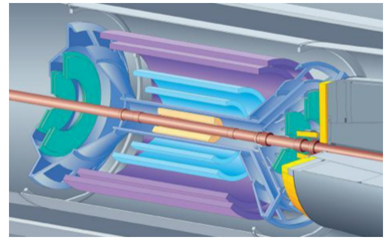
STAR



Belle II

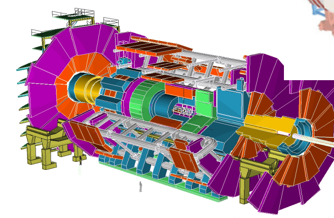


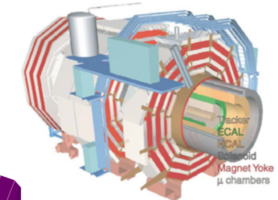
ALICE-(HL)-LHC



ILC

ATLAS





CMS

Numbers for innermost layers (r ≈ 5cm,) -> scale by 1/10 for typical strip layers (r > 25 cm)

	STAR	Belle II	ALICE-LHC heavy ion	ILC	LHC pp	HL-LHC-pp	
						Outer	Inner
BX-time (ns)	110	2	20 000	350	25	25	25
Particle Rate (kHz/mm^2)	4	400	10	250	1 000	1 000	10 000
Φ (n_{eq}/cm^2)	few 10^{12}	3 x 10^{12}	> 10^{13}	10^{12}	2x10^{15}	10^{15}	2x10^{16}
TID (Mrad)*	0.2	20	0.7	0.4	80	50	> 1000

*per (assumed) liftetime
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

- much less material
- high resolution
- monolithic pixels

state of the art

- large area strips
- hybrid pixels

- even larger area
- radhard sensors
- high rate R/O
- new type R&D

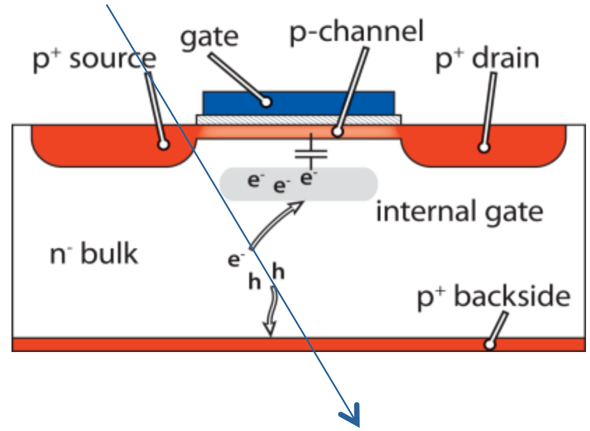
NEW developments

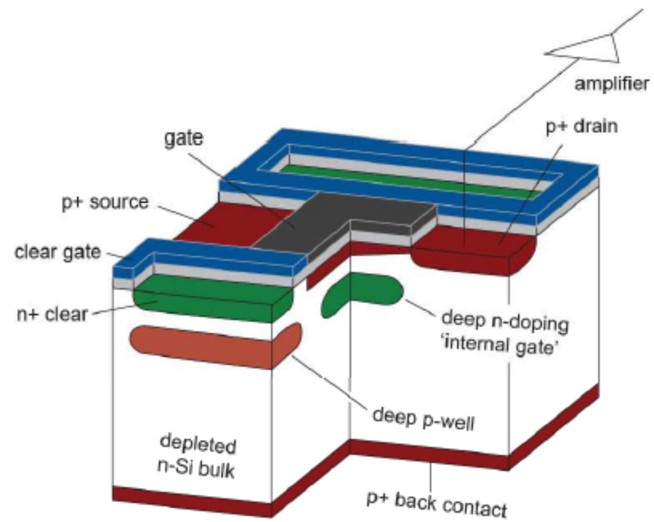
DEPFET Pixels -> Belle II

Monolithic Pixels -> STAR@RHIC, ALICE

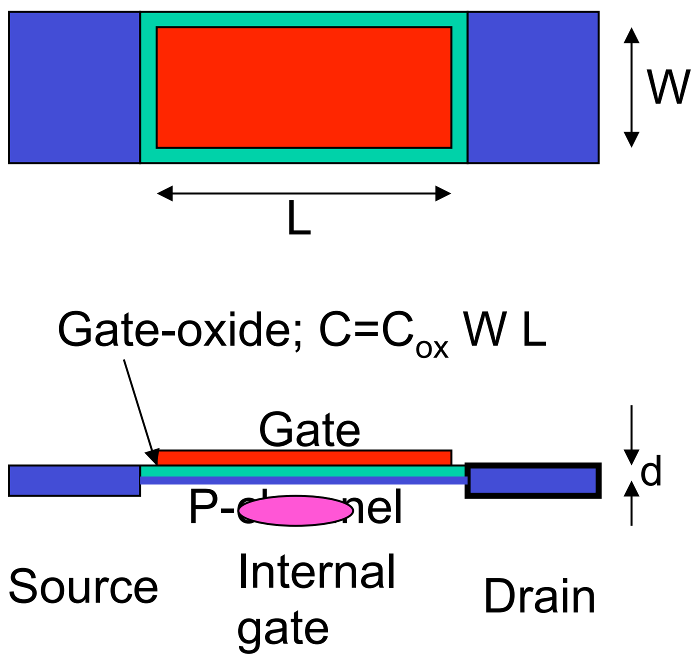
DMAPS (Depleted MAPS) -> LHC Upgrade?

DEPFET Pixels





How does a DEPFET work?



A charge q in the internal gate induces a mirror charge αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$ which in turn changes the transistor current I_d .

q

FET in saturation:

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right)^2$$

I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
W,L: Gate width and length
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

Conversion factor:

$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha\mu}{L^2}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right) = \alpha\sqrt{2\frac{I_d\mu}{L^3WC_{ox}}}$$

$$g_m \quad \boxed{: g_q = \alpha\frac{g_m}{WLC_{ox}} = \alpha\frac{g_m}{C}}$$

How does a DEPFET work?

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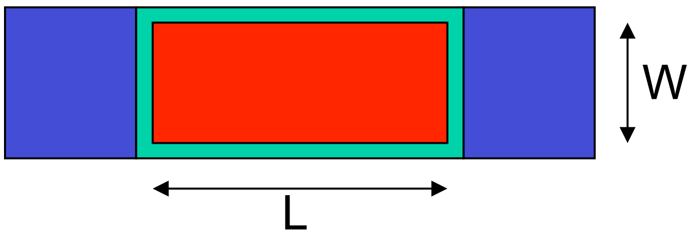
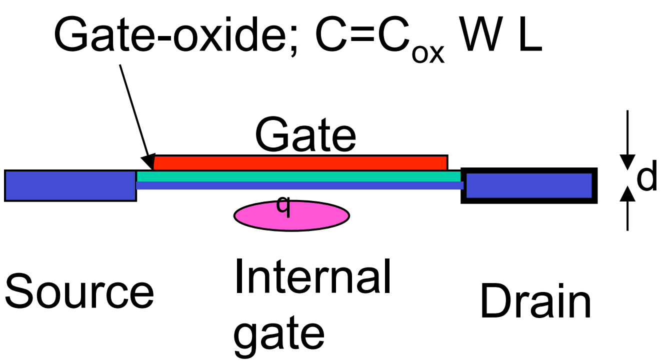
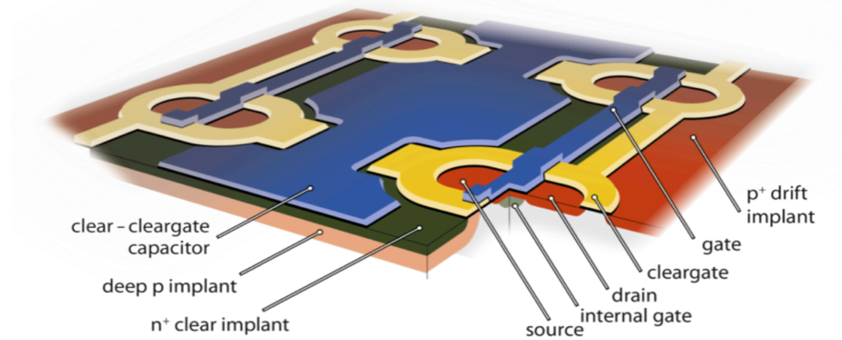
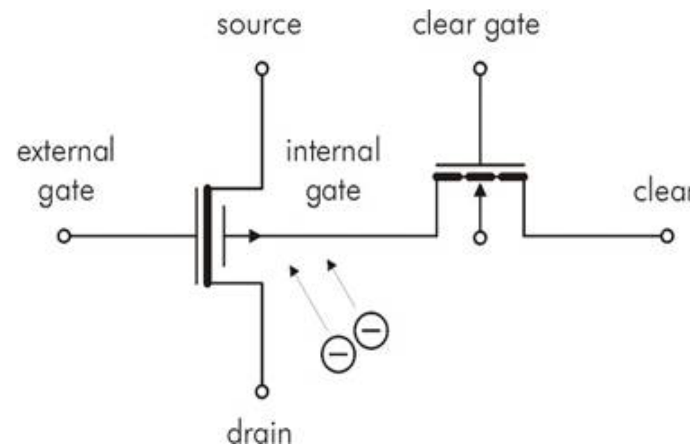




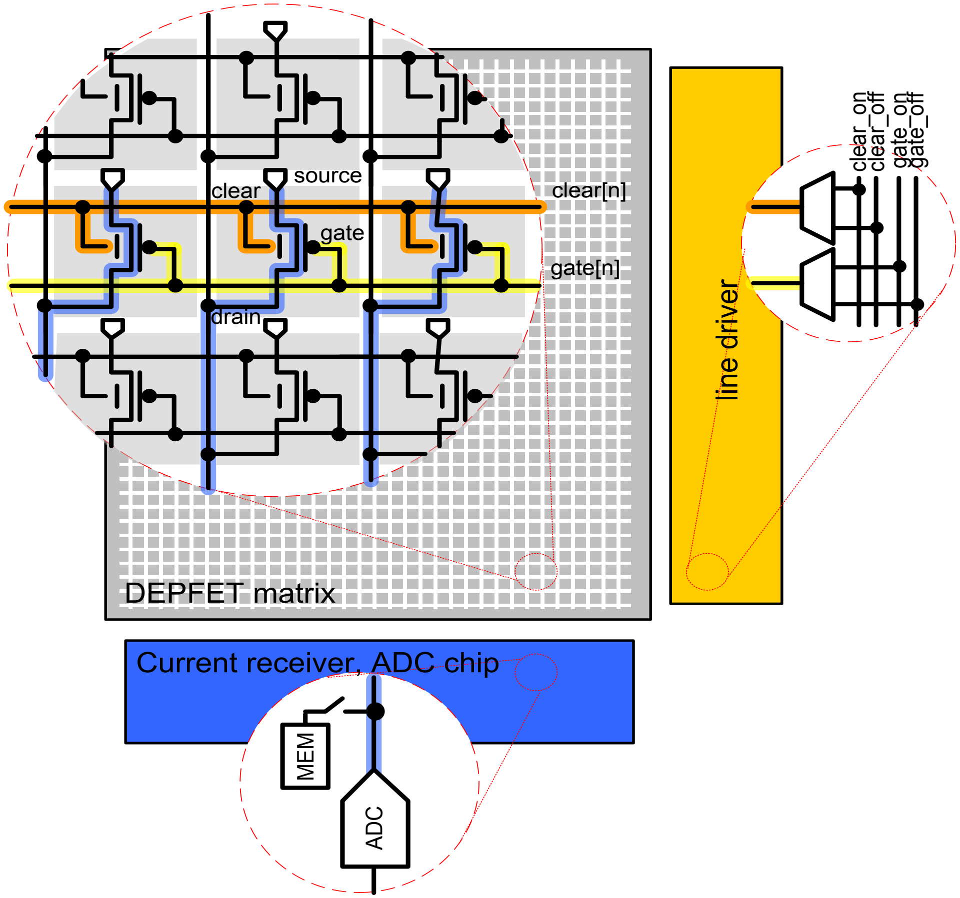




A charge q in the internal gate induces a mirror charge αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$ which in turn changes the transistor current I_d .

- Internal amplification $g_q \sim 500$ pA/e$^-$
- Small intrinsic noise
- Sensitive off-state, no power consumption

DEPFET pixel array



- DEPFET pixel transistors arranged in a matrix
- row wise select -> column wise readout of transistor (drain) currents
- Gate and clear lines need a steering chip
- Long drain readout lines to keep material out of the acceptance region
- 100 ns per row
  20 µs per frame

BELLE II Pixel Detector

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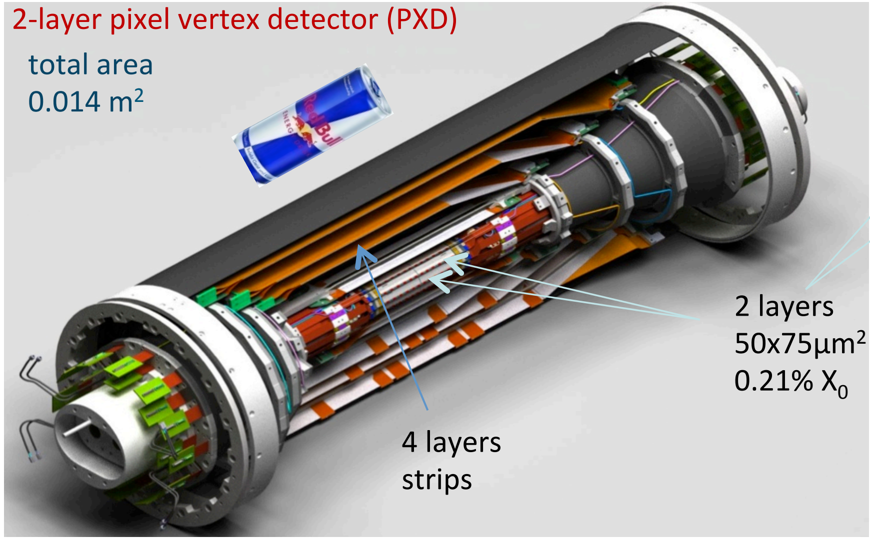
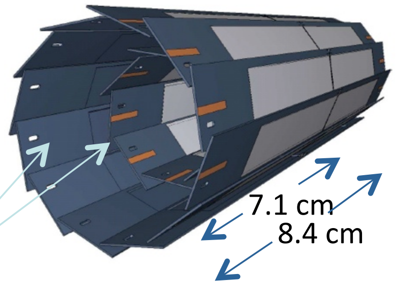
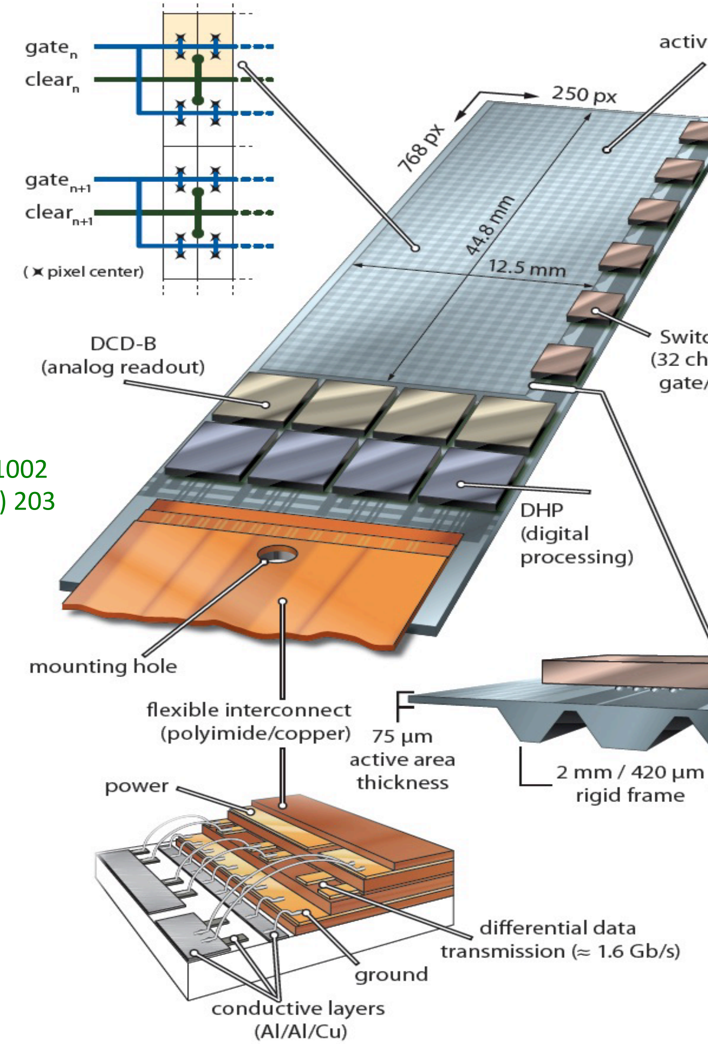


2 layers
50x75μm² pixels
0.21% X_0



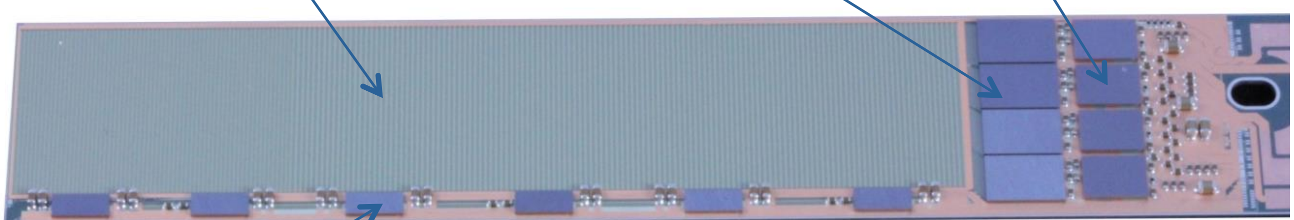
C. Marinas et al., JINST 10 (2015) 11, C11002
C. Kiesling et al., PoS EPS-HEP2011 (2011) 203



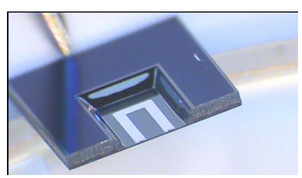
DEPFET sensor

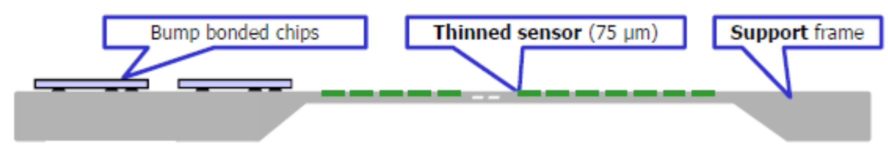
current digitizer chips

data processing chips



switcher chips





L. Andricek, IEEE Trans.Nucl.Sci. 51 (2004) 1117-1120

CMOS Pixels (sometimes called MAPS)

skip ?

From HYBRID to monolithic CMOS pixels

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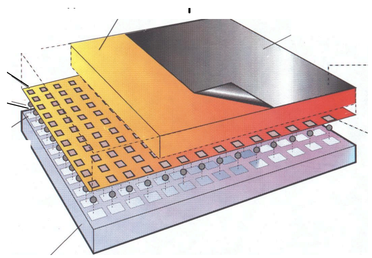
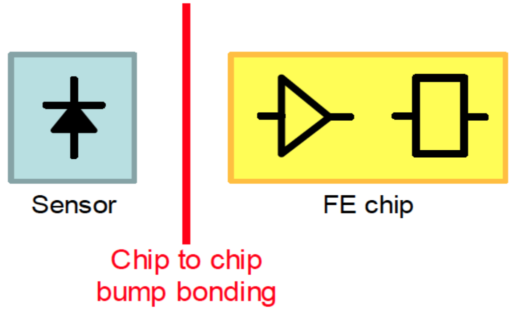
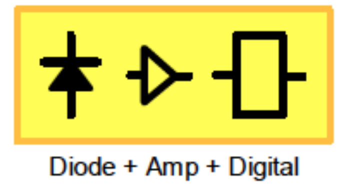
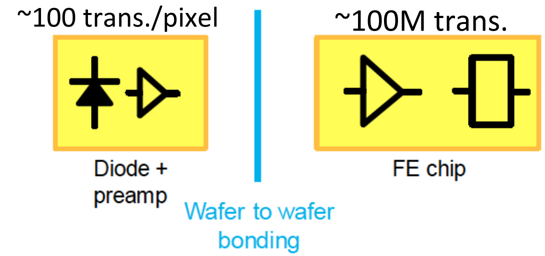






full monolithic



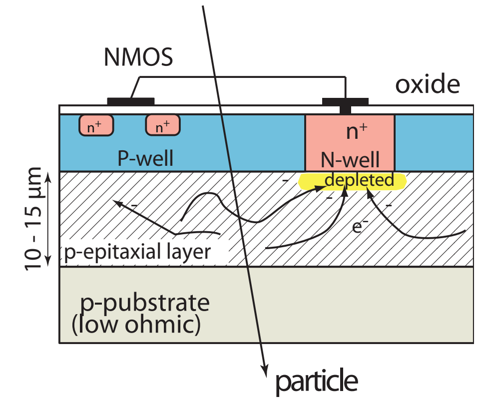
smart sensor bonded to R/O chip (CCPD)

Monolithic Active Pixel Sensors

B. Dierickx, D. Meynants, G. Scheffer, SPIE 3410:68-76 (1998)
R. Turchetta, …, M. Winter et al, NIM A458 (2001) 677-689

- **MAPS** using CMOS with Q-collection in **epi-**layer: developed for > 10 yrs
  Q by diffusion → recent advances

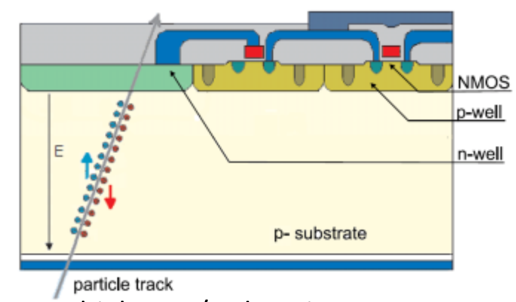
STAR + ALICE



- Depleted **DMAPS** (CMOS pixels)
  - using **HR** substrates and **HV** add-ons to create some depletion region
  - CMOS on **SOI**

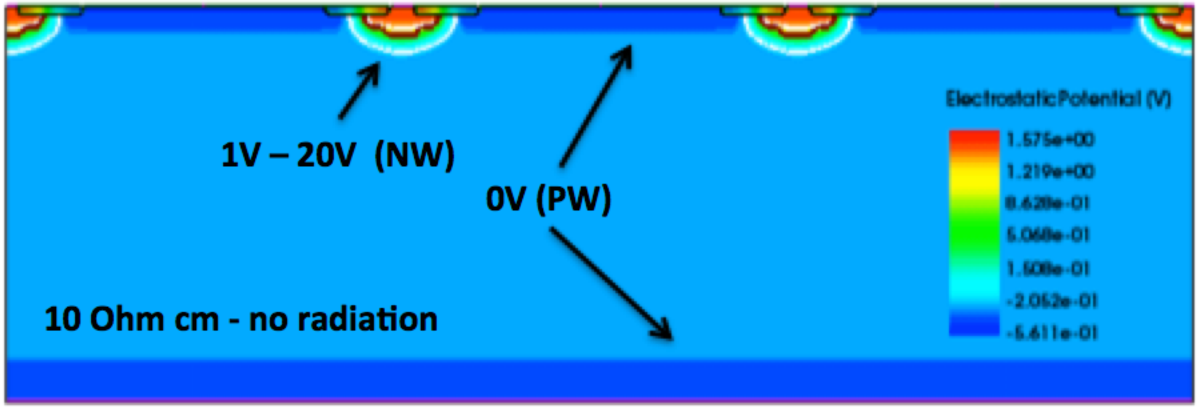
HL - LHC

$$d \sim \sqrt{\rho \cdot V}$$



high rate/rad environment

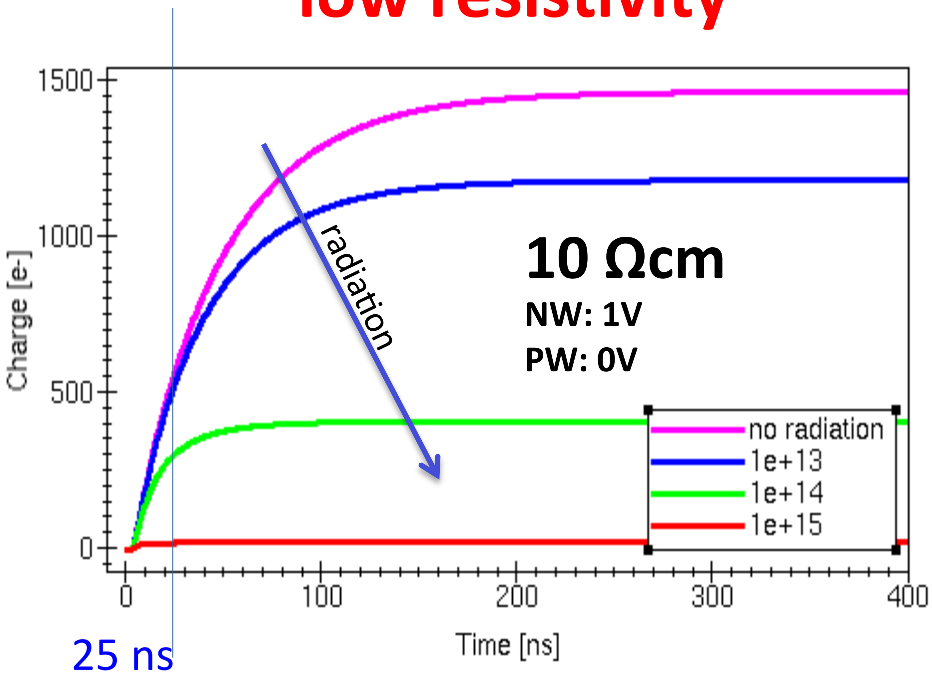
TCAD simulations: resistivity – voltage – fill factor



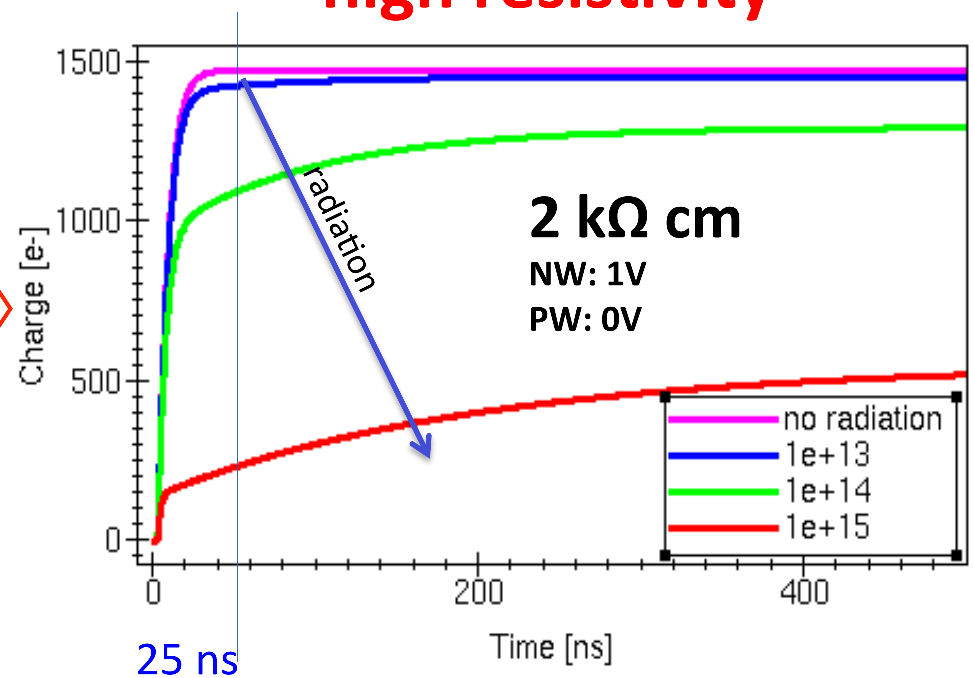
Substrate: 10 Ωcm – 2kΩ cm
Nwell: 1V – 20 V
Pwell: 0V

from Tomasz Hemperek

low resistivity



high resistivity



TCAD simulations: resistivity – voltage – fill factor

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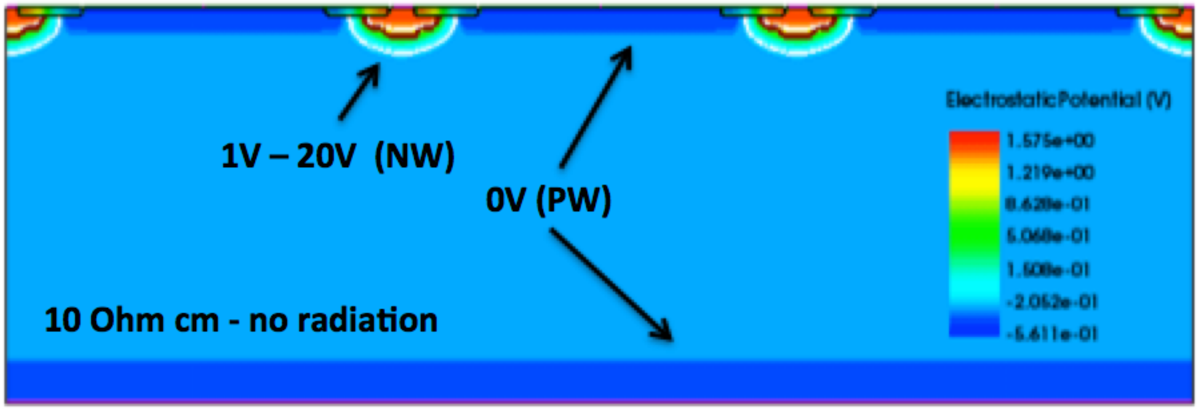
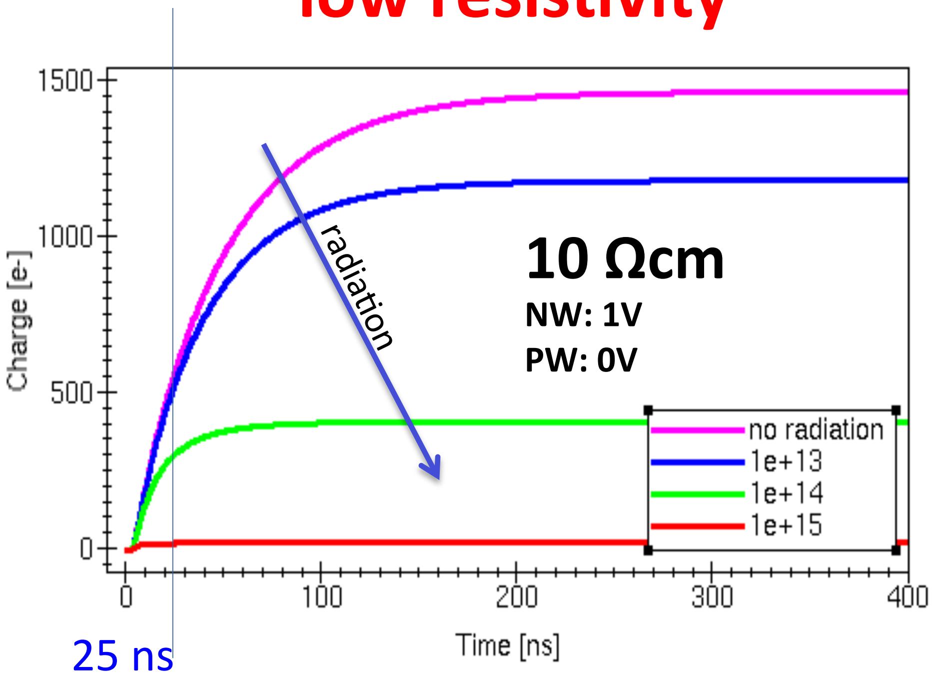


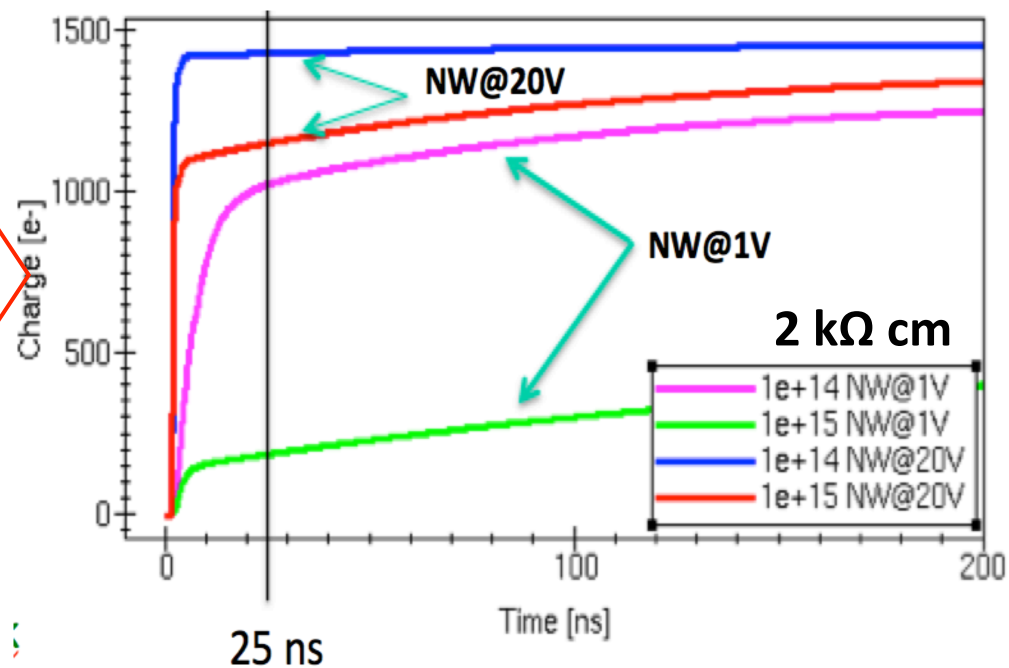
Substrate: 10 Ωcm – 2kΩ cm
Nwell: 1V – 20 V
Pwell: 0V

from Tomasz Hemperek

low resistivity

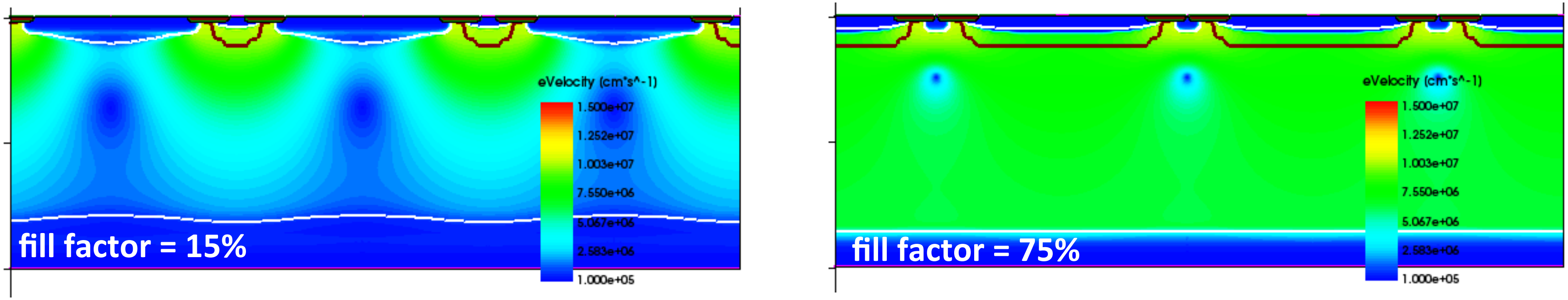


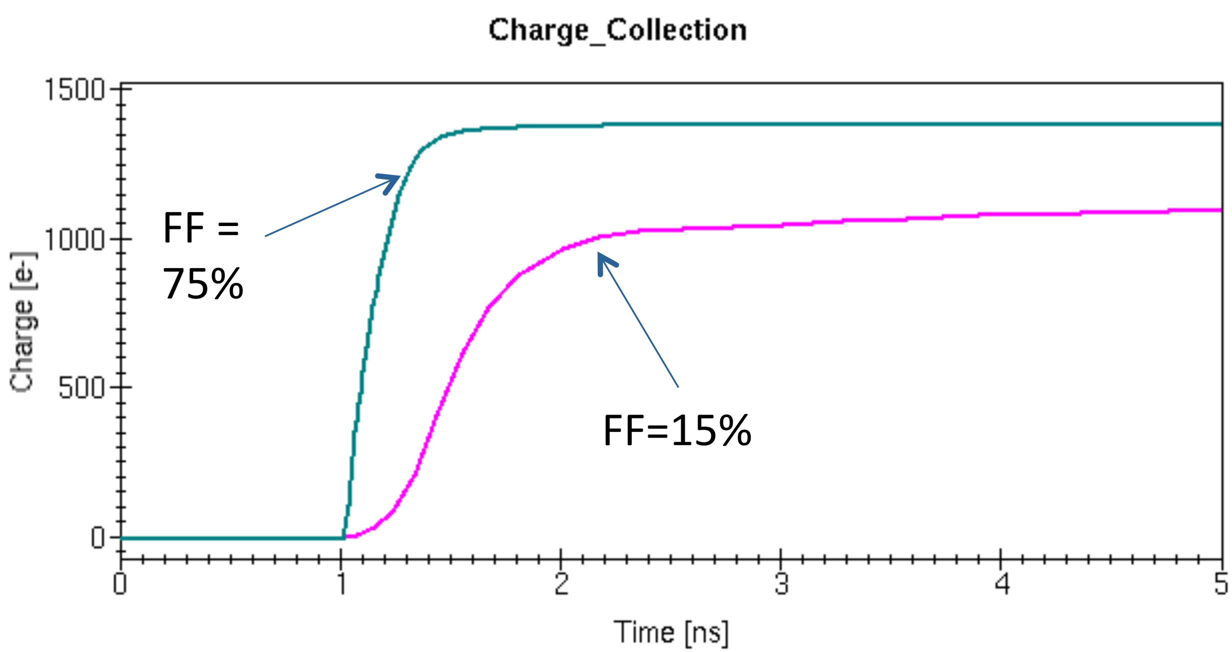
HR plus (high) voltage



Fill Factor influence: here at 10^{15} n_{eq}/cm^2

Electron Velocity





NW: 20V
PW: 0V
Substrate:2kΩ cm
Dose: 10^{15} n_{eq}/cm^2

Tomasz Hemperek

Conclude for CMOS pixels ...

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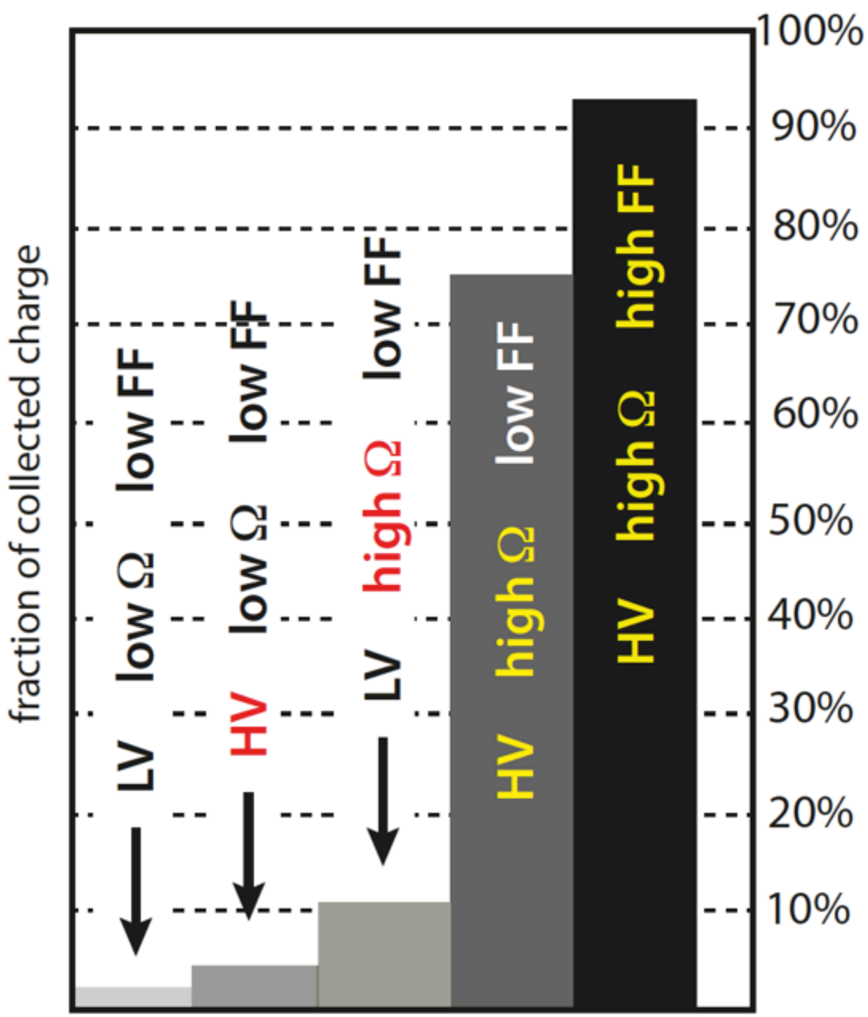
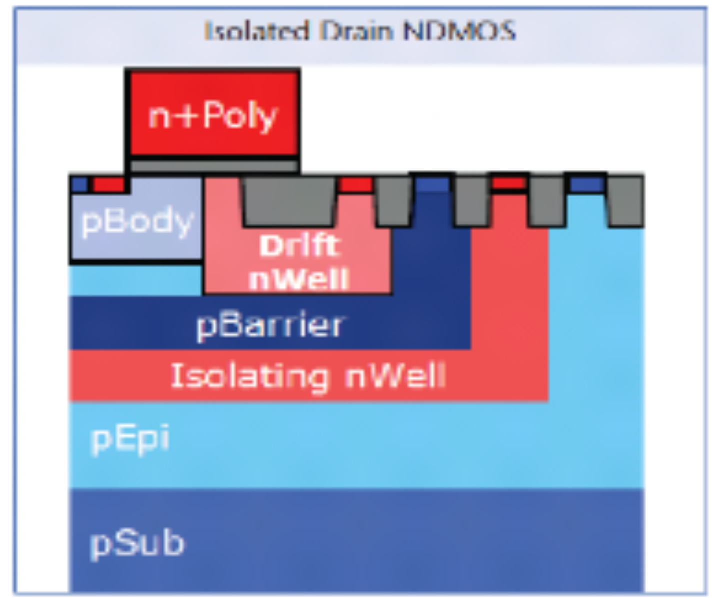
need all three!



for $n_{eq} = 1 \times 10^{15}\,\mathrm{cm}^{-2}$

PLUS



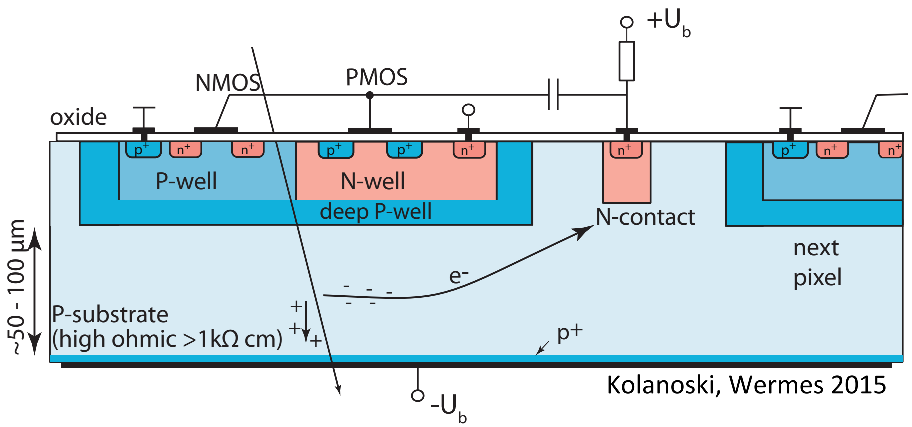
from: www.xfab.com

multiple nested wells

Current DMAPS approaches

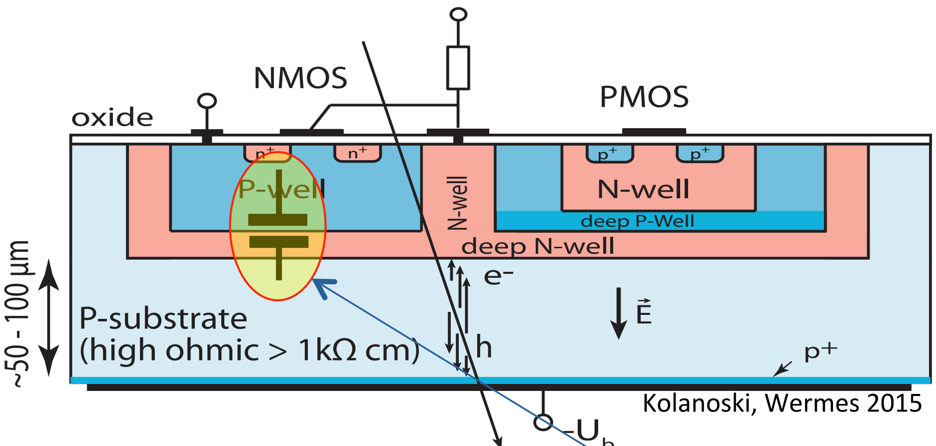
I. Peric et al., NIM A582 (2007) 876-885 & NIM A765 (2014) 172-176
S. Mattiazzo, W. Snoeys et al., NIM A718 (2013) 288-291
M. Havranek, Hemperek, Krüger, NW et al. JINST 10 (2015) 02, P02013

HR/HV - CMOS



- (D)MAPS like configuration but w/ depleted bulk
- small collection node
- long drift path

=> **smaller C, more trapping**



- deep n and deep p wells
- large collection node
- short drift path

=> **larger C, less trapping**

important: (number of) deep wells and detailed cell geometry

watch: capacitance between deep p- and n-wells

4D with LGADs ?

Low Gain Avalanche Detectors

New: How to obtain fast timing with Si detectors?

- How would one go about getting into the 10 ps range with (structured) Si detectors?
- => exploit "in-silicon" charge amplification
  - in "Geiger Mode" fashion (like in gas **RPCs**)

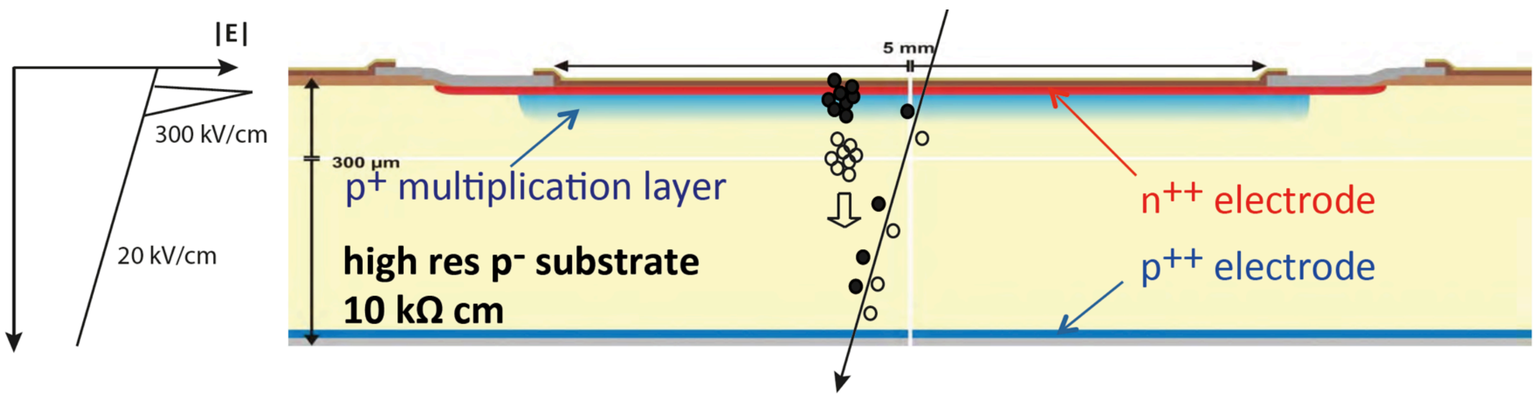
σ_t governed by avalanche fluctuations

$$\sigma_t \approx \frac{1.4}{(\alpha - \eta)\, v_D} \approx 50\text{ps}$$

Townsend coeff. attachment coeff.

see e.g. W. Riegler, C. Lippmann, R. Veenhof NIM A 500 (2003) 144

  - OR .... in "linear mode" fashion
    -> Low Gain Avalanche Detectors



see N. Cartiglia Parallel 2

H. Sadrozinski et al., NIM A730 (2013) 226-231
N. Cartiglia et al., JINST 9 (2014) C02001
A. Seiden et al, Vertex2015, Proceedings

Towards 4D tracking ... Low-Gain Avalanche Detectors

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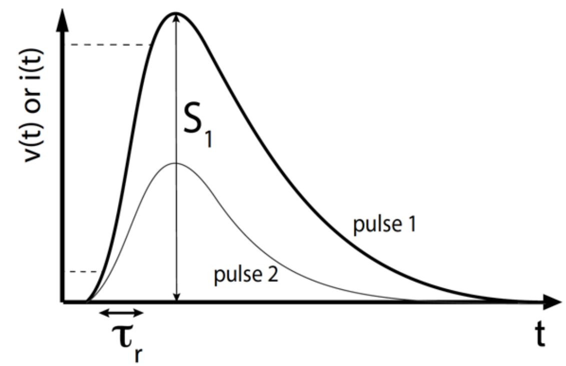
- ❑ Separate the "collection" of charge from the signal gain
- ❑ Figure of merit for σ_t is the "slew rate" $dV/dt \approx \text{Signal}/\tau_{rise}$

$$\sigma_t^2 = \underbrace{\left(\frac{V_{th}}{dV/dt}\bigg|_{rms}\right)^2}_{\text{signal time walk}} + \underbrace{\left(\frac{\text{Noise}}{dV/dt}\right)^2}_{\text{noise time jitter}} + \underbrace{\left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2}_{\text{TDC binning}}$$

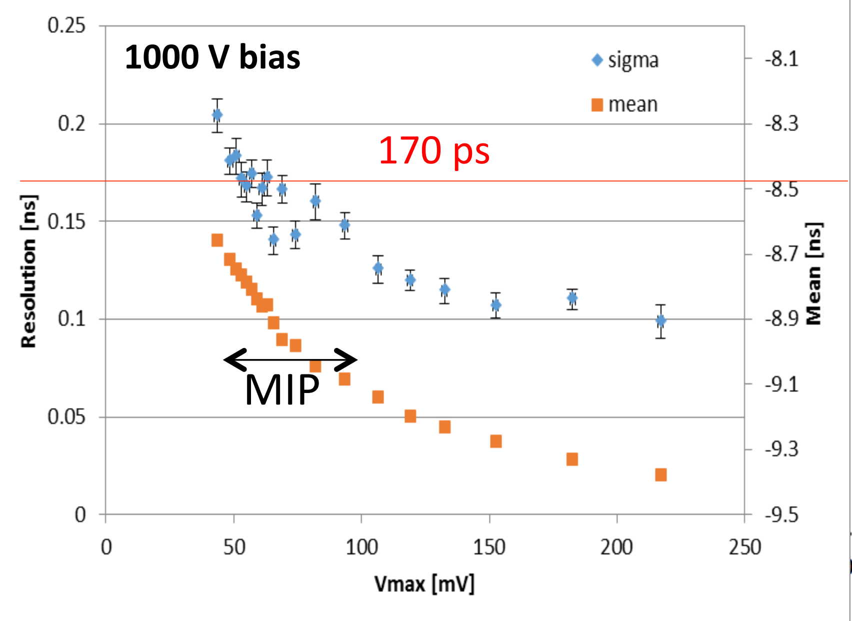
can be made negligible



Need: fast drift - large signals – low noise

- e- drift in sat. (E = 20 kV/cm, $v_D \approx 10^7$ cm/s) => HV
- collect electrons fast => thin
- get large signals => from amplified holes (!)
- small C, small i_{leak}, low noise => small electrodes
- broad-band (non-CSA) amplifier & e.g. CF discr.

<= CNM 8x8 mm^2
300 µm thick, 11 pF
in 120 GeV pion beam



- ❑ Ultimate Goal: simultaneous space (~10µm) and time resolution (< 50 ps) -> pile-up ki
- ❑ Options for ATLAS (HighGranularityTimingDetector; Forward) and CMS-TOTEM (in Roman Pots)

Further Reading

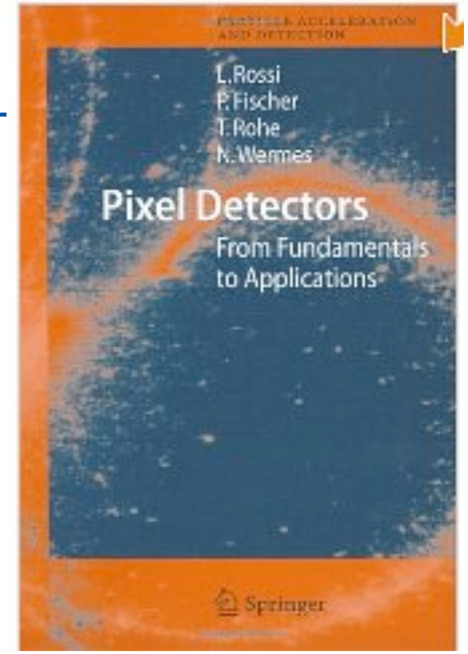
- G. Lutz, “Semiconductor Radiation Detectors”,
  Springer Berlin-Heidelberg-New York, 1999.

- Rossi, Fischer, Rohe, Wermes,
  “Pixel Detectors: From Fundamentals to Applications”,
  Springer Berlin-Heidelberg-New York, 2006, (ISBN 3-540-283324)

- ATLAS Pixel Detector, Technical Design Report, CERN/LHCC/98-13 (1998)
  CMS Tracker Technical Design Report, CERN/LHCC/98-6 (1998)
  ALICE Inner Tracker System, Technical Design Report, CERN/LHCC/99-12 (1999)

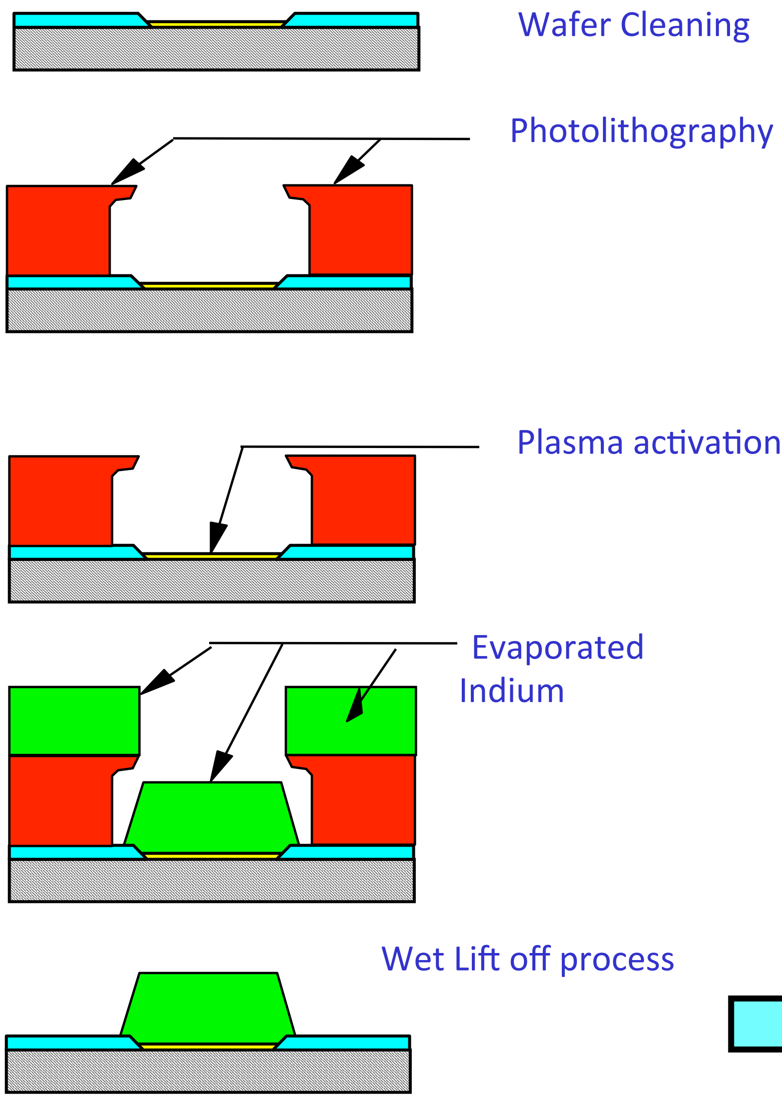
- N. Wermes, “Pixel Detectors for Charged Particles”
  Published in Nucl.Instrum.Meth. A604 (2009) 370-379,
  e-Print Archive: physics/0811.4577

- Kolanoski, H. and Wermes, N.
  Teilchendetektoren – Grundlagen und Anwendungen, Spektrum-Verlag,
  (2016) in print



BACKUP

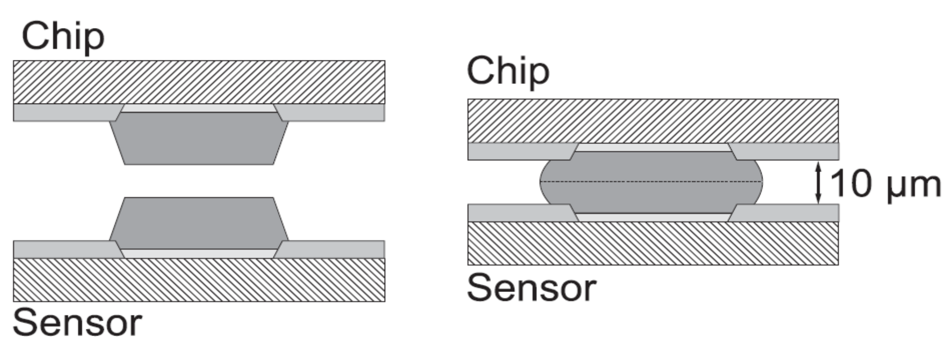
Indium bumping process



Process parameters:

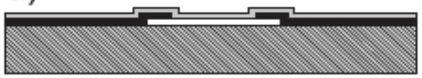
- Resist Thickness: 15 μm
- Pre-bake: 30min @ 80 °C
- Deposition rate: 0.5 μm/min
- Dep. Pressure: 9 x 10 $^{-7}$ Torr
- Temp. during Dep. < 50 °C

Flip-Chip



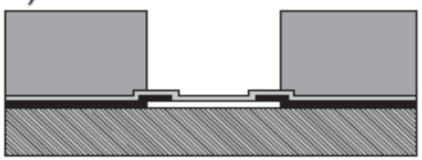
Solder bumping & flip chip process

a)



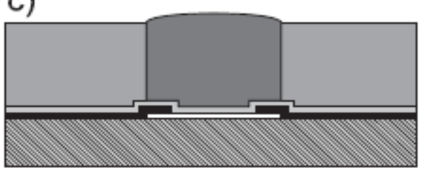
Sputter etching and sputtering of the plating base / UBM

b)



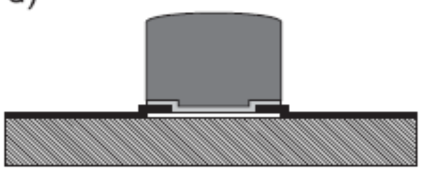
Spin coating and printing of Photoresist

c)



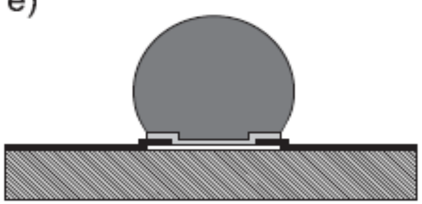
Electroplating of Cu and PbSn

d)

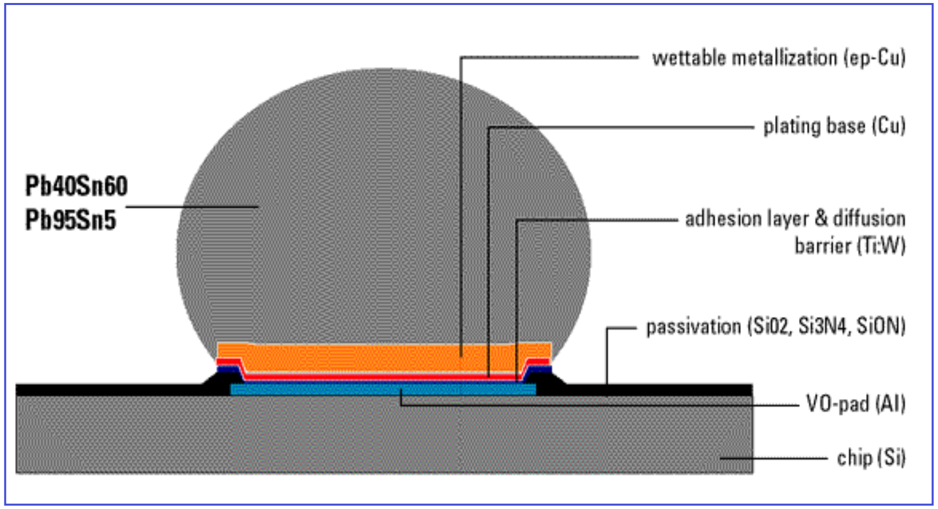


Resist stripping and wet etching of the plating base

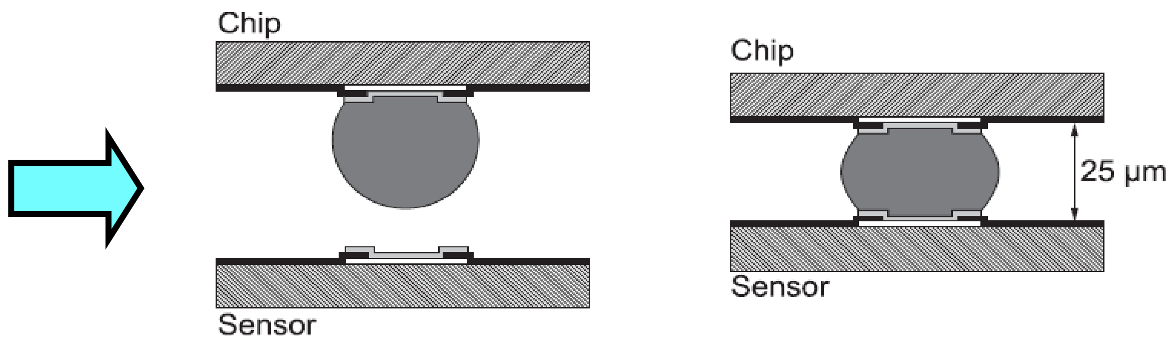
e)



Reflow

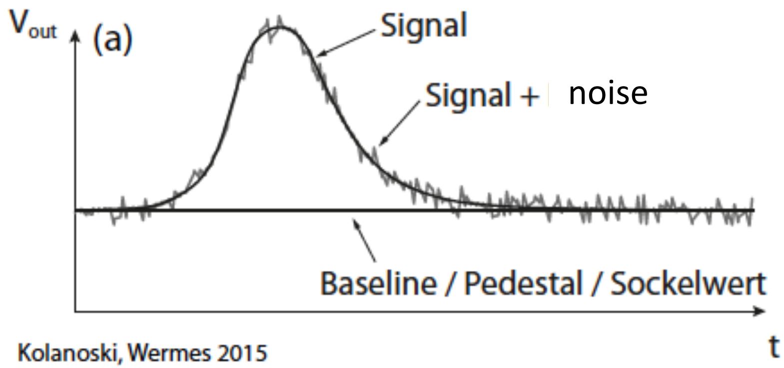


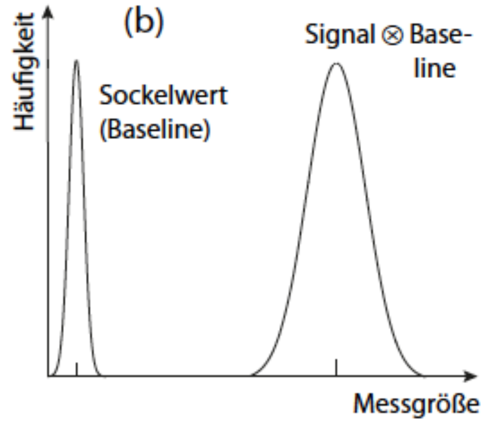
Flip-Chip

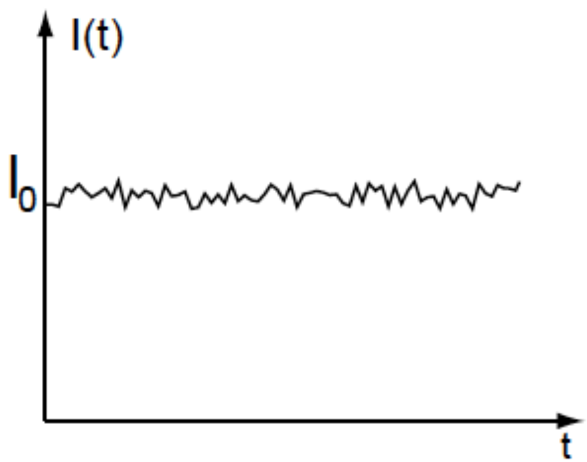


Noise

Noise in ionisation detectors





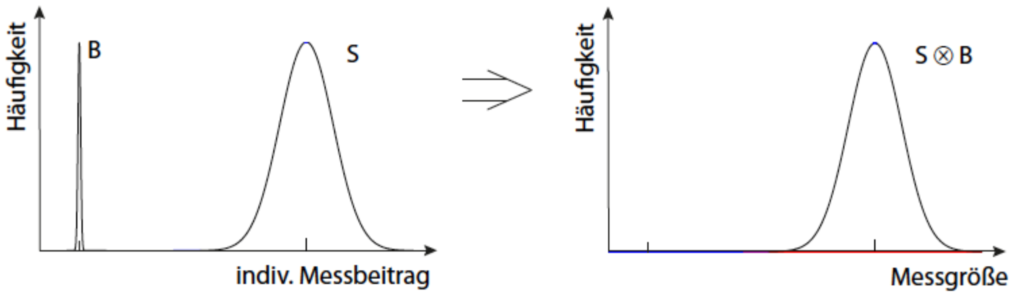


$$\boxed{\sigma^2 = \lim_{T\to\infty} \frac{1}{T}\int_0^T (I(t) - I_0)^2 dt}$$

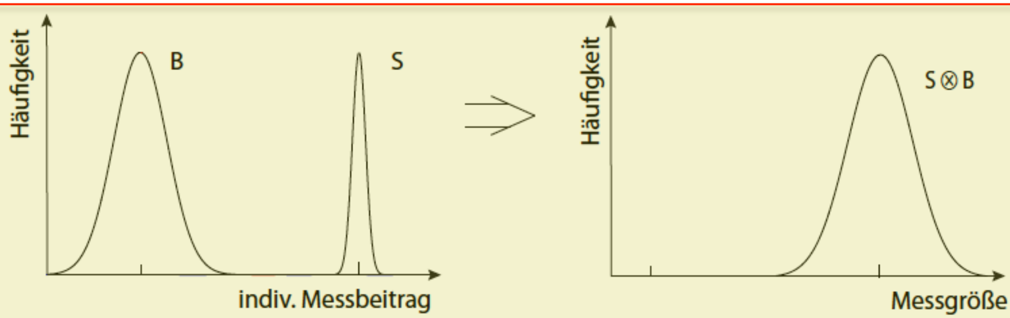
$$dP_n/df = \frac{1}{R}\, d\langle u^2\rangle/df = R\, d\langle i^2\rangle/df$$

When to care about noise …

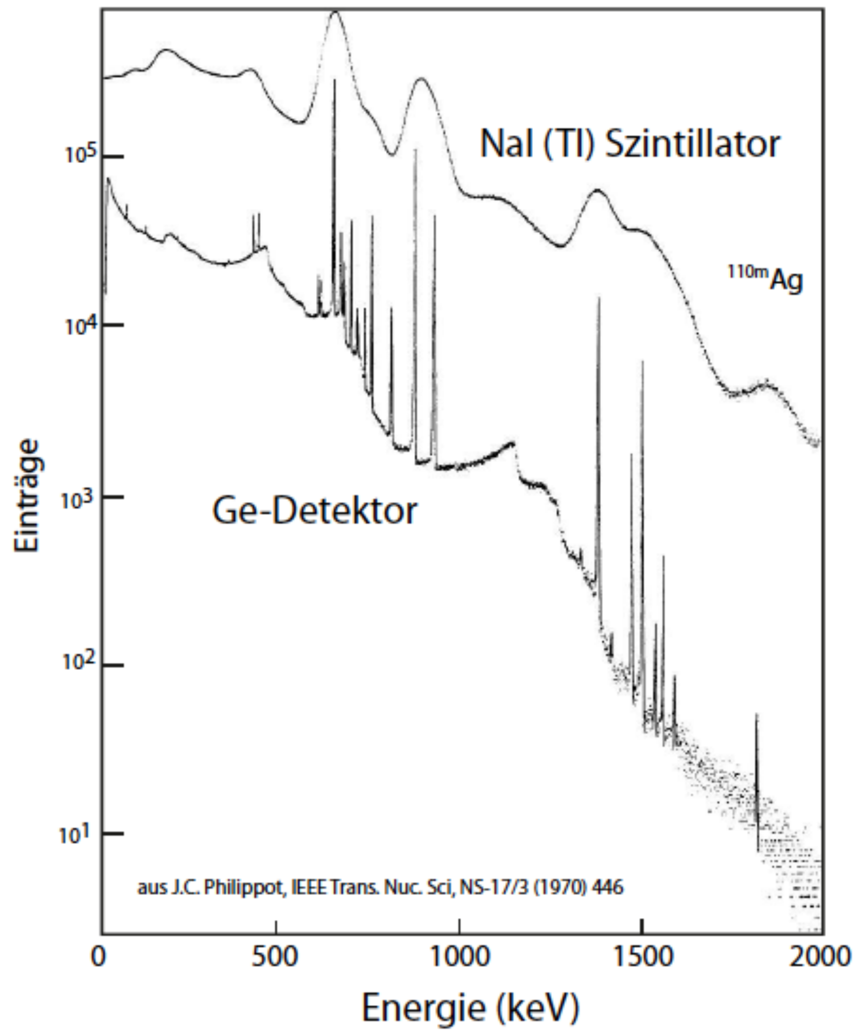
- always …
- but particularly, when situation is like this



(a) $\sigma_S \gg \sigma_B$



(b) $\sigma_S \ll \sigma_B$



- even if you are not interested in an energy measurement, remember … thresholds

Noise

shot noise

white noise

current noise

resistor noise

switching noise

series noise

flicker noise

popcorn noise

Nyquist Noise

parallel noise

Johnson Noise

kT/C noise

Thermal noise

RTS noise

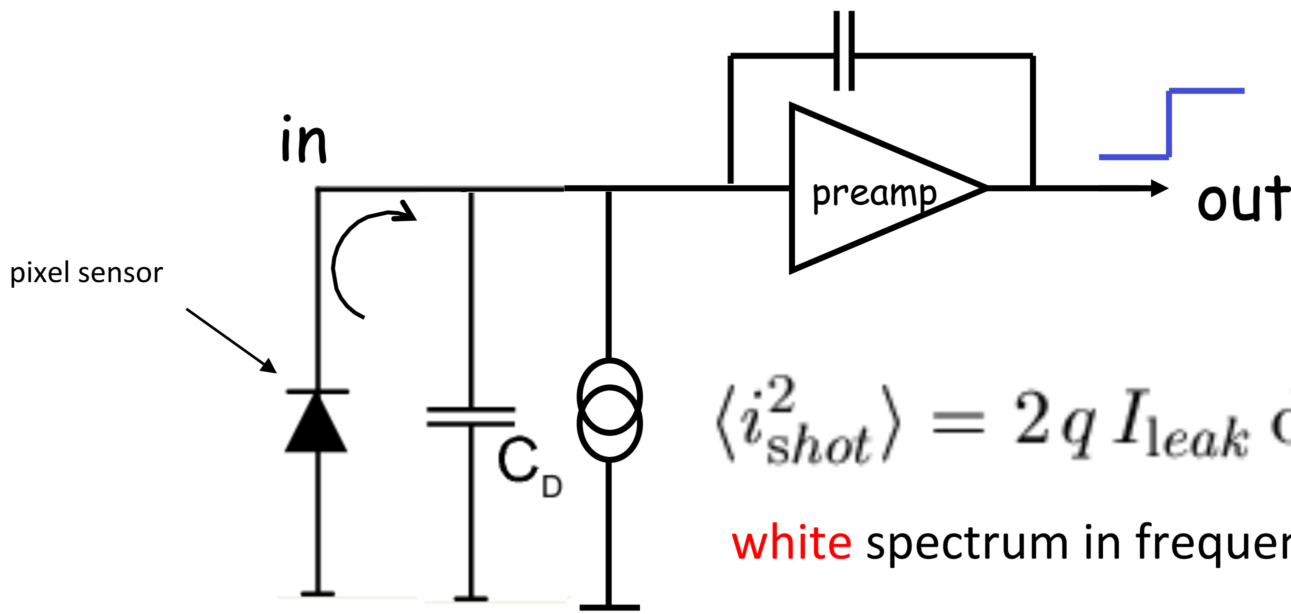
1/f noise

Noise in a pixel/strip detector (ionisation detector)

three physical noise sources:

number fluctuations of quanta	→	1. shot noise	$\langle i^2 \rangle = 2q \langle i \rangle\, df$
		2. 1/f noise	$\langle i^2 \rangle = \text{const.}\ 1/f\, df$
velocity fluctuations of quanta	→	3. thermal noise	$\langle i^2 \rangle = 4kT / R\, df$

where do they appear in a typical pixel detector readout chain ?



$$\langle i^2_{shot} \rangle = 2q\, I_{leak}\, \mathrm{d}f$$

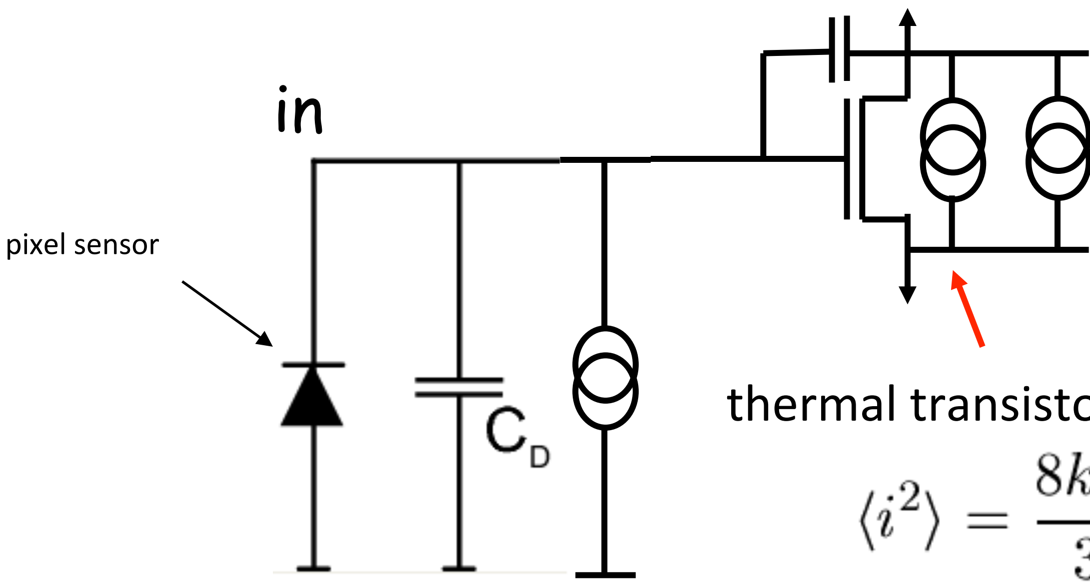
white spectrum in frequency f

Noise in a pixel/strip detector (ionisation detector)

three physical noise sources:

number fluctuations of quanta	→	1. shot noise	$\langle i^2 \rangle = 2q \langle i \rangle \, df$
		2. 1/f noise	$\langle i^2 \rangle = \text{const.} \; 1/f \, df$
velocity fluctuations of quanta	→	3. thermal noise	$\langle i^2 \rangle = 4kT / R \, df$

where do they appear in a typical pixel detector readout chain ?



transistor 1/f noise

$$\langle i^2 \rangle = \frac{K_f}{C_{ox} W L} \frac{1}{f} \, \mathrm{d}f$$

thermal transistor channel (white) noise

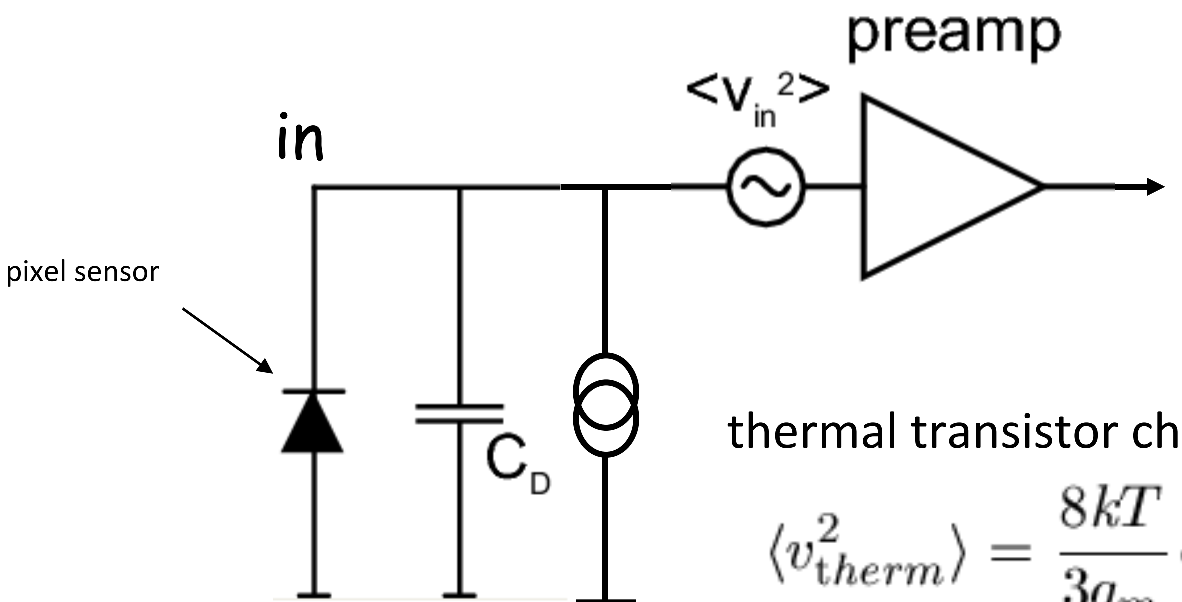
$$\langle i^2 \rangle = \frac{8kT}{3} g_m \, \mathrm{d}f$$

Noise in a pixel/strip detector (ionisation detector)

three physical noise sources:

number fluctuations of quanta	→	1. shot noise	$\langle i^2 \rangle = 2q \langle i \rangle\, df$
		2. 1/f noise	$\langle i^2 \rangle = \text{const.}\ 1/f\, df$
velocity fluctuations of quanta	→	3. thermal noise	$\langle i^2 \rangle = 4kT / R\, df$

where do they appear in a typical pixel detector readout chain ?



transistor 1/f noise

$$\langle v_{1/f}^2 \rangle = \frac{K_f}{C_{ox} W L} \frac{1}{f}\, \mathrm{d}f$$

thermal transistor channel noise

$$\langle v_{therm}^2 \rangle = \frac{8kT}{3g_m}\, \mathrm{d}f$$

Noise in a pixel/strip detector (ionisation detector)

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equivalent noise charge $$\mathrm{ENC} = \frac{\text{noise output voltage (rms)}}{\text{signal output voltage for the input charge of } 1\mathrm{e}^-}$$

$$ENC^2_{tot} = ENC^2_{shot} + ENC^2_{therm} + ENC^2_{1/f}$$

charge sensitive preamplifier only

$$ENC_{\mathrm{shot}} = \sqrt{\frac{I_{leak}}{2q}\tau_f} = 56e^- \times \sqrt{\frac{I_{leak}}{\mathrm{n}A}\frac{\tau_f}{\mu s}}$$

$$ENC_{\mathrm{therm}} = \frac{C_f}{q}\sqrt{\langle v^2_{\mathrm{therm}}\rangle} = \sqrt{\frac{kT}{q}\frac{2C_D}{3q}\frac{C_f}{C_{load}}} = 104e^- \times \sqrt{\frac{C_D}{100\,\mathrm{fF}}\frac{C_f}{C_{load}}}$$

$$ENC_{1/\mathrm{f}} \approx \frac{C_D}{q}\sqrt{\frac{K_f}{C_{ox}WL}}\sqrt{\ln\left(\tau_f\frac{g_m}{C_{load}}\frac{C_f}{C_D}\right)} = 9e^- \times \frac{C_D}{100\,\mathrm{fF}}(\text{for NMOS trans.})$$

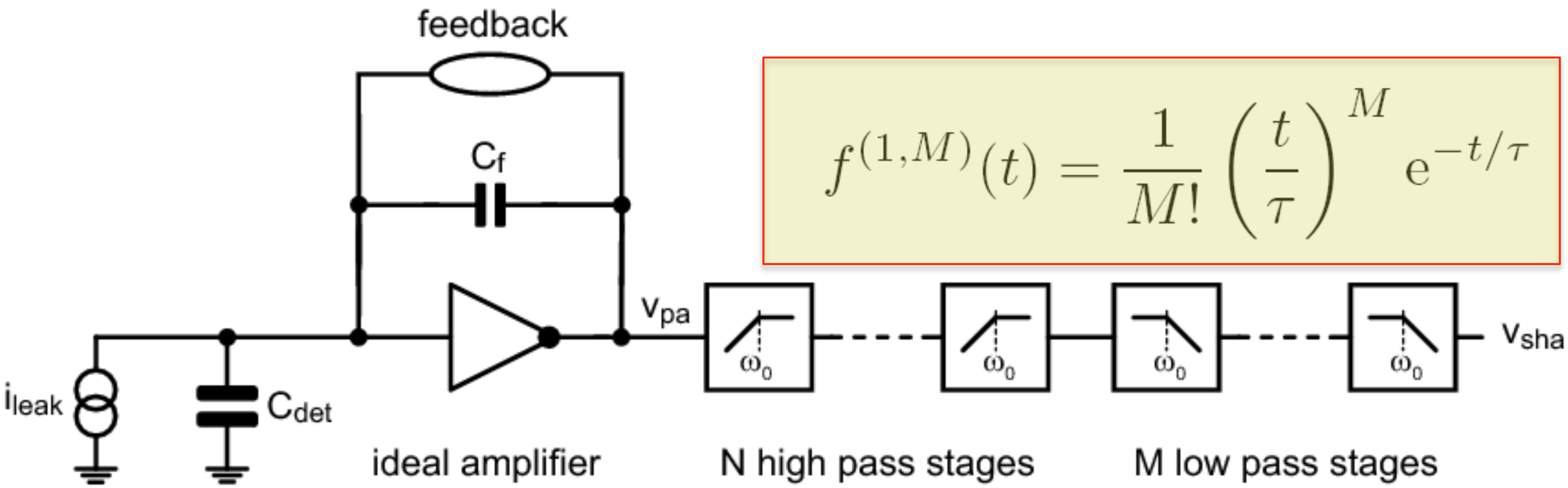
W, L = width and length of trans. gate
K_f = 1/f noise coefficient
C_{ox} = gate oxide capacitance

C_f = feedback capacitance
C_{load} = load capacitance
C_D = detector capacitance
τ_f = feedback time constant

reference
Rossi, Fischer, Rohe, Wermes
Pixel Detectors. Springer 2006

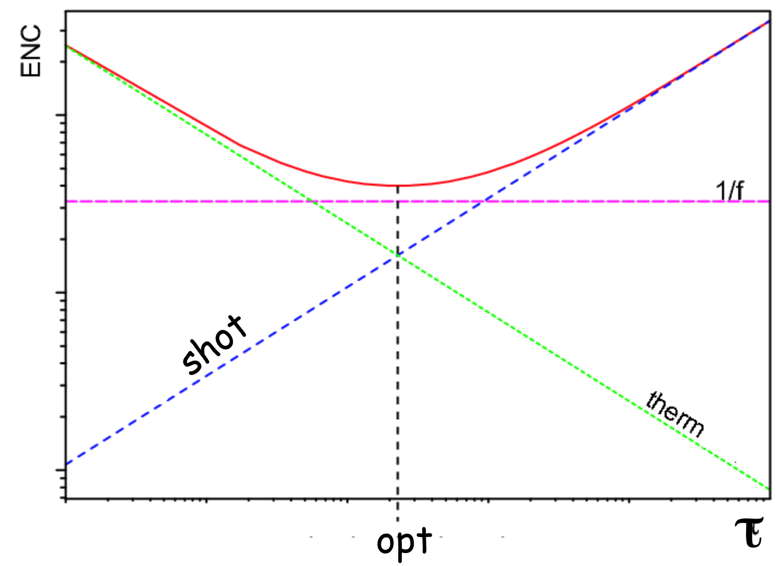
Noise in a pixel/strip detector (ionisation detector)

… with an additional filter amplifier (shaper) being the band width limiter



$$f^{(1,M)}(t) = \frac{1}{M!}\left(\frac{t}{\tau}\right)^M \mathrm{e}^{-t/\tau}$$

$$\mathrm{ENC}^2(e^2) = 11\, I_0(\mathrm{nA})\,\tau(\mathrm{ns}) + 740\,\frac{1}{WL(\mu\mathrm{m}^2)}\,C_D^2(100\,\mathrm{fF}) + 4000\,\frac{1}{g_m(\mathrm{mS})}\,\frac{C_D^2(100\,\mathrm{fF})}{\tau(\mathrm{ns})}$$



Noise in a pixel/strip detector (ionisation detector)

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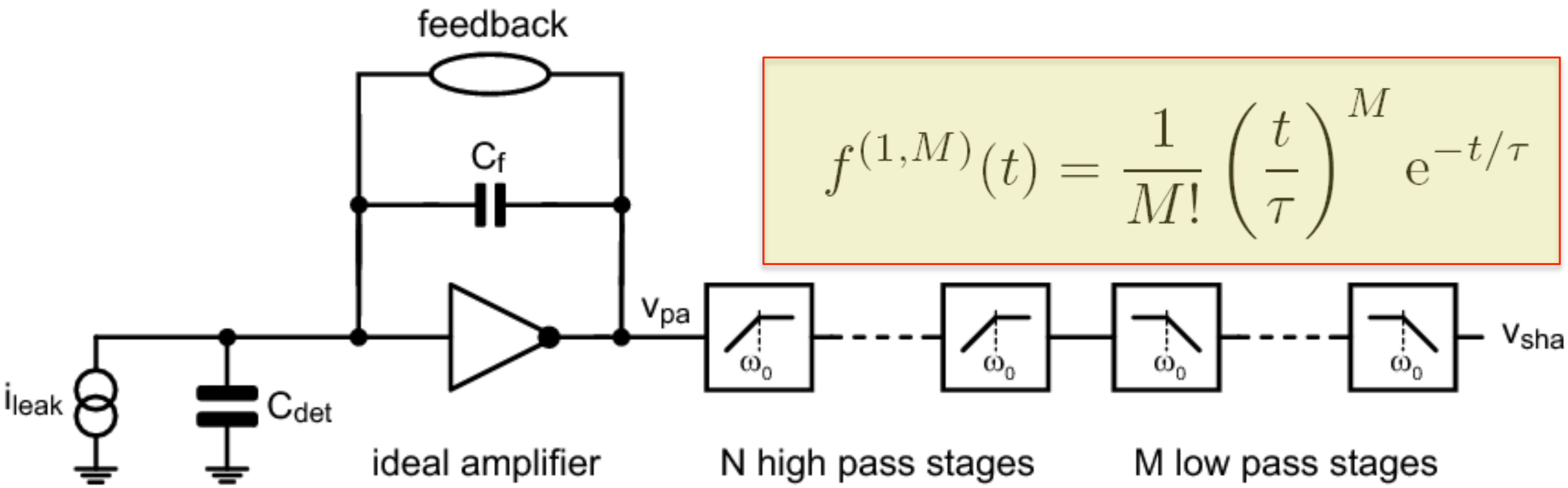
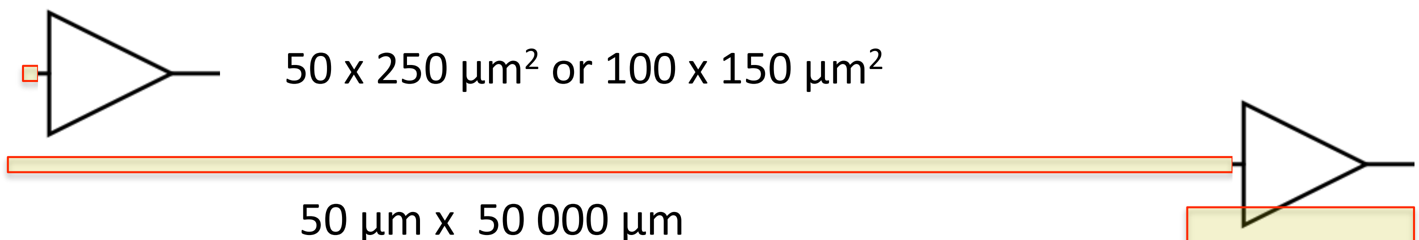
… with an additional filter amplifier (shaper) being the band width limiter



$$f^{(1,M)}(t) = \frac{1}{M!}\left(\frac{t}{\tau}\right)^M e^{-t/\tau}$$

comparing pixels and strips



	C_D	I_0	τ	W	L	g_m	ENC therm	ENC 1/f	ENC shot	ENC tot
pixel	200 fF	1 nA	50 ns	20 µm	0.5 µm	0.5 mS	25 e⁻	17 e⁻	24 e⁻	**40 e⁻**
strip	20 pF	1 µA	50 ns	2000 µm	0.4 µm	5 mS	800 e⁻	200 e⁻	750 e⁻	**1100 e⁻**