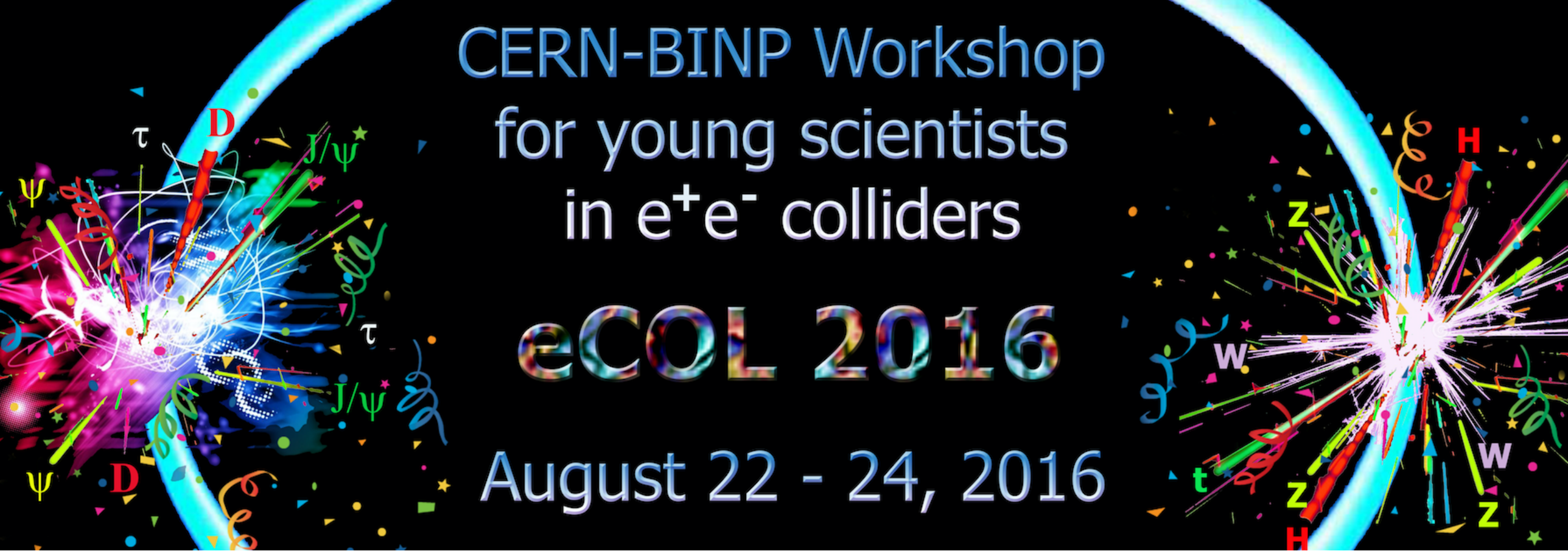


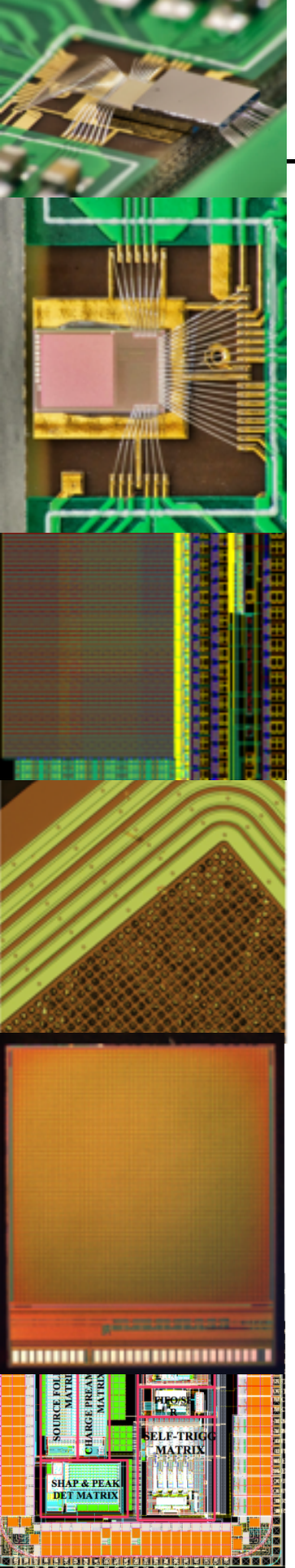
CLIC vertex and tracker R&D

Magdalena Munker (CERN, University of Bonn)
On behalf of the CLICdp collaboration

24 August 2016

SPONSORED BY THE
Federal Ministry of Education and Research

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

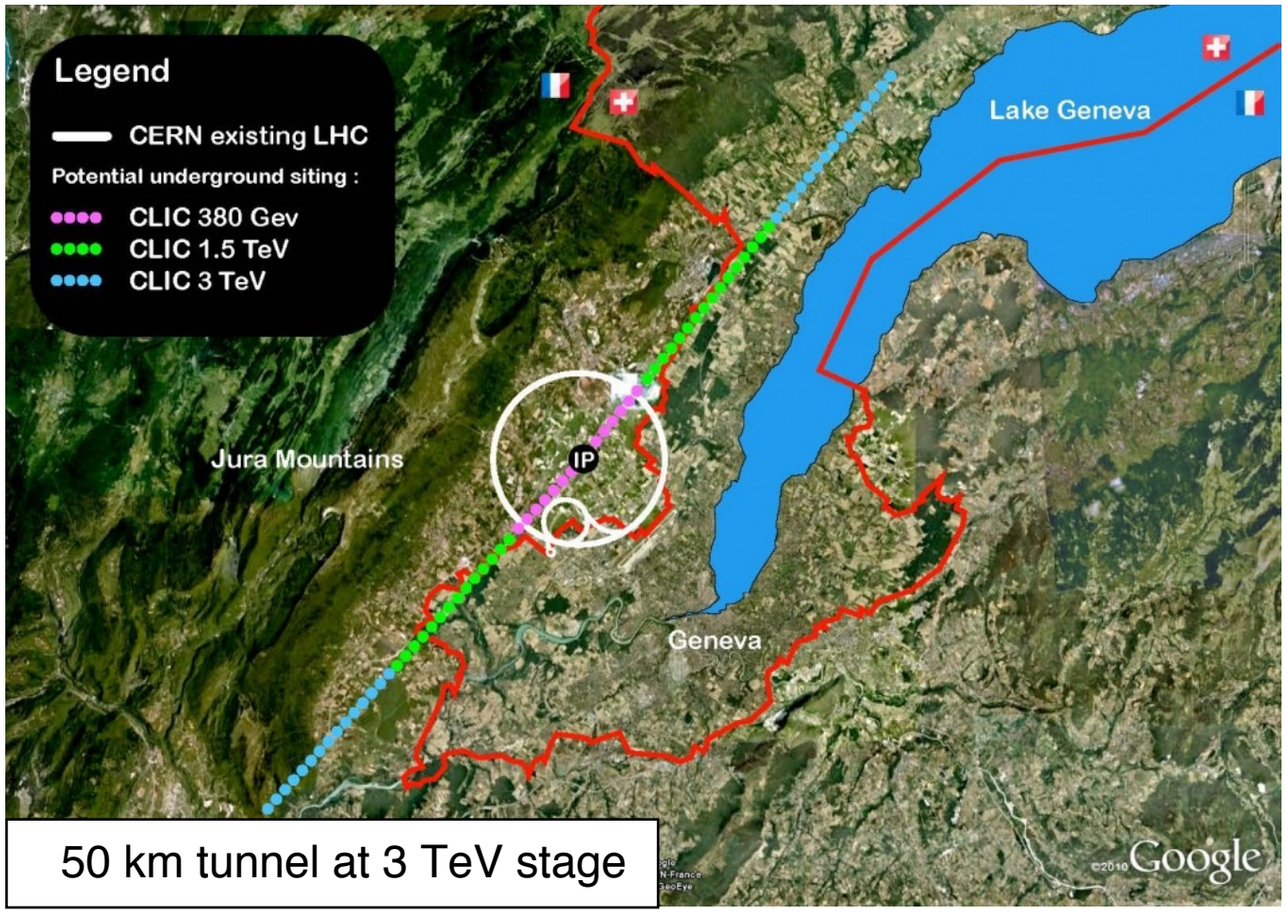


Outline

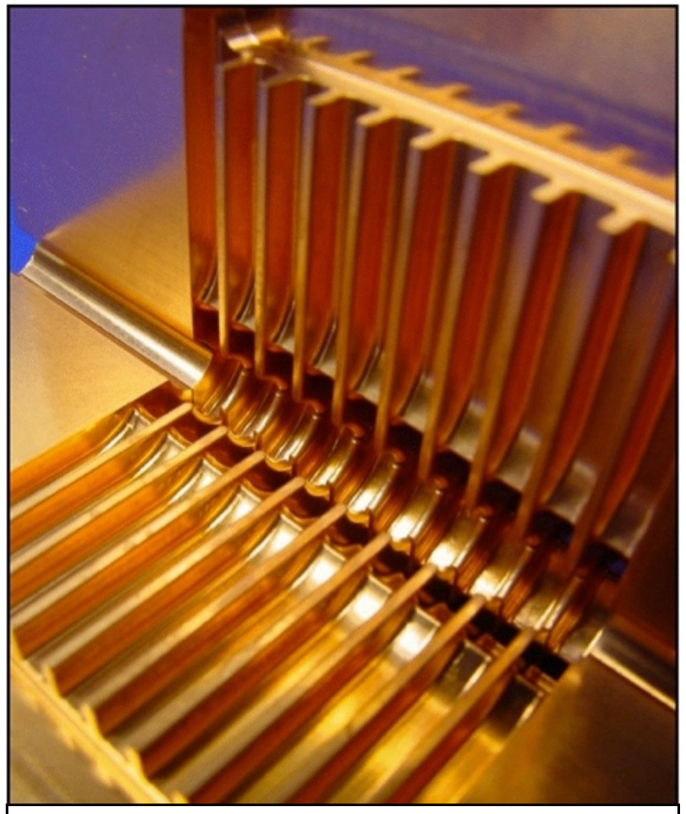
- Introduction
- Requirements for the vertex and tracking detector of CLIC
- R&D on sensor and readout technologies:
  - Planar sensor assemblies
  - HV-CMOS active sensors and capacitive coupling
  - Integrated CMOS technologies
- Summary

CLIC - the Compact Linear Collider

- Proposed e^+e^- linear collider at CERN for the post HL-LHC phase
- Energy range from a few hundred GeV up to 3 TeV (two-beam acceleration with ~100 MV/m)



50 km tunnel at 3 TeV stage



CLIC accelerating structure

↳ See talk of Florian Pitters on Monday, *The CLIC Detector Concept*

- **Physics goals:**
  - Precision measurements of Standard Model Processes (Higgs, Top)
  - Precision measurements of new physics potentially discovered at 14 TeV LHC
  - Search for new physics, unique sensitivity to particles with electroweak charge

↳ See lecture from Philipp Roloff on Monday, *Physics at high-energy e+e- colliders*

Requirements for the vertex and the tracker

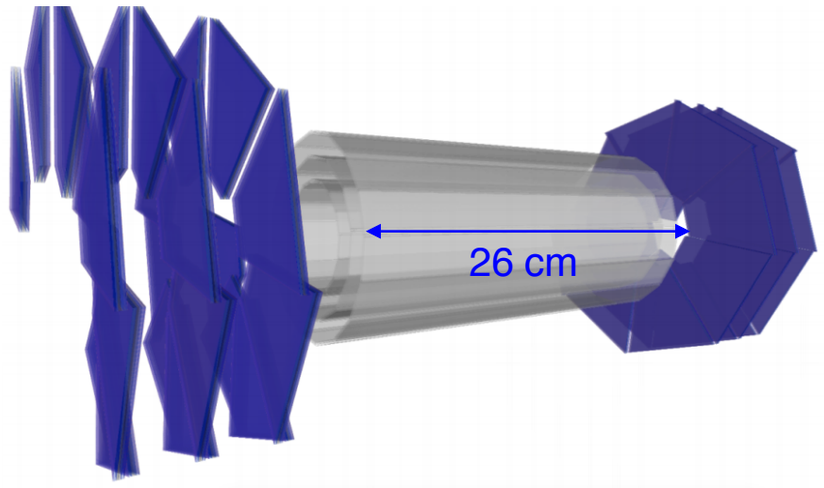
Vertex:

Efficient tagging of of heavy flavour quarks:

→ Good single point resolution of 3 µm
  → Small pixels with a pitch of ~ 25 µm and analog read out

→ Low material budget of ≲ 0.2 % X_0 per layer
  Forced airflow cooling & low-power electronics (≲ 50 mW/cm^2)

Vertex detector layout:



Tracker:

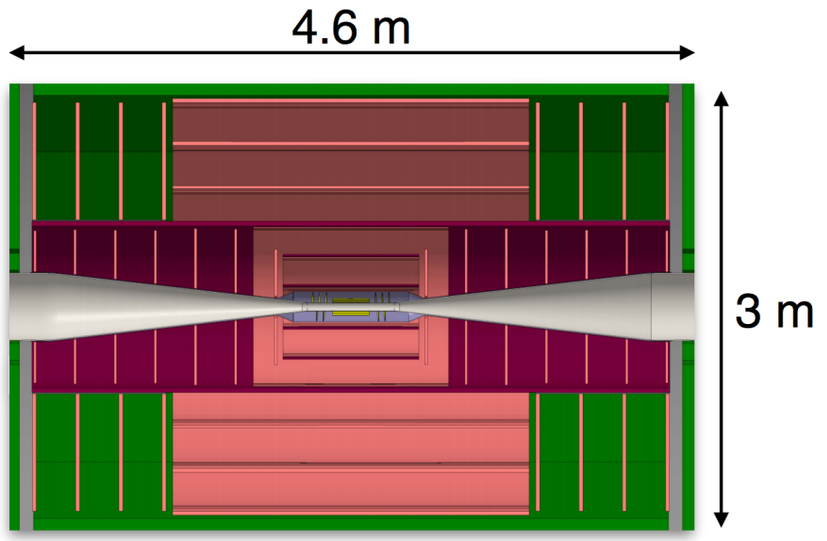
Good momentum resolution:

→ Good single point resolution of 7 µm (pitch of ~ 50 µm, t.b.c.)

→ Low material budget of ≲ 2 % X_0 per layer:
  → Low-mass supports, cabling and cooling

→ Occupancies from beam-beam interactions define readout granularity:
  → 50 µm pitch and 1-10 mm strip lengths

Tracker layout:

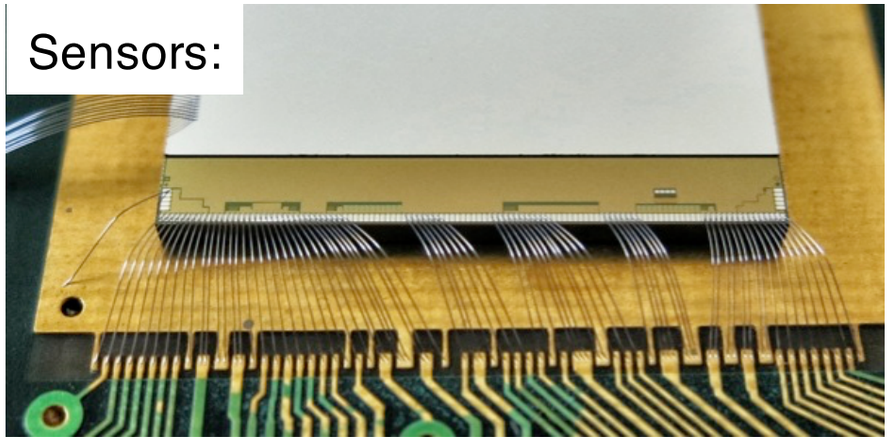


Both:

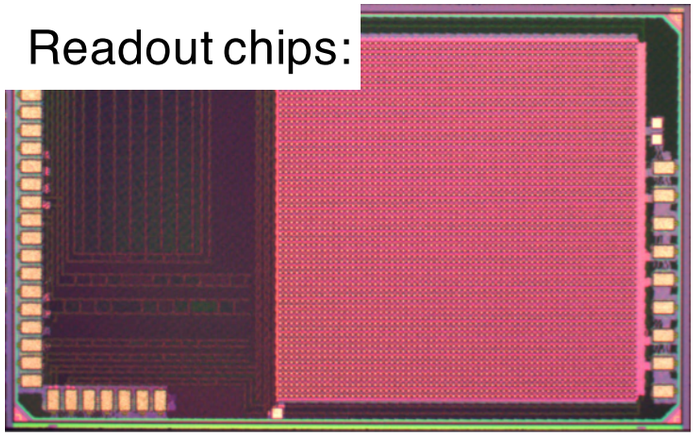
- Fast time slicing of ~ 10 ns to suppress background from beam-beam interactions
- Low radiation exposure ~ 10^4 times below LHC

CLIC vertex and tracker R&D programme

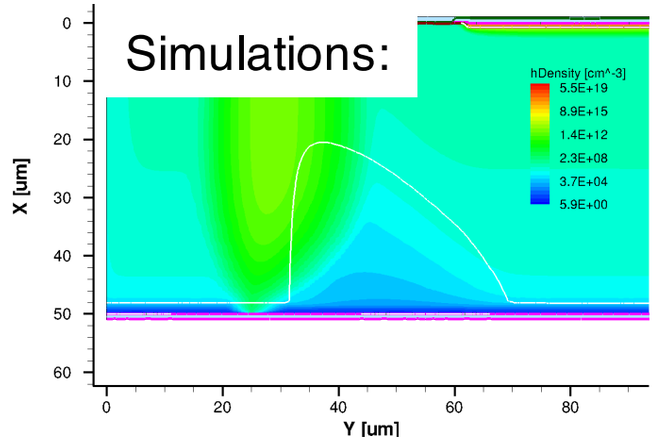
Sensors:



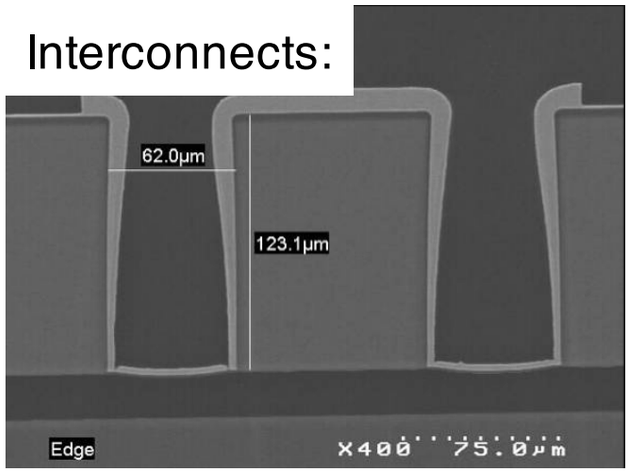
Readout chips:



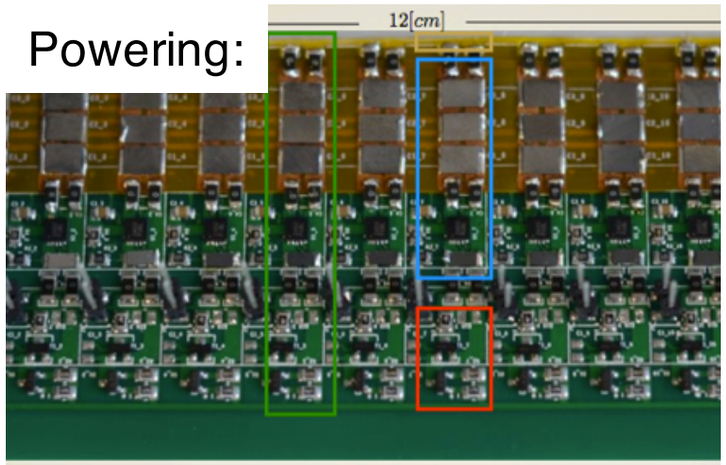
Simulations:



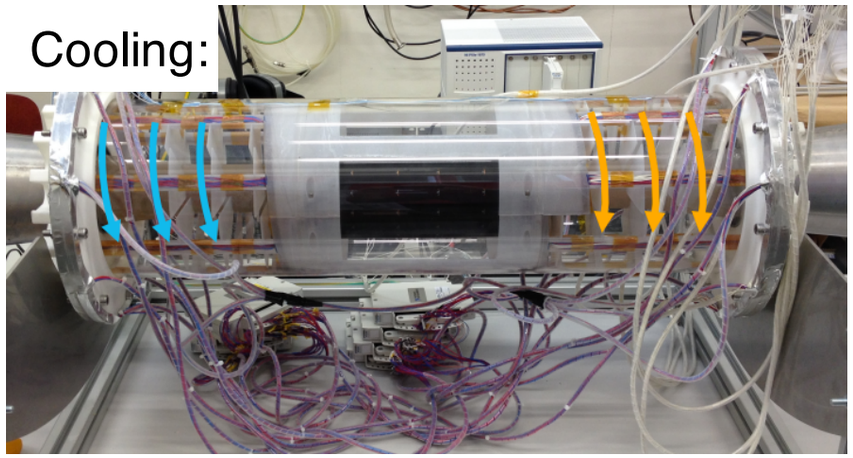
Interconnects:



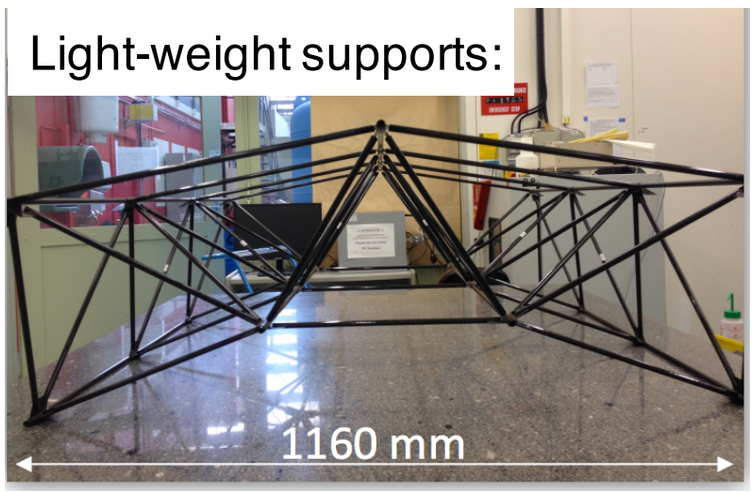
Powering:



Cooling:



Light-weight supports:



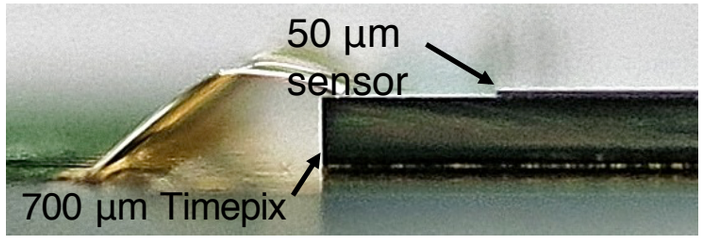
Integrated R&D effort addressing vertex & tracker simultaneously:

→ A few examples of sensor and readout technologies are presented in the following

Timepix(3) thin planar sensor assemblies

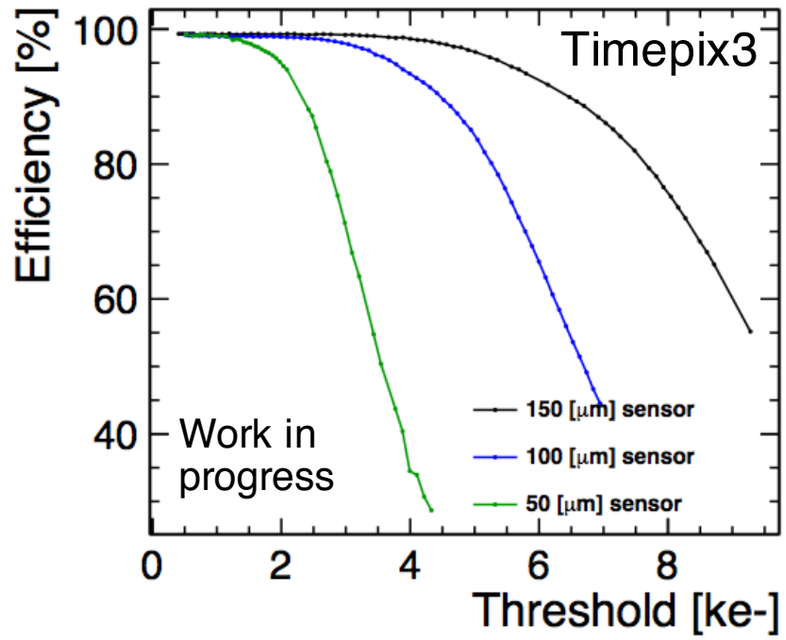
- Planar sensor assemblies with 55 µm pitch (Micron, Advacam)
- Readout with Timepix / Timepix3
- 50-500 µm sensor thickness, 100-700 µm readout chip thickness

Timepix assembly:

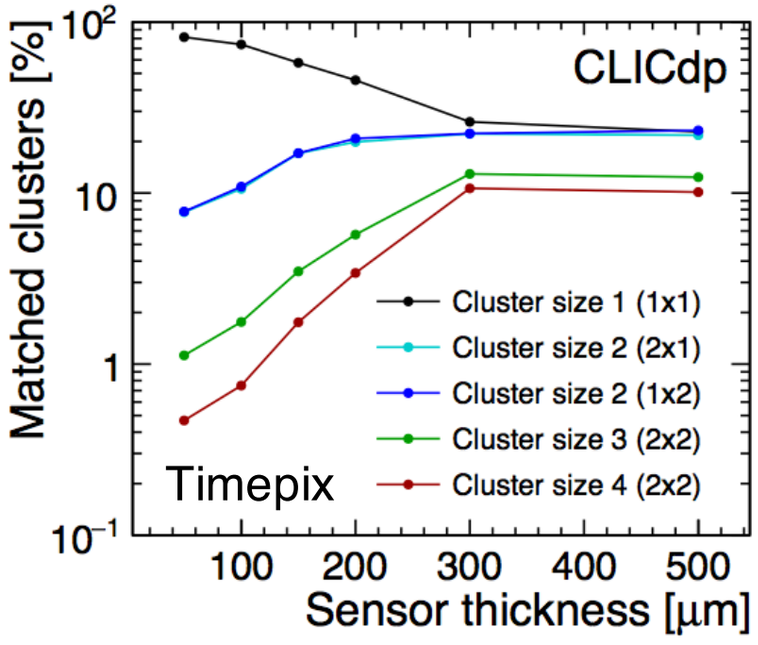


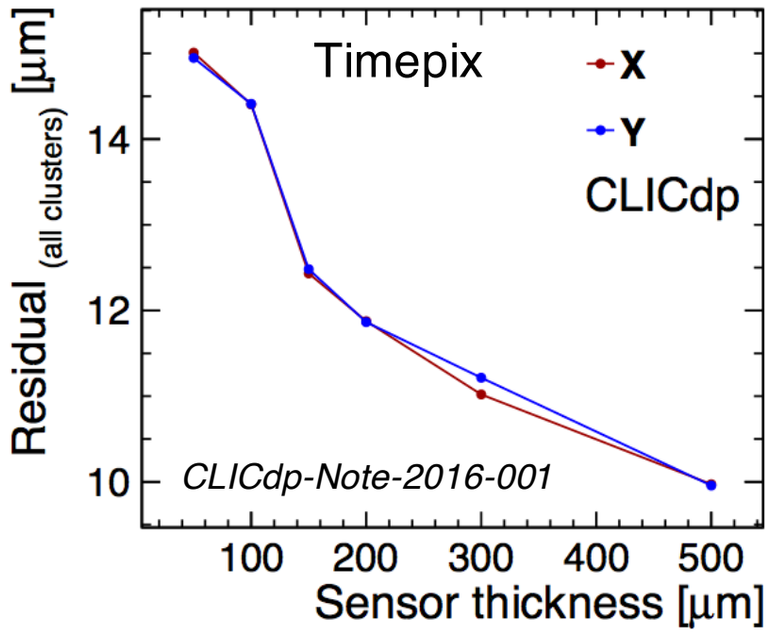
Test beam results:

- Investigate efficiency for different threshold levels
- Low noise allows for low detection threshold (~ 1000 electrons)
- ~ 99% efficiency with 50 µm thin sensor demonstrated



- Resolution depends strongly on charge sharing
- Less charge sharing for thin sensors
  → Degradation of resolution with sensor thickness
- Resolution ~ 14 µm for 50 µm thin sensor

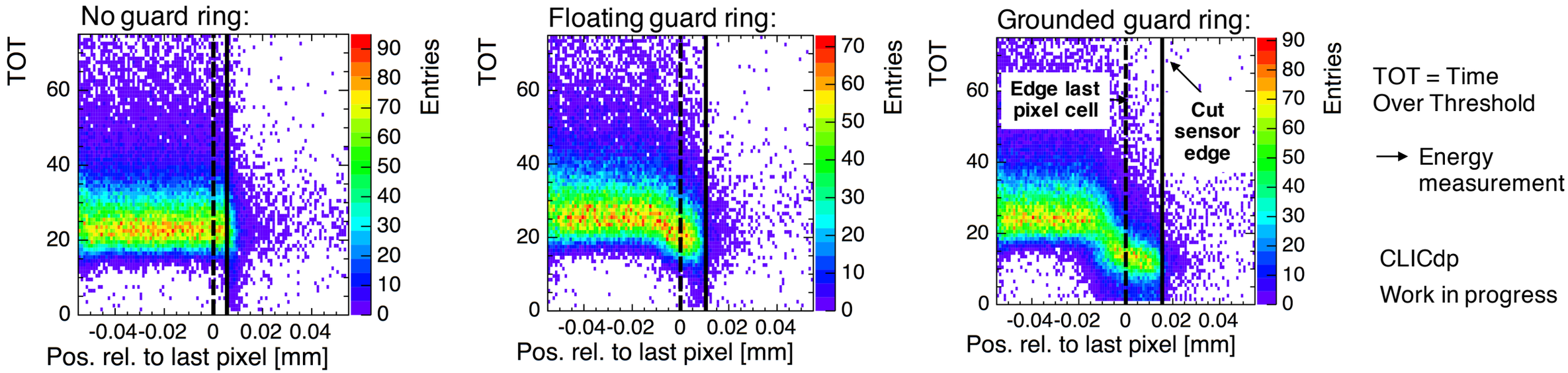




Timepix3 active edge sensor assemblies

- Active edge sensors provide possibility of seamless tiling → reduced material budget
- 50 µm thin planar sensors with active edge and Timepix3 readout
- Deep Reactive-Ion Etching (DRIE) process to cut sensor edge
- Extend backside electrode to the cut edge of the sensor
- Different guard ring designs to create a smooth voltage drop between last pixel implant and edge

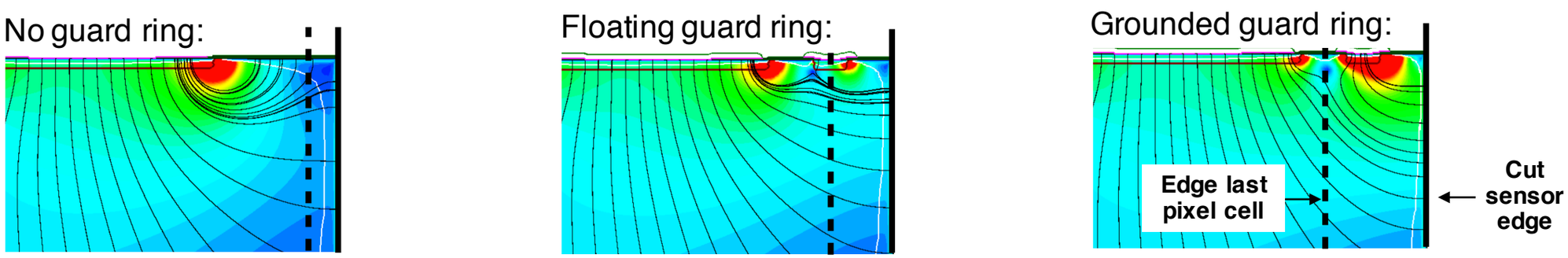
Test beam results:



→ No / less signal loss at the edge of the sensor for layout with no guard ring and floating guard ring

→ Proof of principle achieved

Finite element TCAD simulation:

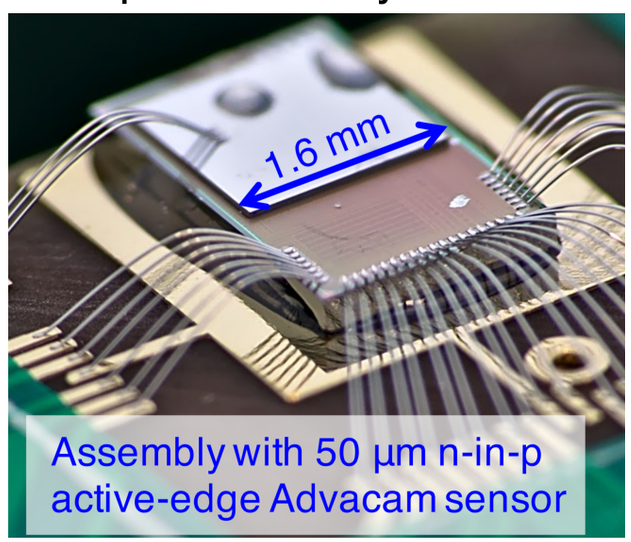


→ TCAD simulation explains signal loss at the edge for the layout with a grounded guard ring

CLICpix 25 µm pitch planar sensor assemblies

- CLICpix demonstrator chip with 64x64 pixel matrix bump bonded to 200, 150 and 50 µm thick planar sensors
- 4-bit Time over Threshold (ToT) and Time of Arrivel (ToA) readout: ToT → Energy measurement, ToA → timing measurement
- Single-chip bump-bonding process for 25 µm pitch developed at SLAC (C. Kenney, A. Tomada)

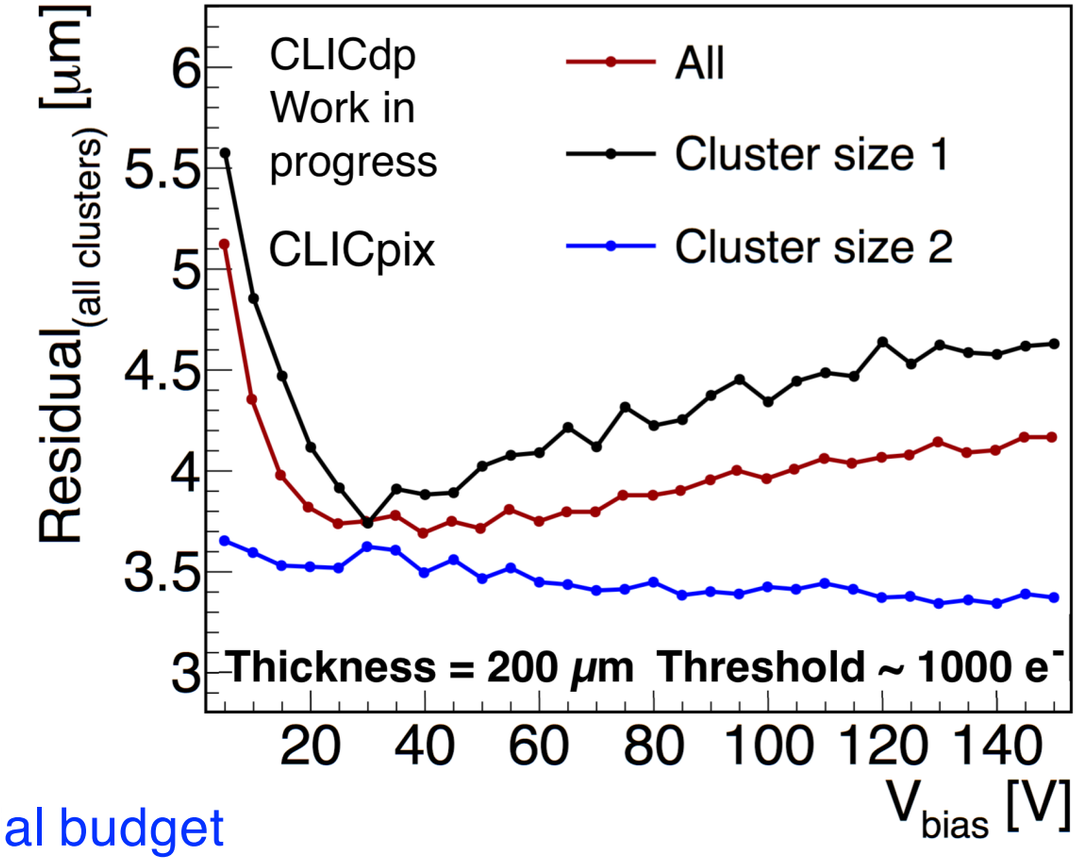
CLICpix assembly:



Test beam results, 200 µm assembly:

- Higher bias voltage leads to thicker depletion zone
→ Resolution improves with higher bias voltage until the sensor is fully depleted

- Higher bias voltage leads to higher / more homogeneous field in sensor
→ Less charge sharing
→ Resolution degrades for over depletion



- Single point resolution ~ 3 - 4 µm, efficiency ~ 99 %

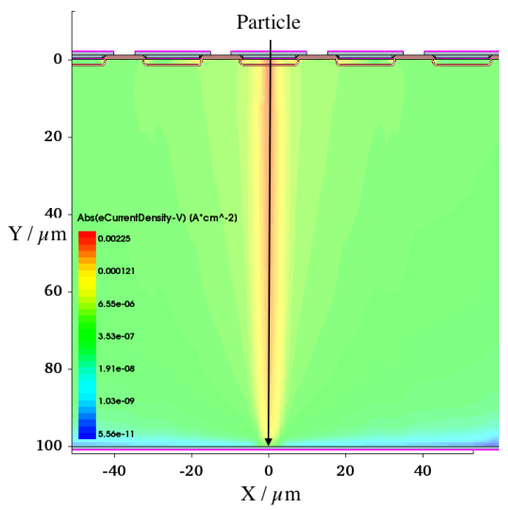
→ Promising results but too thick sensor to reach low material budget

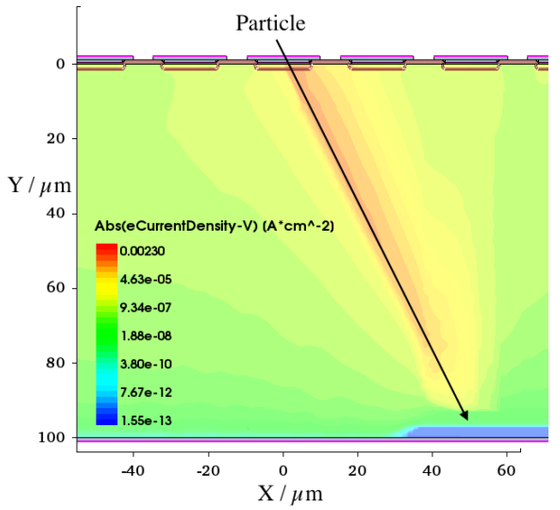
→ Ongoing validation of assembly with 50 µm thick active edge sensor

Simulation of planar sensor performance

Simulation chain:

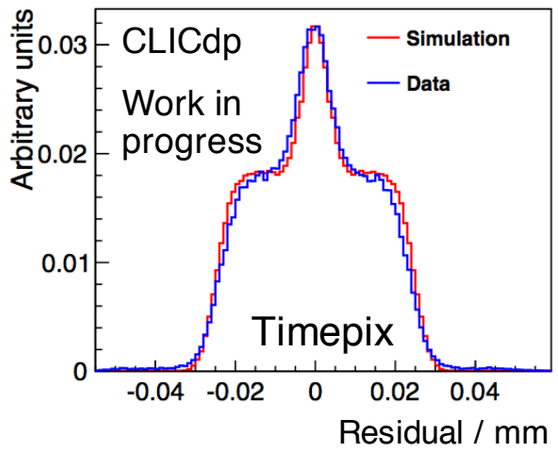
1. GEANT4 simulation of energy deposit in silicon sensor
2. Finite element TCAD simulation of silicon sensor
3. Fast parametric model of front end electronics and energy fluctuations
4. Reconstruction and calculation of observables

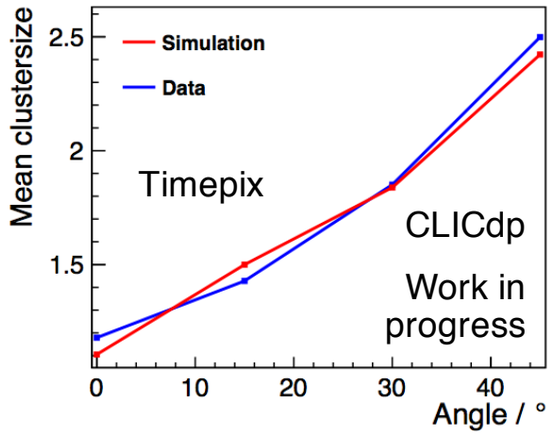




Validation of simulation using Timepix test-beam results:

- Simulation reproduces distribution of residual
- Simulation reproduces dependency of charge sharing on incident angle

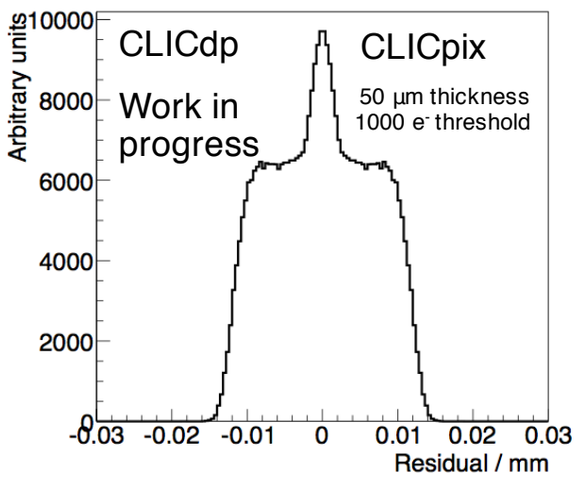


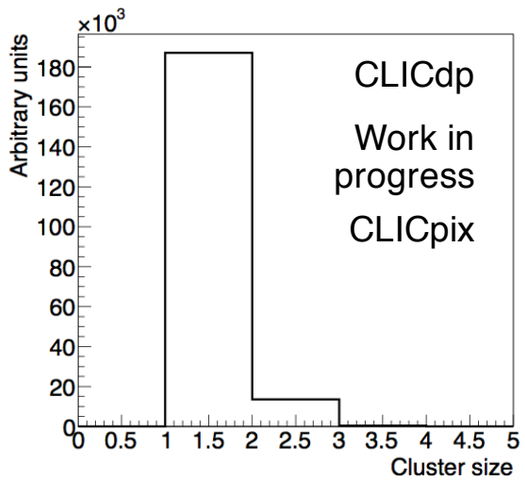


Application of simulation to predict performance of 50 µm thick CLICpix planar sensor assemblies:

- Resolution limited to ~ 6 µm due to less charge sharing in thin sensors

→ To be confirmed in test-beam study of thin CLICpix assembly (currently ongoing)





HV-CMOS active sensor assemblies

Capacitive Coupled Pixel Detector (CCPD) as active sensor:

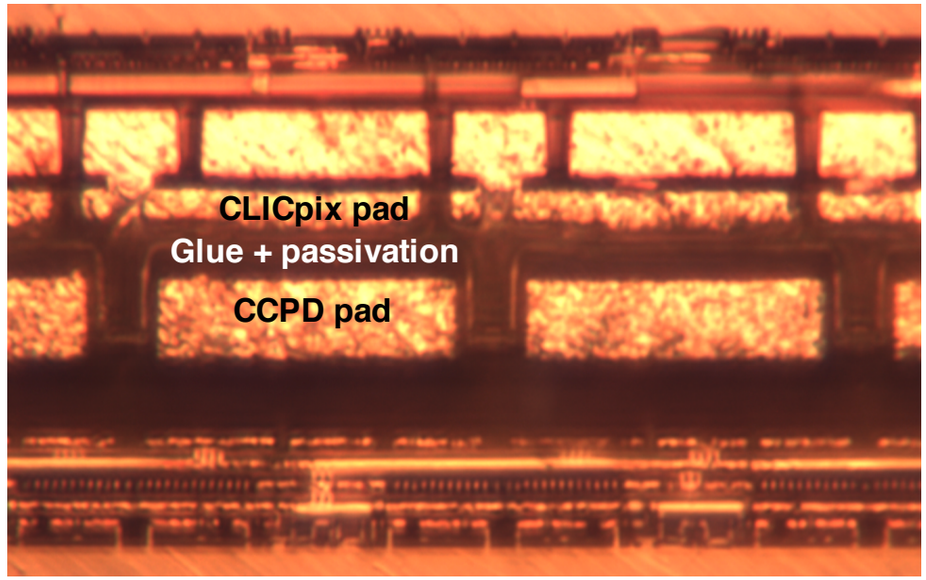
- Commercial 180 nm High-Voltage-CMOS process
- Deep n-well to shield electronics from the substrate bias
- HV substrate bias of ~ 60 V

→ Fast signal by drift due to creation of depletion layer

- Amplifier stages implemented in each pixel of sensor (simulated peaking time of ~ 120 ns)
- Amplifier output coupled through layer of glue to CLICpix ASIC (25 µm pitch)

→ No bump-bonding

Optical microscope picture:



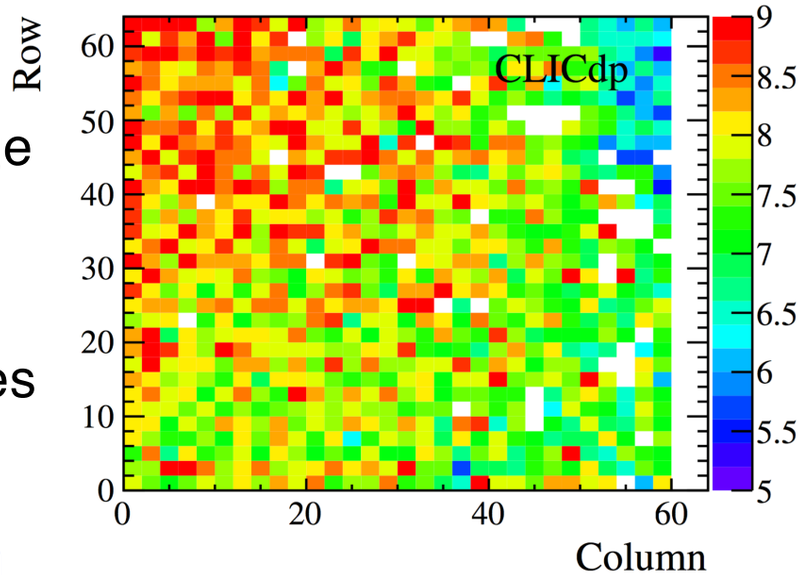
Test beam results:

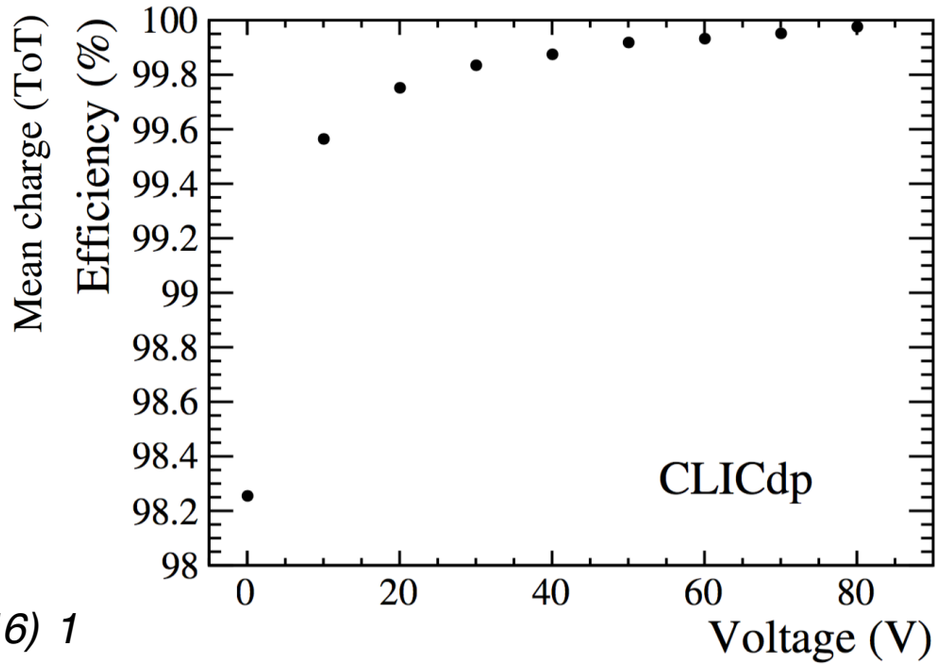
- Non-uniformity of mean charge due to non uniformity of glue layer in early assemblies

→ Improved for newer assemblies

- Efficiency ~ 99.9 %
- Single point resolution ~ 6 µm

→ Proof of principle achieved





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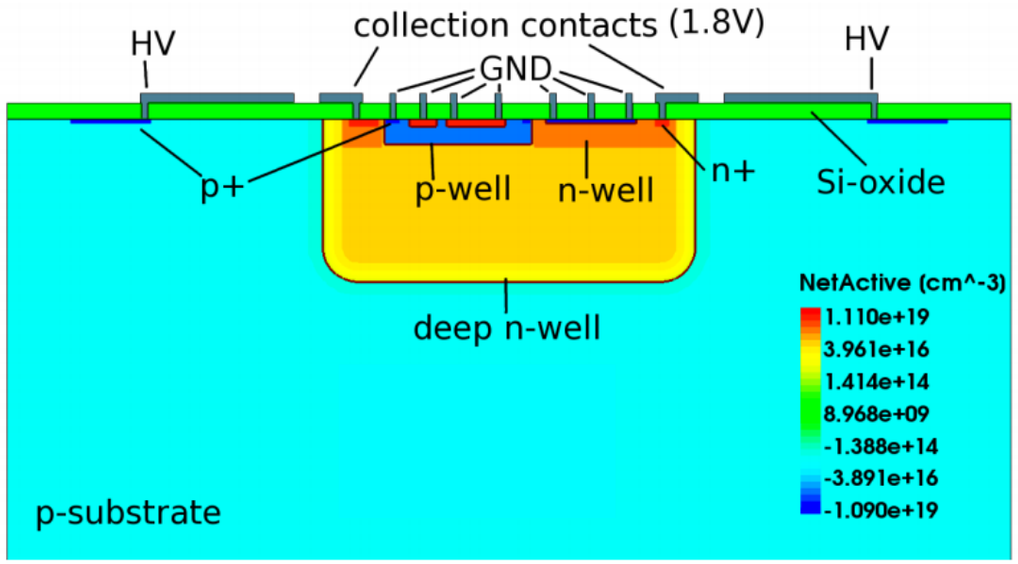
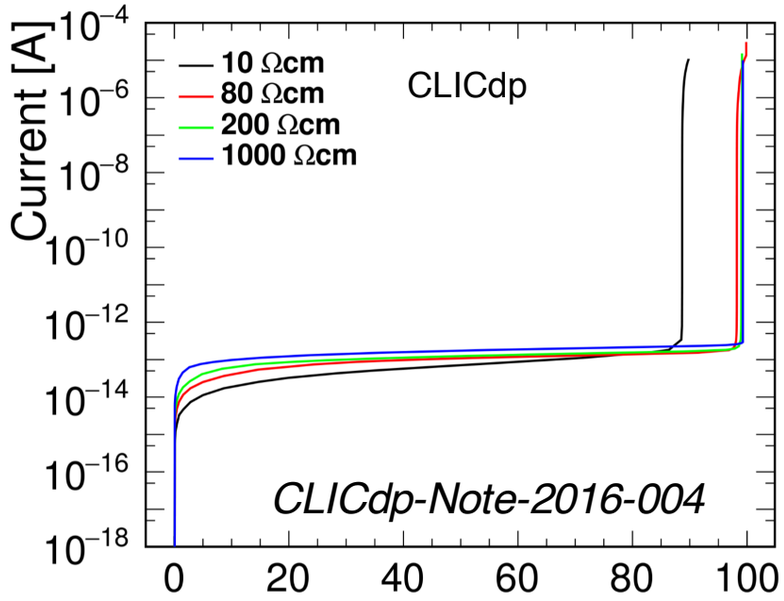
Simulation of HV-CMOS sensors

Implementation of CCPDv3 pixel structure in 2d TCAD simulation:

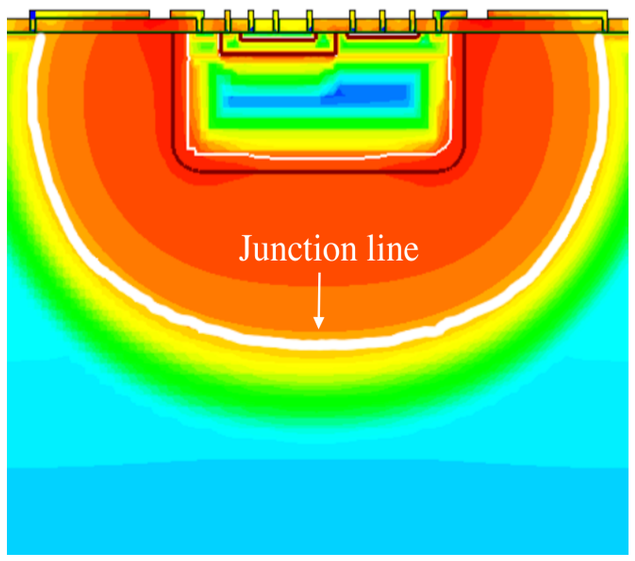


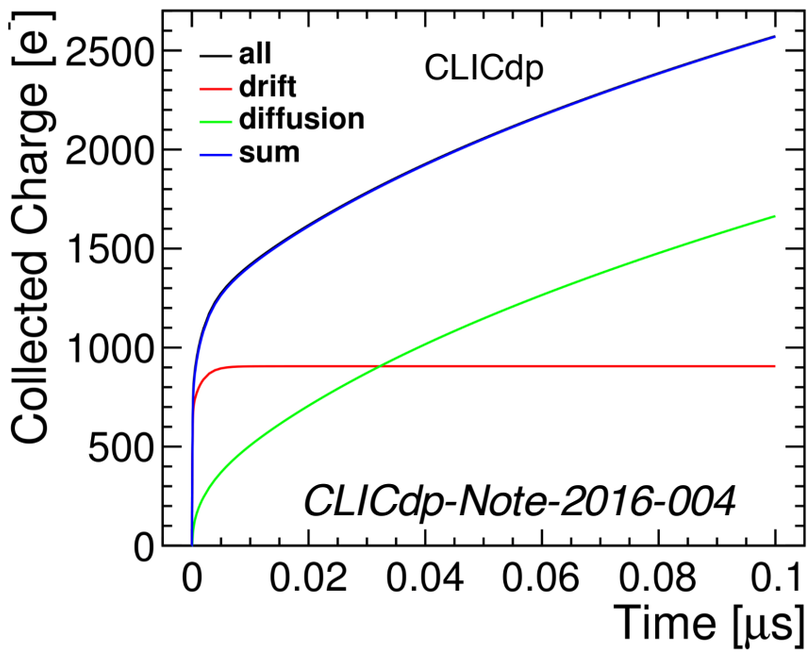


- Simulation reveals pixel layout as reason for breakdown at ~ 90 V

→ Simulation used to improve next CCPD version

Transient simulation of collected charge in depleted and non depleted region:





- Fast charge collection time of ~ 10 ns by drift in the depleted region
- Significant slower charge collection time by diffusion in non depleted region

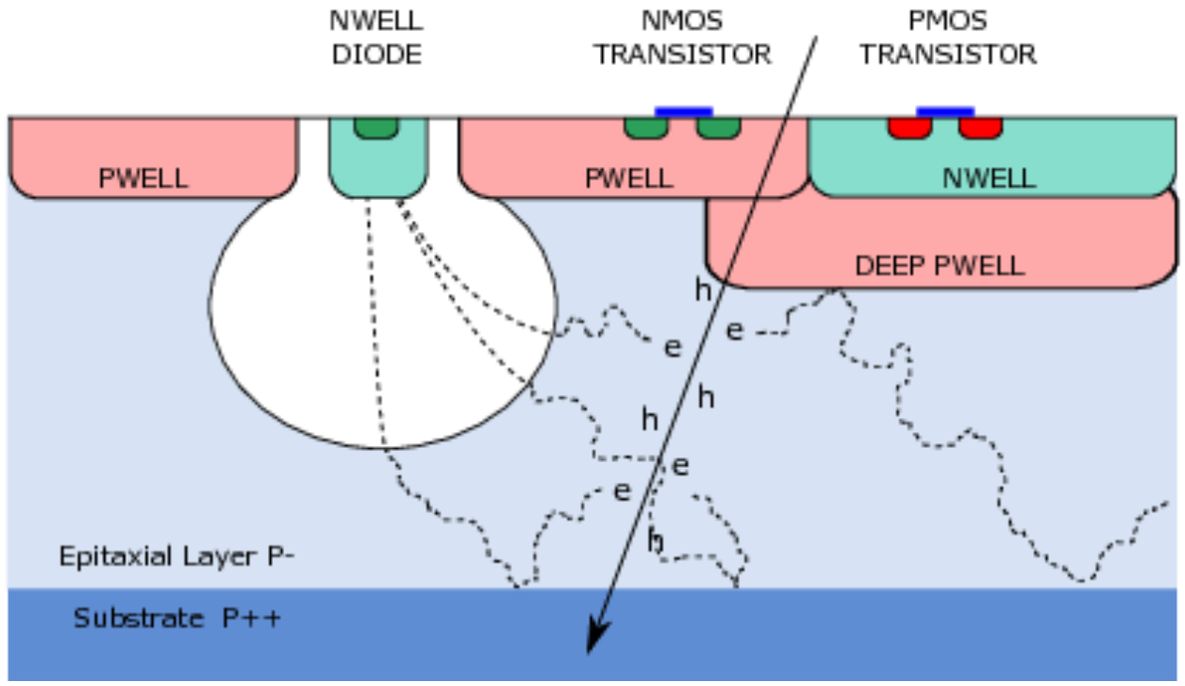
→ Simulation used to gain understanding of sensor performance

The ALICE investigator chip

ALICE INVESTIGATOR, monolithic HR-CMOS test-chip *(W. Snoeys, J. W. Van Hoorne et. al.)*:

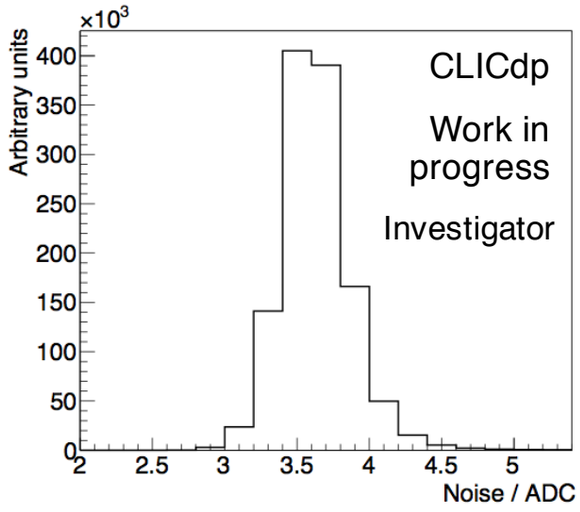
- Developed by the ALICE collaboration to test analogue performance
- 180 nm High Resistivity (HR) CMOS process
- 15-40 µm thick epitaxial layer (1-8 kΩcm)
- 134 mini-matrices with different pixel layouts
- 8x8 pixel matrix per mini-matrix
- Optimisation of collection-diode geometry

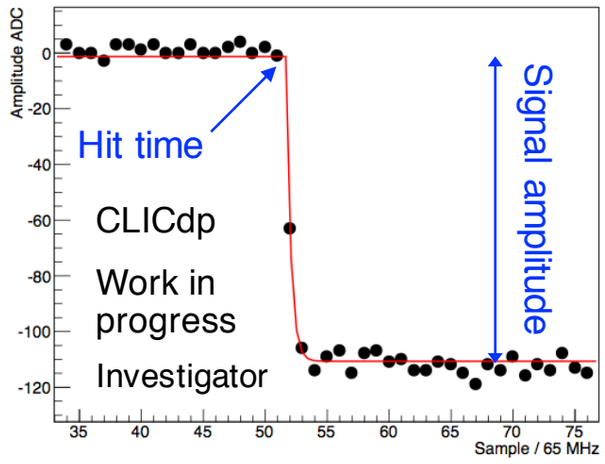
→ Minimise capacitance (~ 2 fF) → fast timing (~ ns)



Digitisation and readout not integrated in chip:

- External 65 MHz sampling ADC per pixel reads out full waveform *(designed by K. M. Sielewicz)*
- Threshold on signal/noise to define hit pixels
- Position reconstruction by Centre of Gravity, timing extracted from fit to full waveform of hit pixels



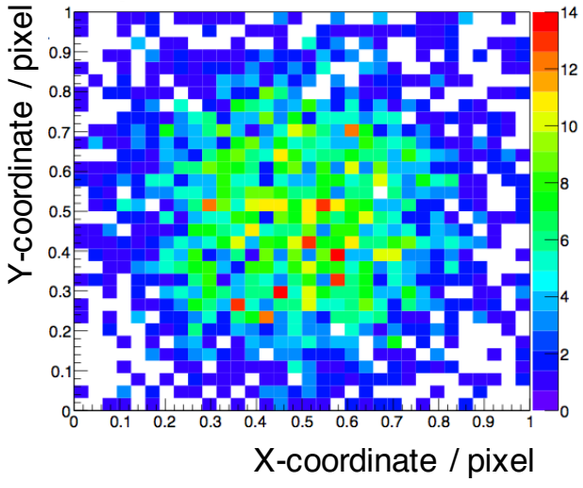


Test-beam results / ALICE investigator chip

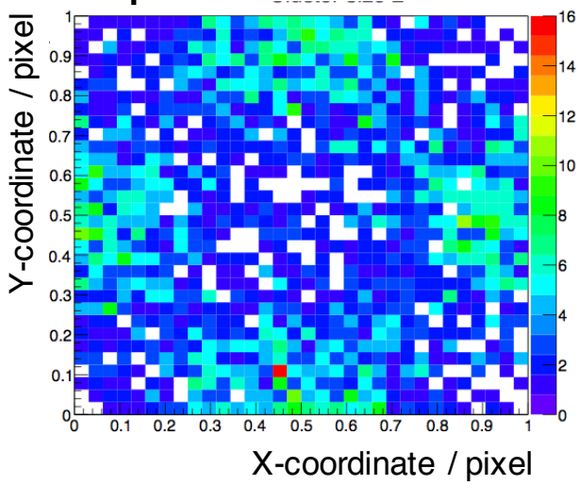
Number of counts for different cluster sizes within pixel cell for a pitch of 28 μm:

V_{Bias} = 6 V, signal/noise > 10

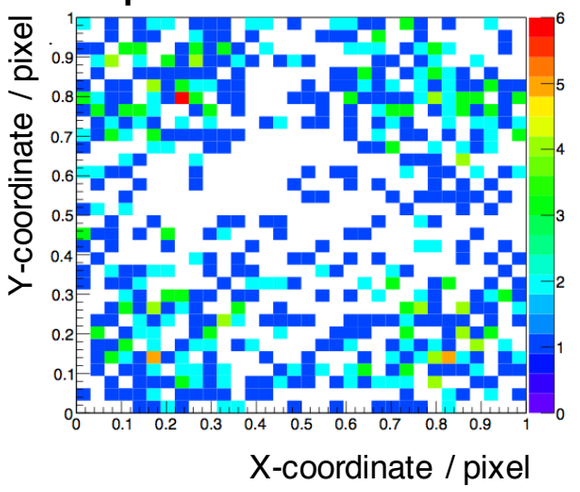
1 pixel hits:



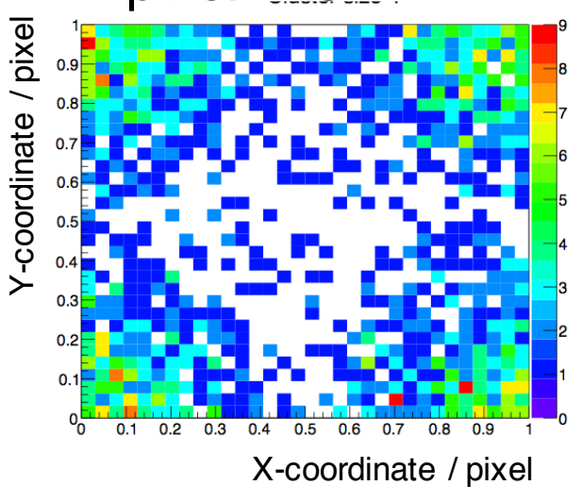
2 pixel hits:



3 pixel hits:



4 pixel hits:



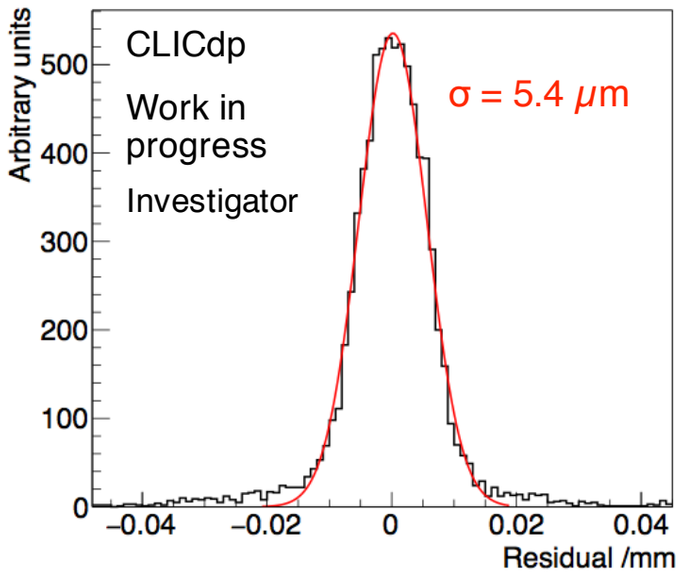
Spatial and timing resolution for a pitch of 28 μm:

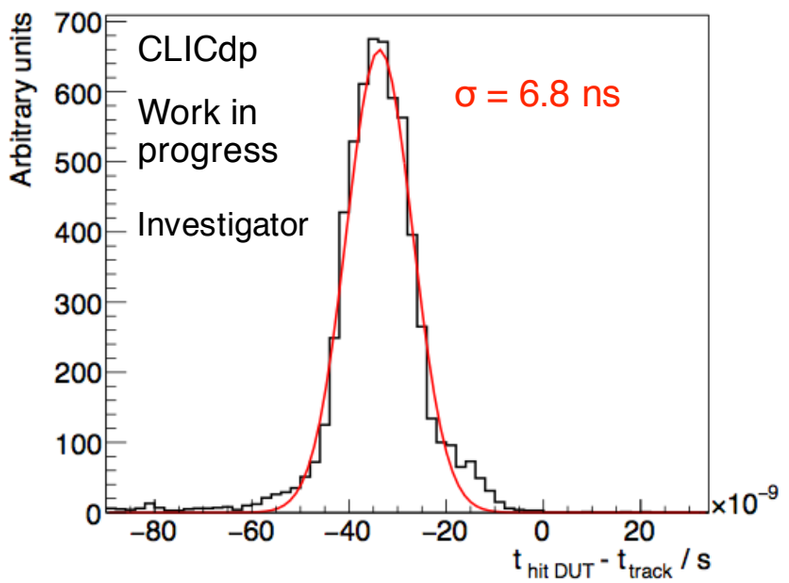
V_{Bias} = 6 V, signal/noise > 10

- Single point resolution of ~ 5 μm
- Timing resolution of ~ 7 ns

(Results comparable with single point resolution of ~ 5 μm achieved for ALICE ALPIDE chip with fully integrated readout and a pitch of 28 μm)

→ Promising results with respect to CLIC requirements





The AGH-Cracow SOI chip

Silicon On Insulator (SOI) technology:

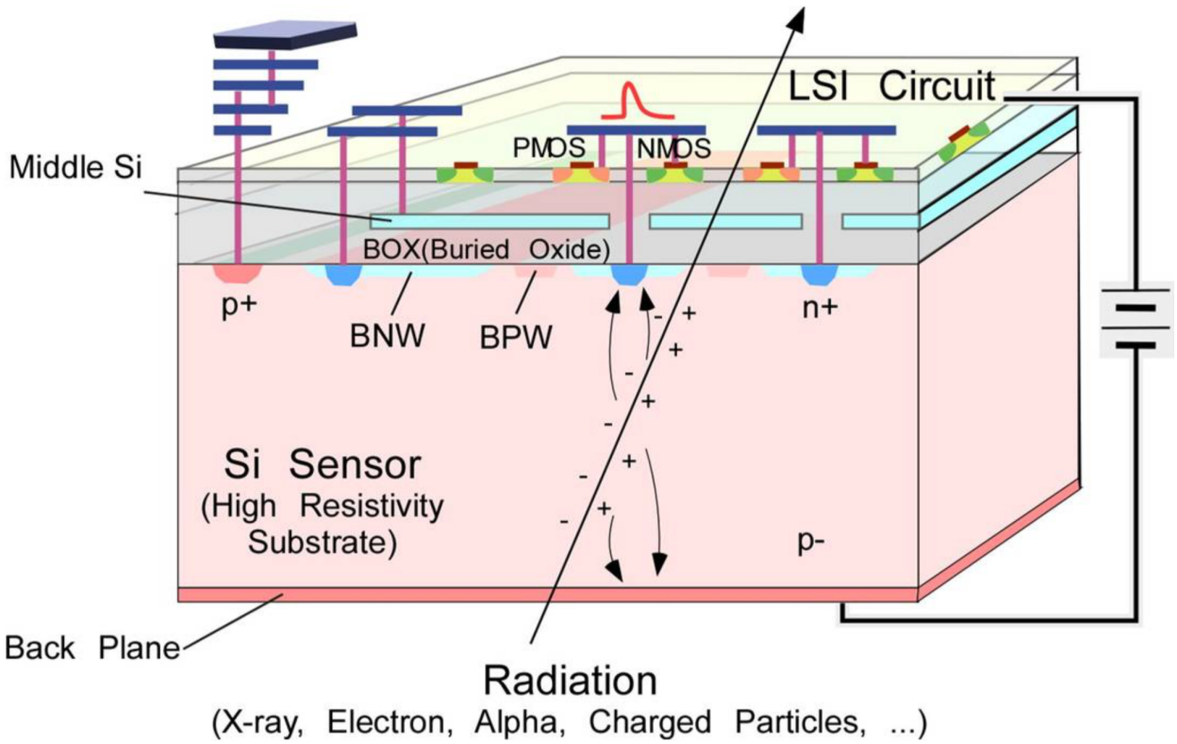
- Electronics (CMOS transistors) on low resistivity wafer

- High resistivity sensor separated by buried oxide (insulator)

→ Separation of electronics from bias voltage of sensor substrate

→ Full depletion of sensor substrate possible

→ Fast timing capability



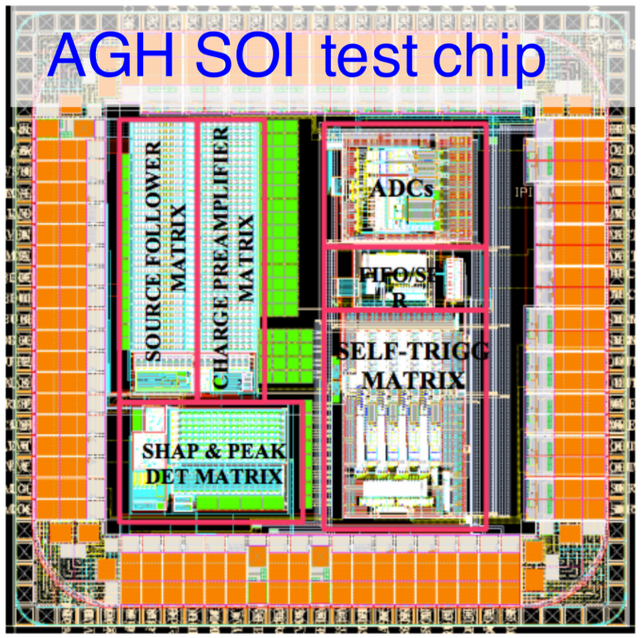
AGH-Cracow test-chip:

- 200 nm CMOS process
- Designed to target CLIC requirements

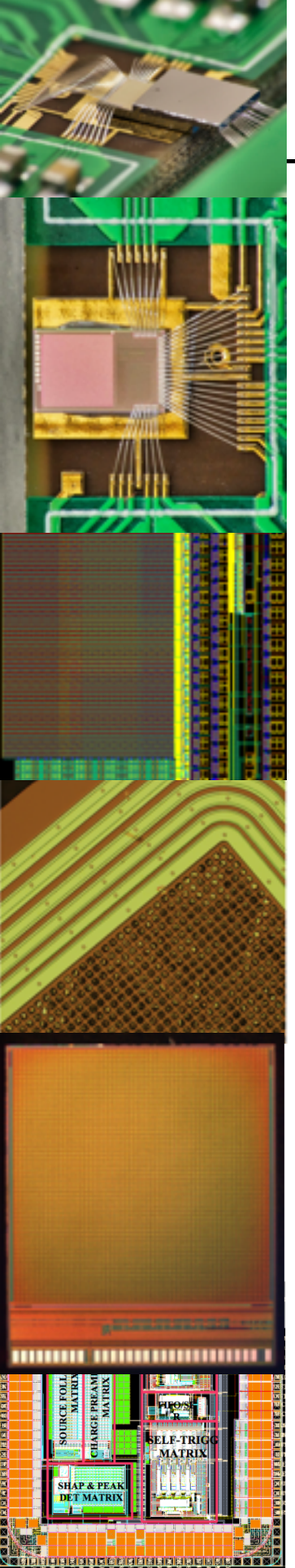
→ Small pitch ≥ 30 μm and fast timing

- Successfully integrated in the CLICdp Timepix3 telescope

→ Data taking and analysis currently ongoing



arXiv:1507.00864



Summary & outlook

Challenging requirements for the CLIC vertex and tracking detectors

Very active integrated R&D effort for the vertex and the tracker:

- Thin planar sensors with Timepix(3) readout:

→ Efficiency of > 99 % even for thin sensors of 50 µm

- Active edge sensors with Timepix3 readout:

→ Study of different guard ring layouts to obtain efficiency up to the edge

- CLICpix (64x64 pixel matrix with 25 µm pitch) planar sensor assemblies:

→ Developed single-chip bump-bonding process for 25 um pitch

→ Performance in agreement with expectations

- HV-CMOS active sensors and capacitive coupling:

→ Proof of principle by coupling of CCPD to CLICpix ASIC achieved

- ALICE investigator chip:

→ Promising results of spatial and timing resolution with respect to the CLIC

- AHG-Cracow SOI chip:

→ Designed to target CLIC requirements, data taking and analysis currently ongoing

Thanks to everybody who provided material for this talk!