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GotthardII development status

XDAC Meeting, 23.05.2016

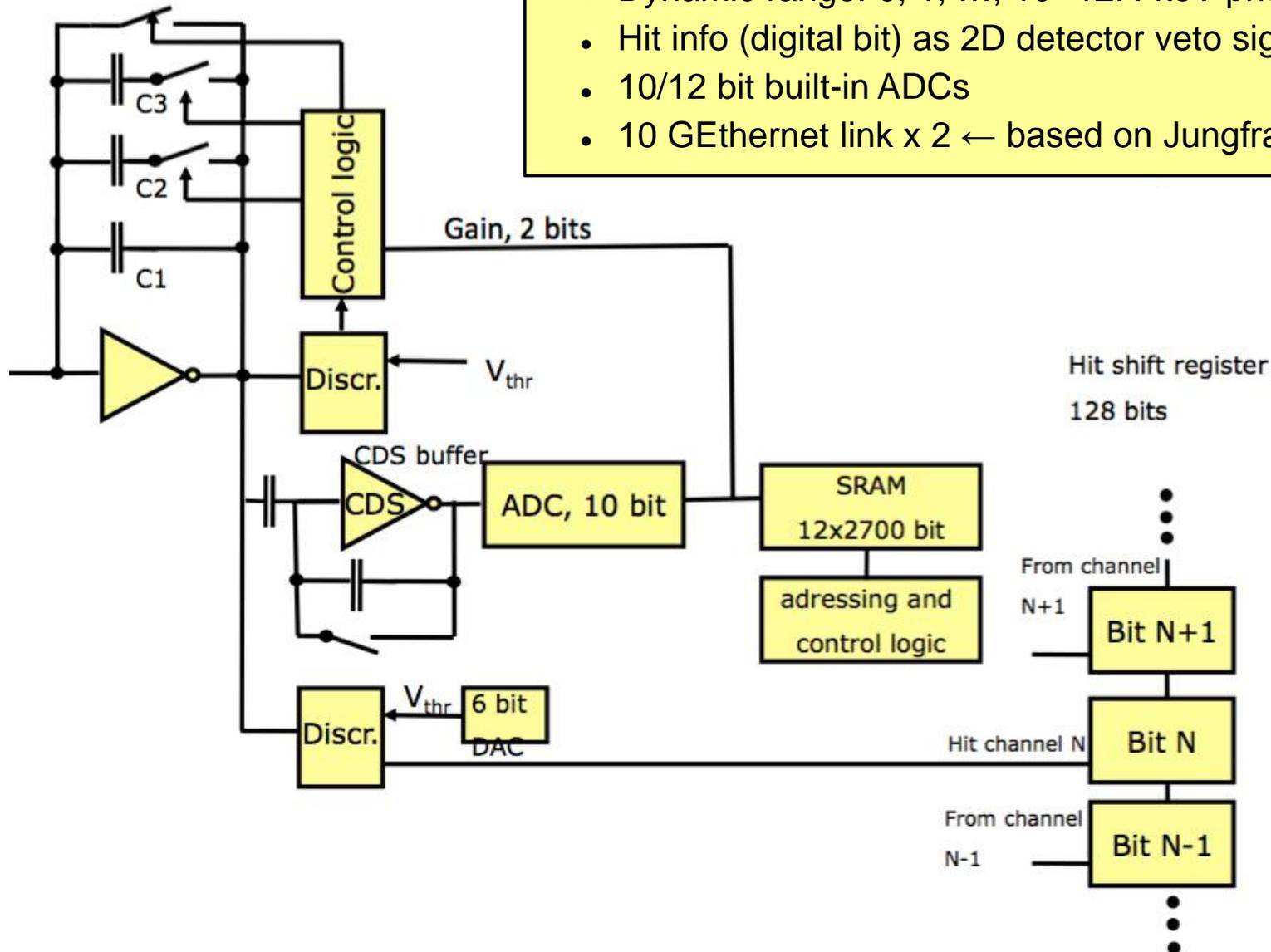


Outline

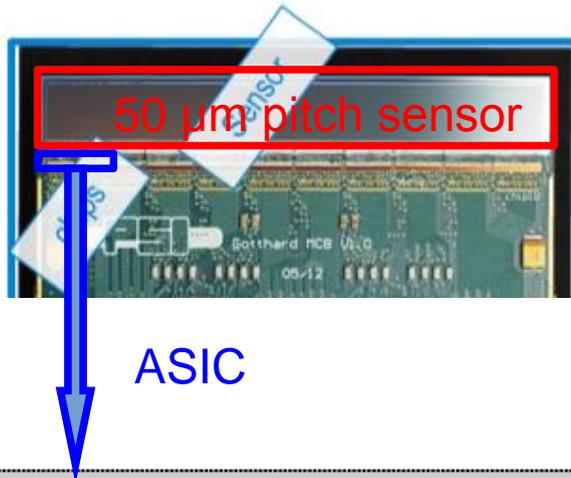
- The Gotthard-II
- Gotthard-1.5(&1.4) front-end characterization
 - Architecture
 - Test results
- Towards Gotthard-II and next submission:
 - New front-end
 - ADC status
- Summary

Reminder of Gotthard-II: Schematic

- 4.5 MHz frame rate ← bunch structure of the Eu-XFEL
- Dynamic range: 0, 1, ..., 10^4 12.4 keV photons
- Hit info (digital bit) as 2D detector veto signal
- 10/12 bit built-in ADCs
- 10 GEthernet link x 2 ← based on Jungfrau read-out

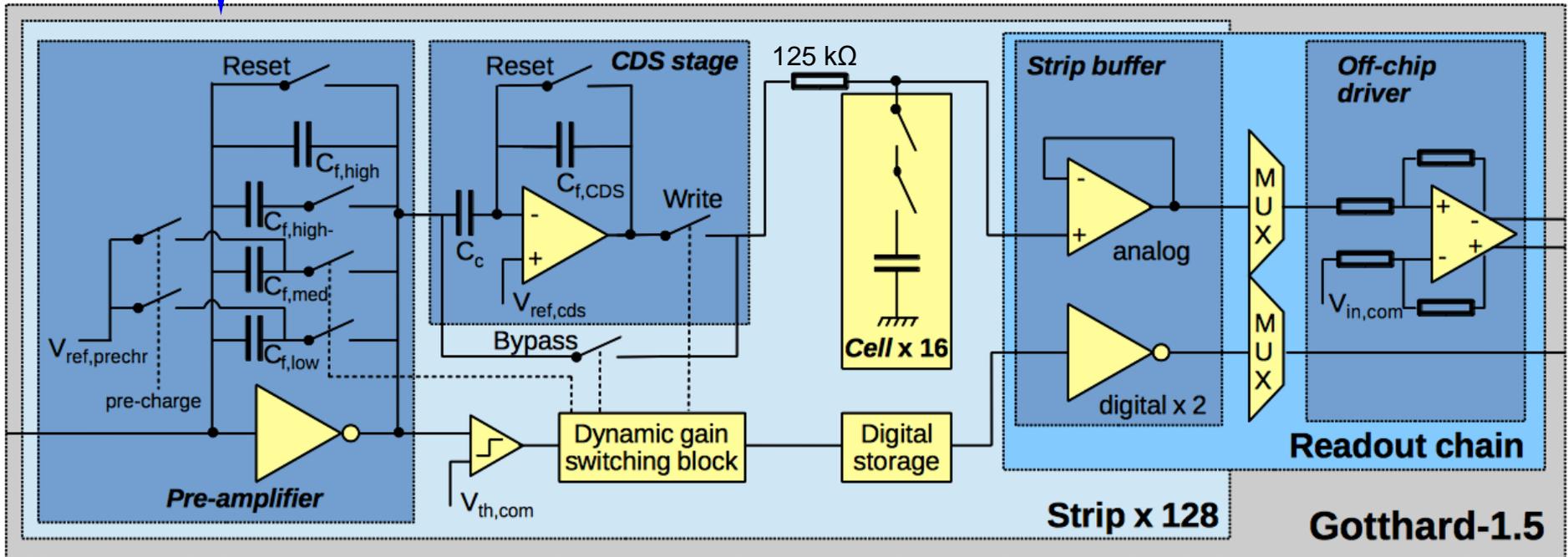


Gotthard-1.4&1.5 Architecture



Key features:

- Dynamic gain switching (Jungfrau & AGIPD)
- Different high gain capacitor: HG0 and G0
- Med. & low gain capacitors pre-chargeable
- CDS bypass after gain switching
- Digital gain bit

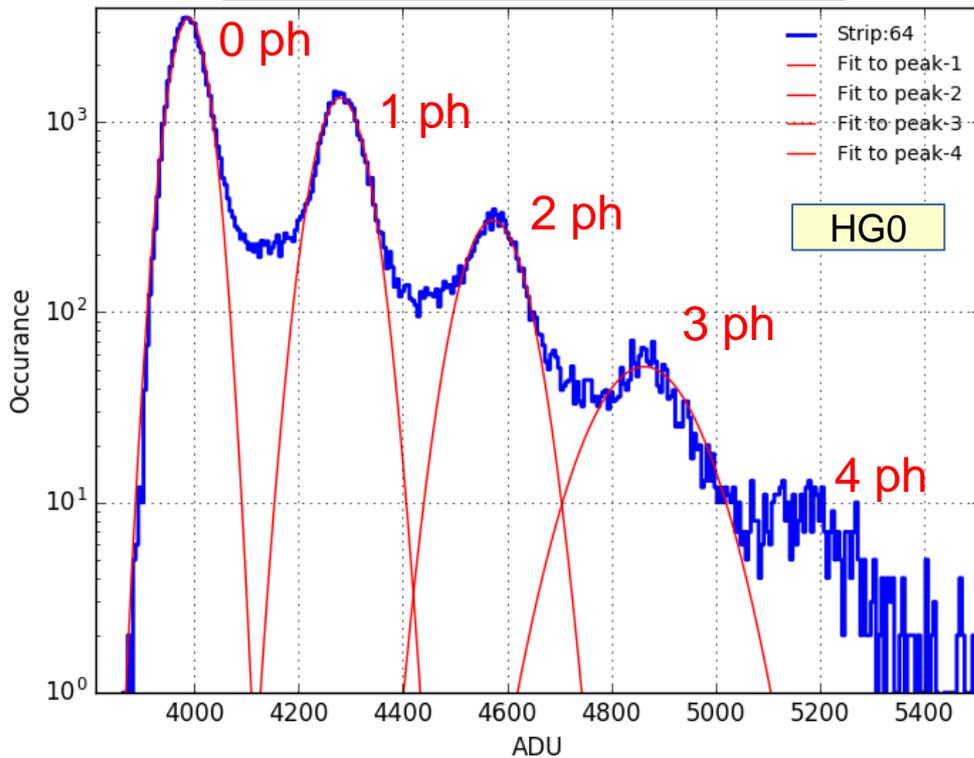


Less channels but similar complexity to the other integrating detector!

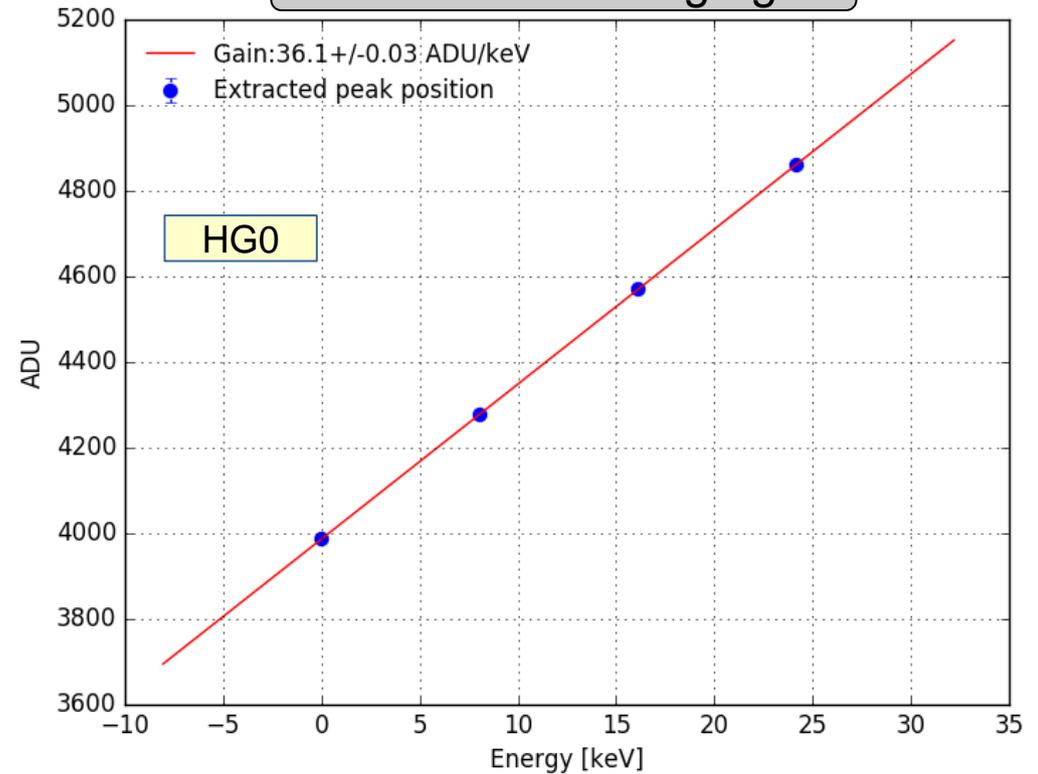
High gain: X-ray fluorescence

- Cu-target for fluorescence: $E_{ph} \rightarrow 8.05 \text{ keV}$
 \rightarrow Conversion gain [ADU/keV]

Histogram: 100,000 frames



Gain extraction: High gain

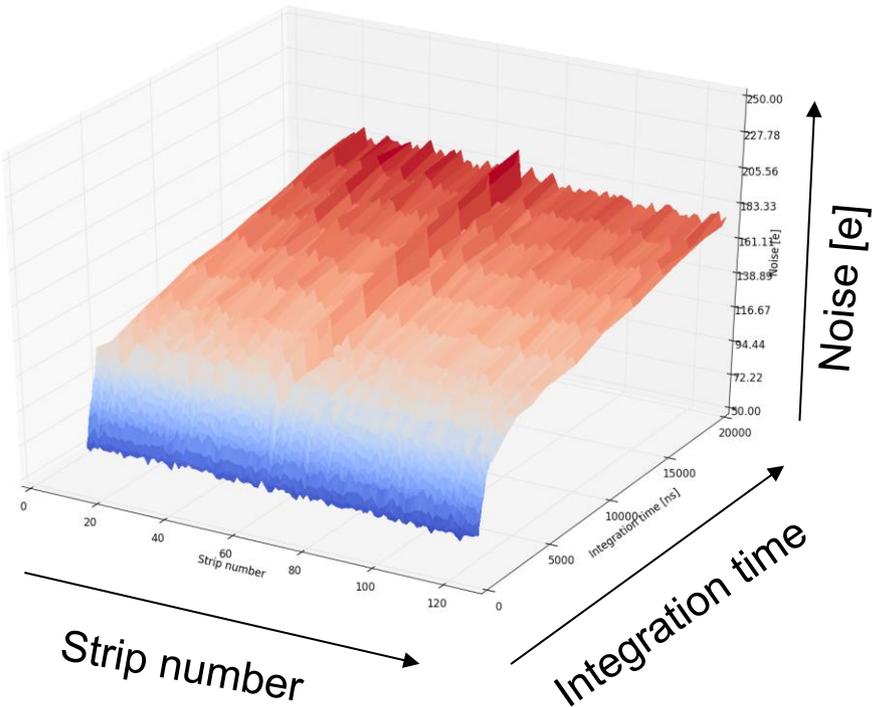


More coincident photons due to large detection area per channel!

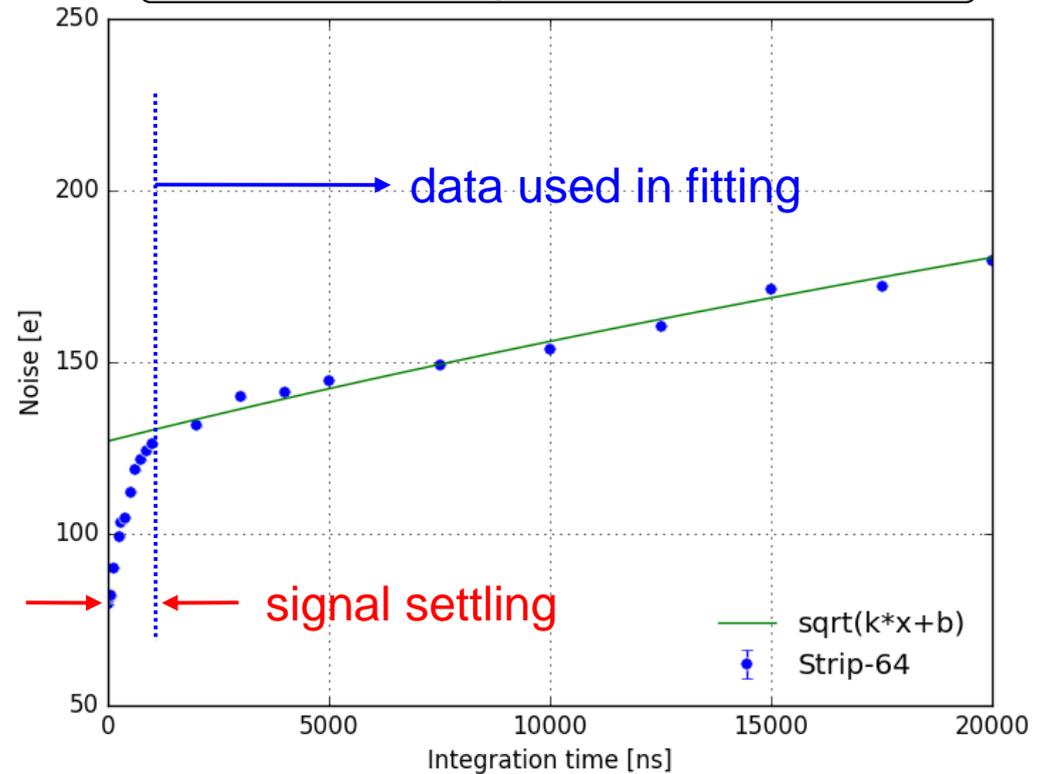
Noise vs. integration time

- Noise as function of integration time for HG0 with $C_f=13.4$ fF:
 - Integration time from 50 ns up to 20 μ s
 - Fitting model: $Noise[ENC] = \sqrt{k \cdot t_{int} + b^2}$ with b intrinsic para. indep. t_{int}

Example for all strips



Noise vs. integration time for HG0

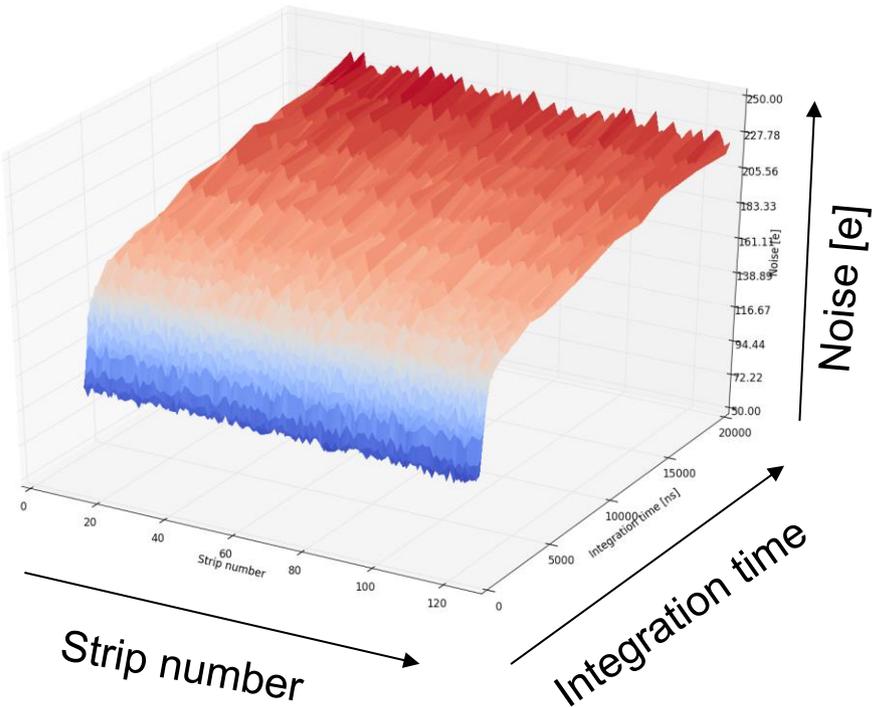


Noise HG0: ~ 125 e @ $t_{int} = 100-150$ ns (XFEL timing)

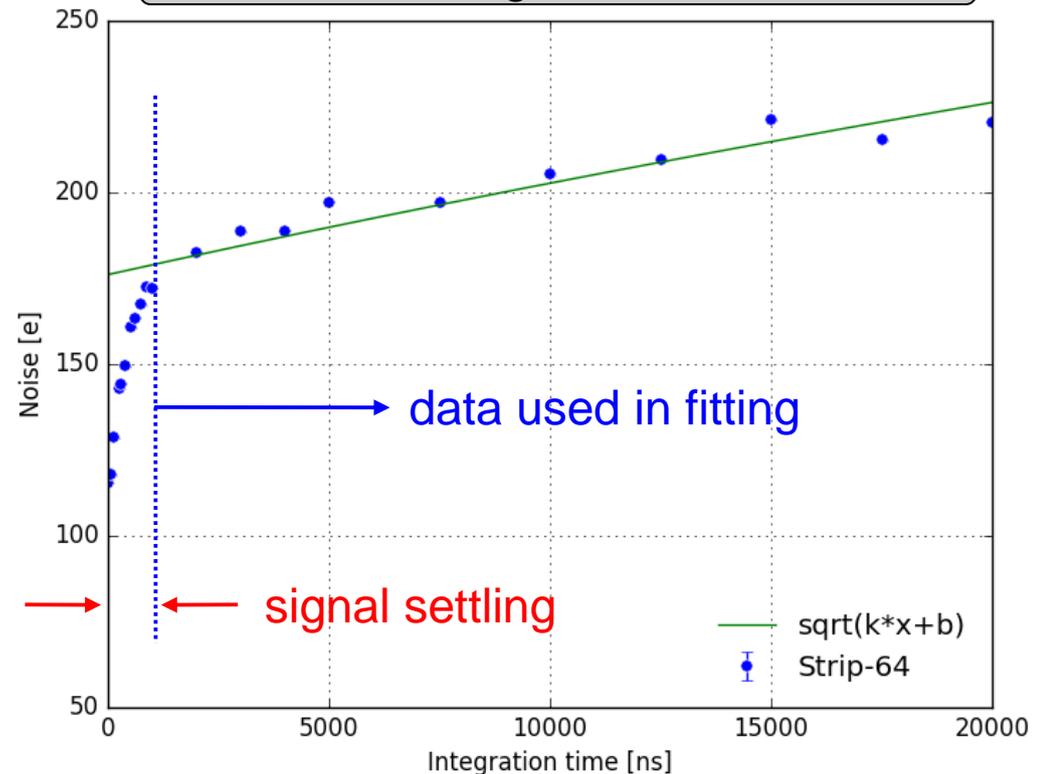
Noise vs. integration time

- Noise as function of integration time for G0 with $C_f=46.4$ fF:
 - Integration time from 50 ns up to 20 μ s
 - Fitting model: $Noise[ENC] = \sqrt{k \cdot t_{int} + b^2}$ with b intrinsic para. indep. t_{int}

Example for all strips



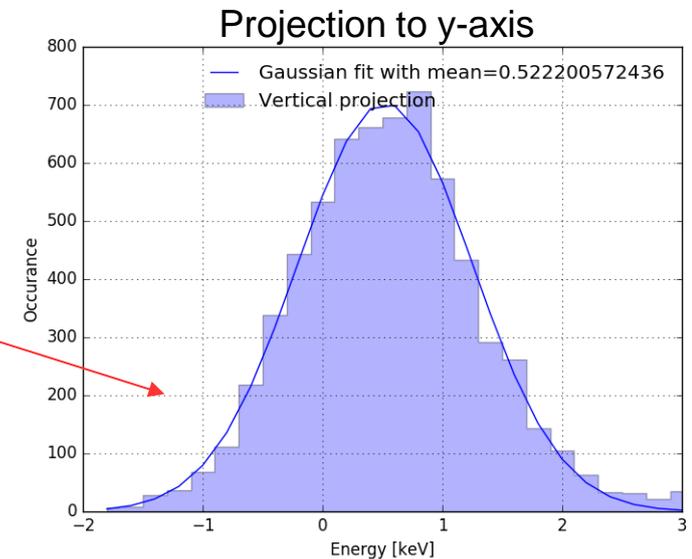
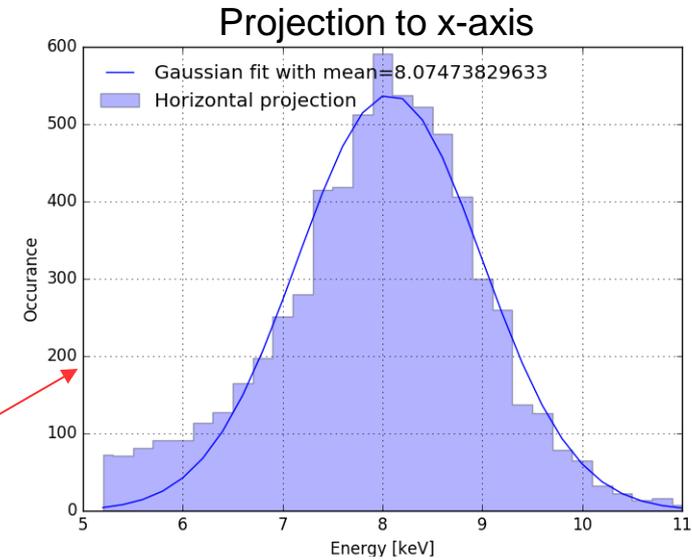
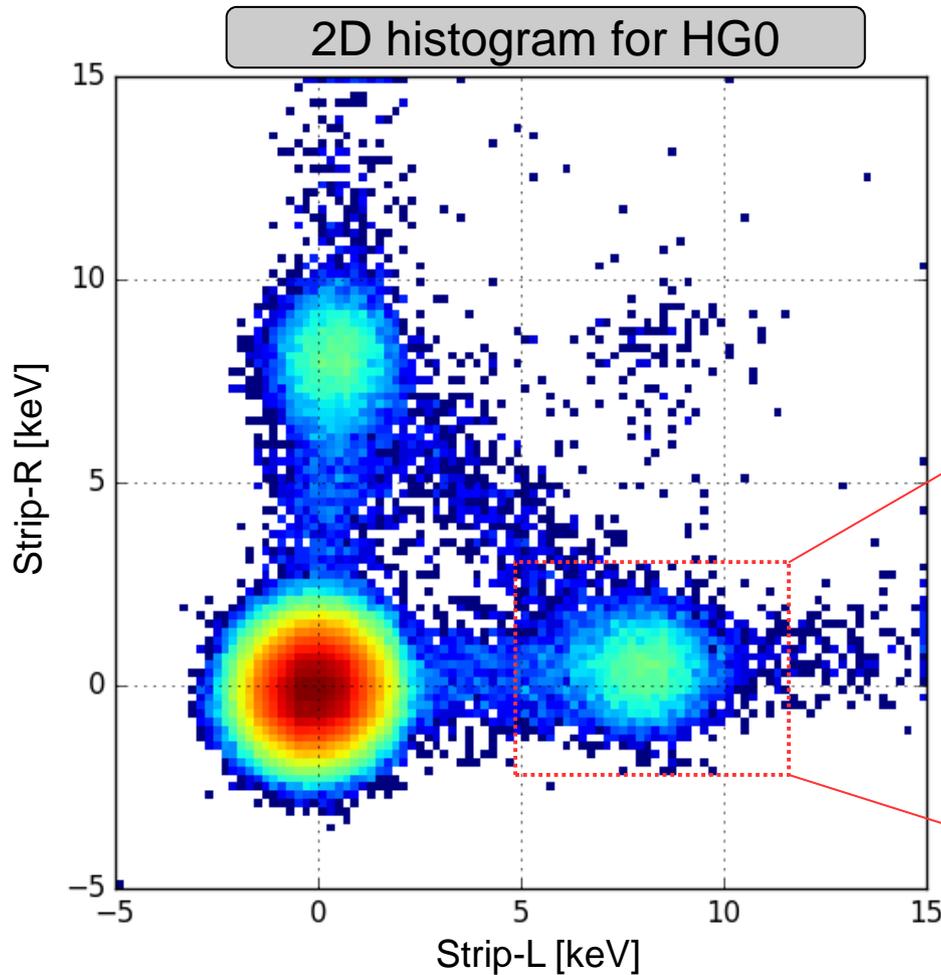
Noise vs. integration time for G0



Noise G0: ~ 175 e @ $t_{int} = 100-150$ ns (XFEL timing)

Coupling: Low rate X-ray measurement

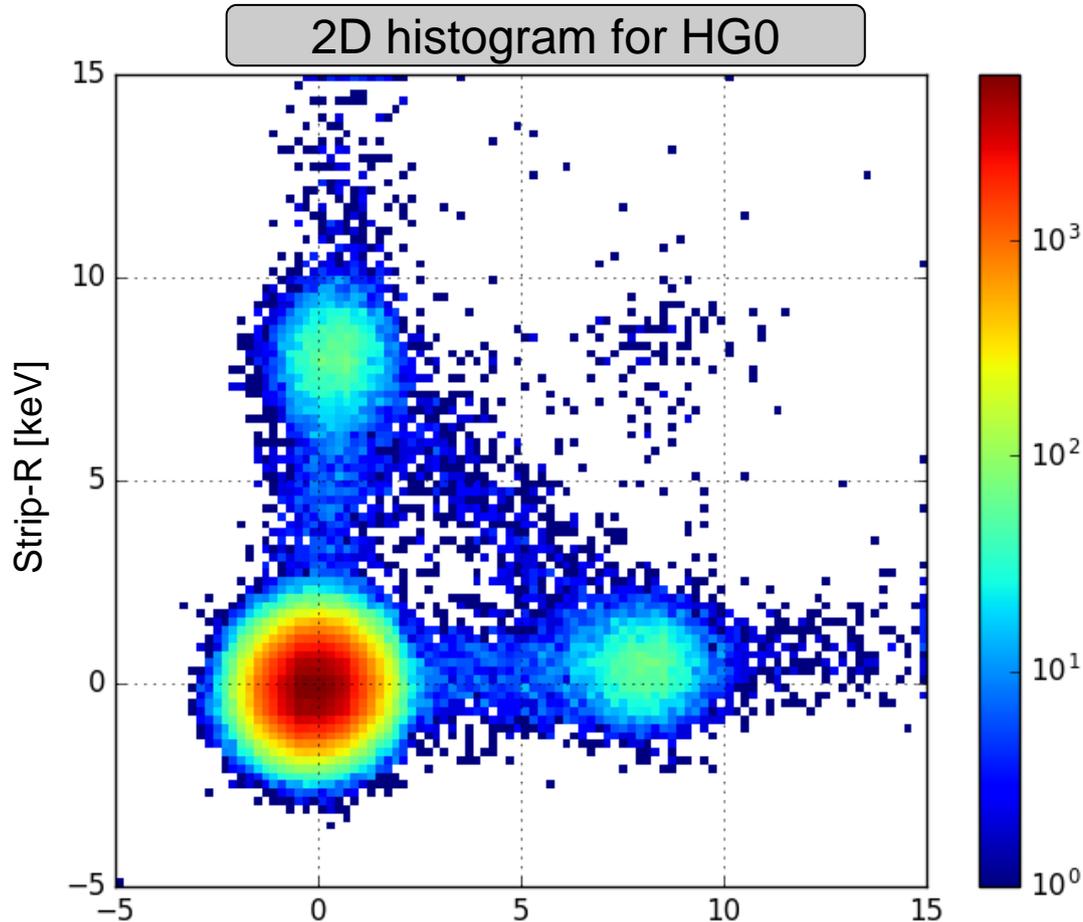
- Low rate X-ray measurement: 0 or 1 ph entry



- Coupling: 6.5% for HG0; 3.9% for G0

Coupling: Low rate X-ray measurement

- Low rate X-ray measurement: 0 or 1 ph entry



Simple calculation/approximation:

$$Coupling = \frac{1}{A} \cdot \frac{C_{int}}{C_f + C_{para}}$$

↑ interstrip cap. (239 fF)
 ↓ DC gain (125) ↓ parasitic cap. (15 fF)

HG0: 6.8 %; G0: 3.1%

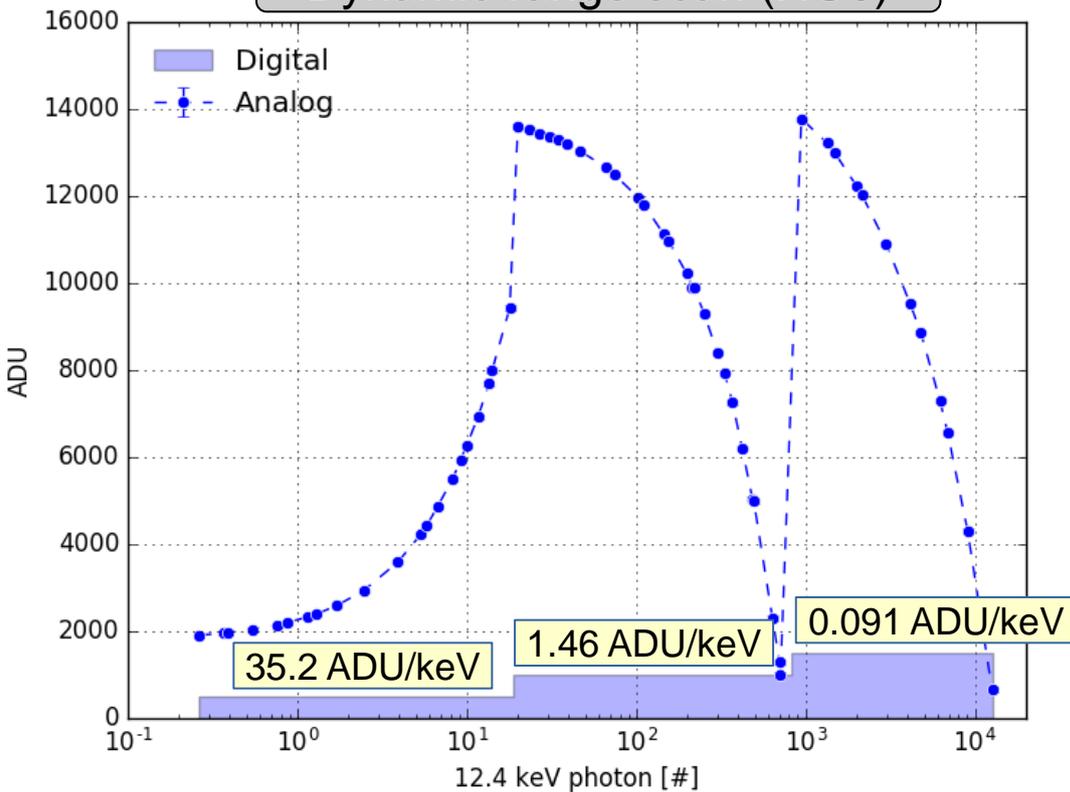
Good agreement with measurement!

- Coupling: 6.5% for HG0; 3.9% for G0

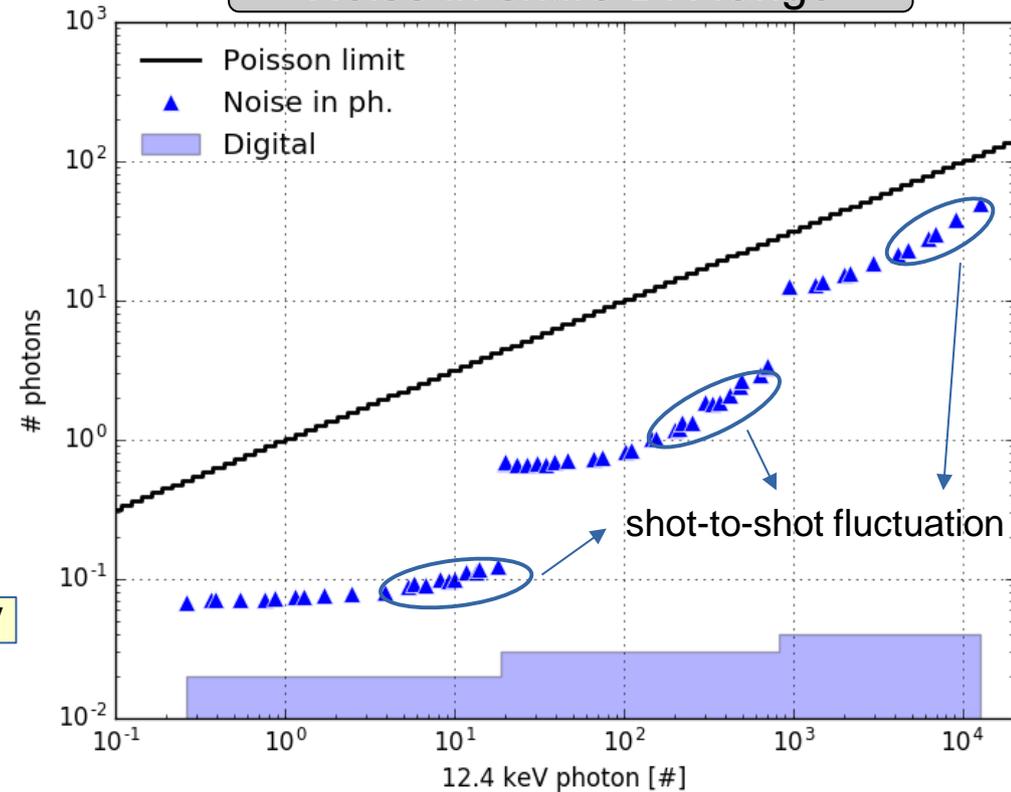
Dynamic range: Infrared laser

- Photon conversion based on high gain measured with X-rays
- Dynamic range up to 1.35×10^4 12.4 keV
- Noise below poisson limit: $S/N > 14$ for single photon detection

Dynamic range scan (HG0)



Noise in entire DR range

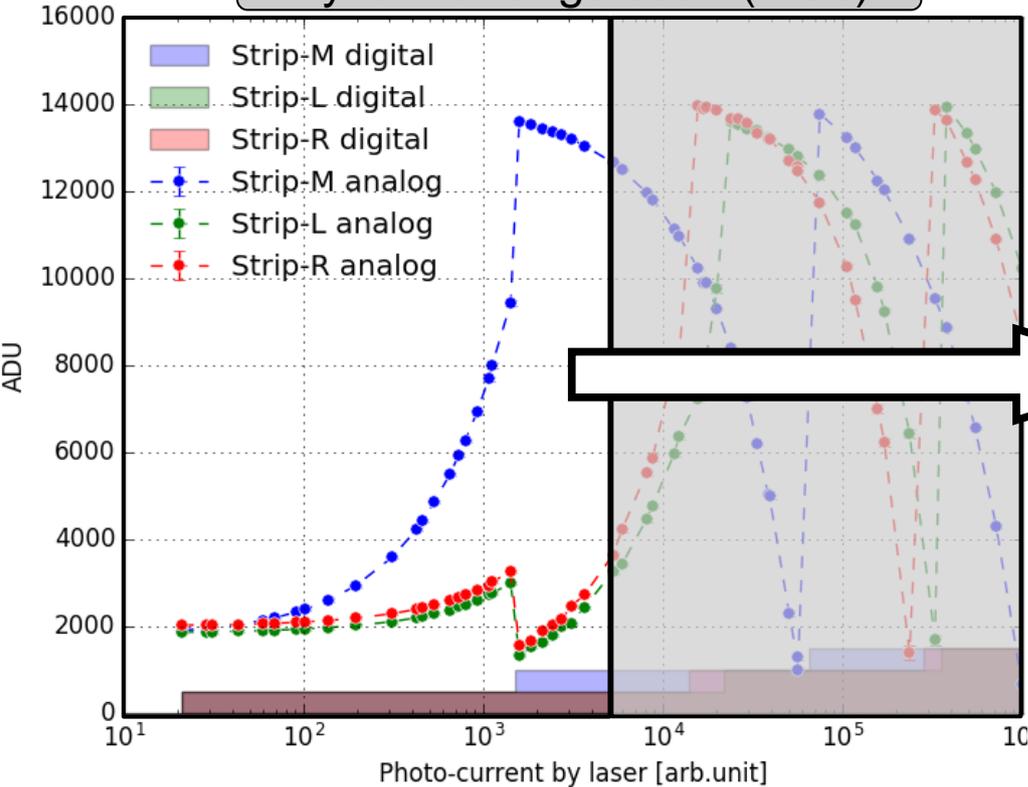


Resolution of 1 ph (H), 3 ph (M) and 55 ph (L) for 5σ separation

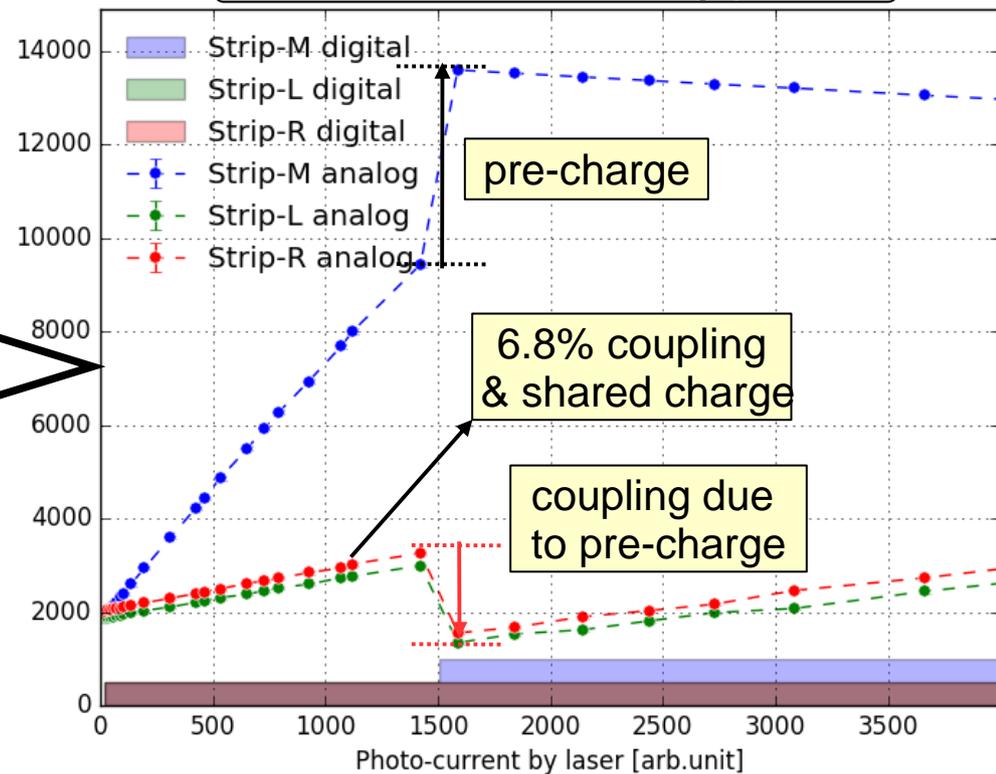
Coupling due to pre-charge: Measurement

- Laser injection into a single channel
- Charge in neighbouring strip in high gain: 6.8% coupling + shared charge
- Charge loss in neighbouring strips when injected channel switched

Dynamic range scan (HG0)



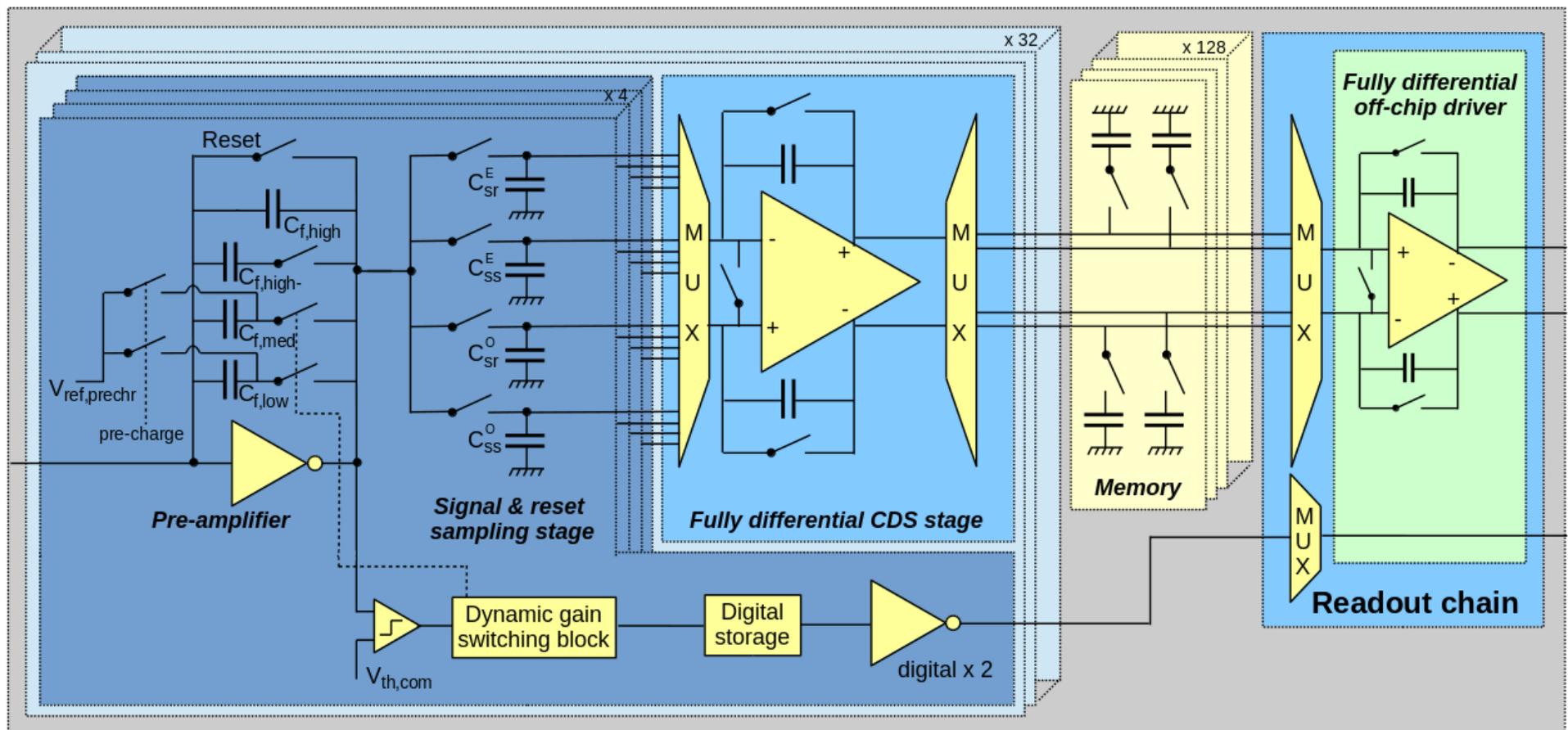
Zoom-in at switching point



Schematic of new front-end

- Features of new front-end:

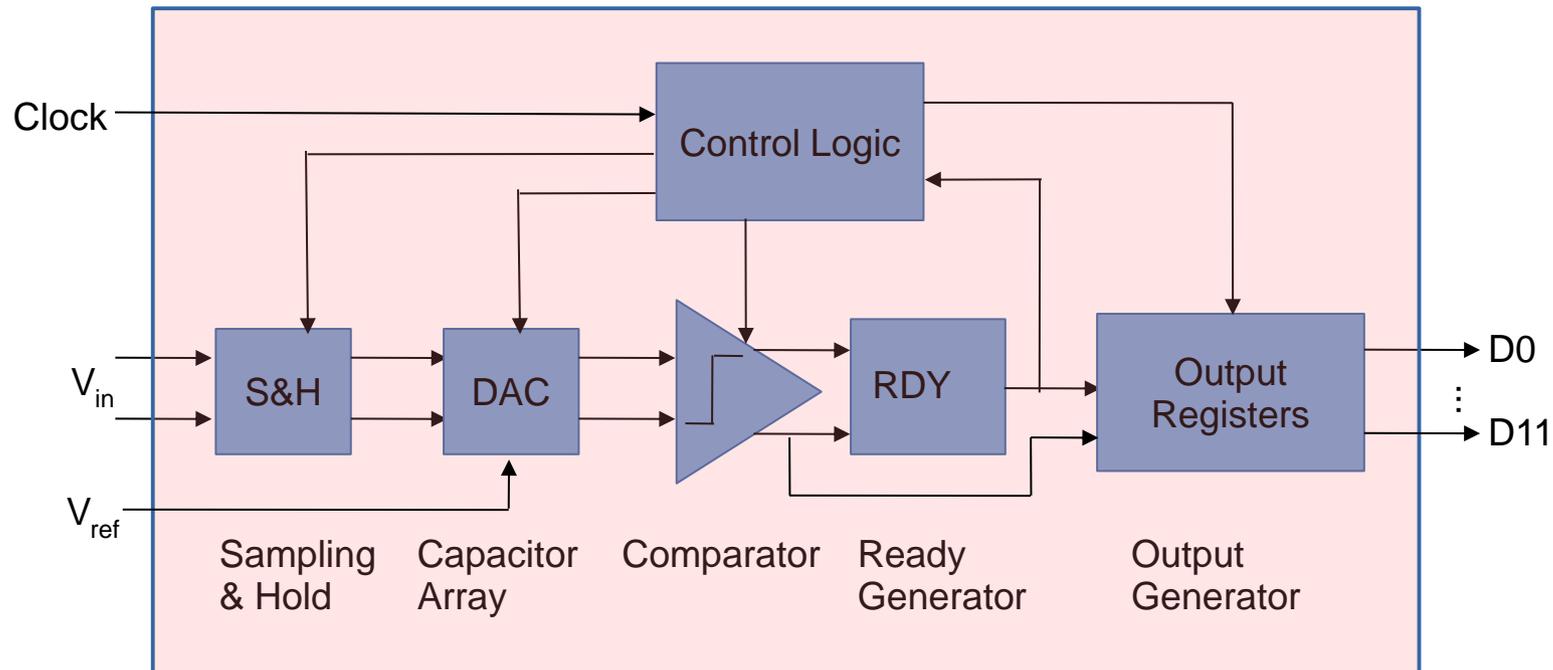
- high DC gain pre-amplifier
- fully differential output
- continuous CDS sampling
- available for plugging build-in ADCs



4.5 MHz 18 MHz up to 80 MHz

ADC design progress

12 Bit Asynchronous SAR ADC with Charge Redistribution DAC

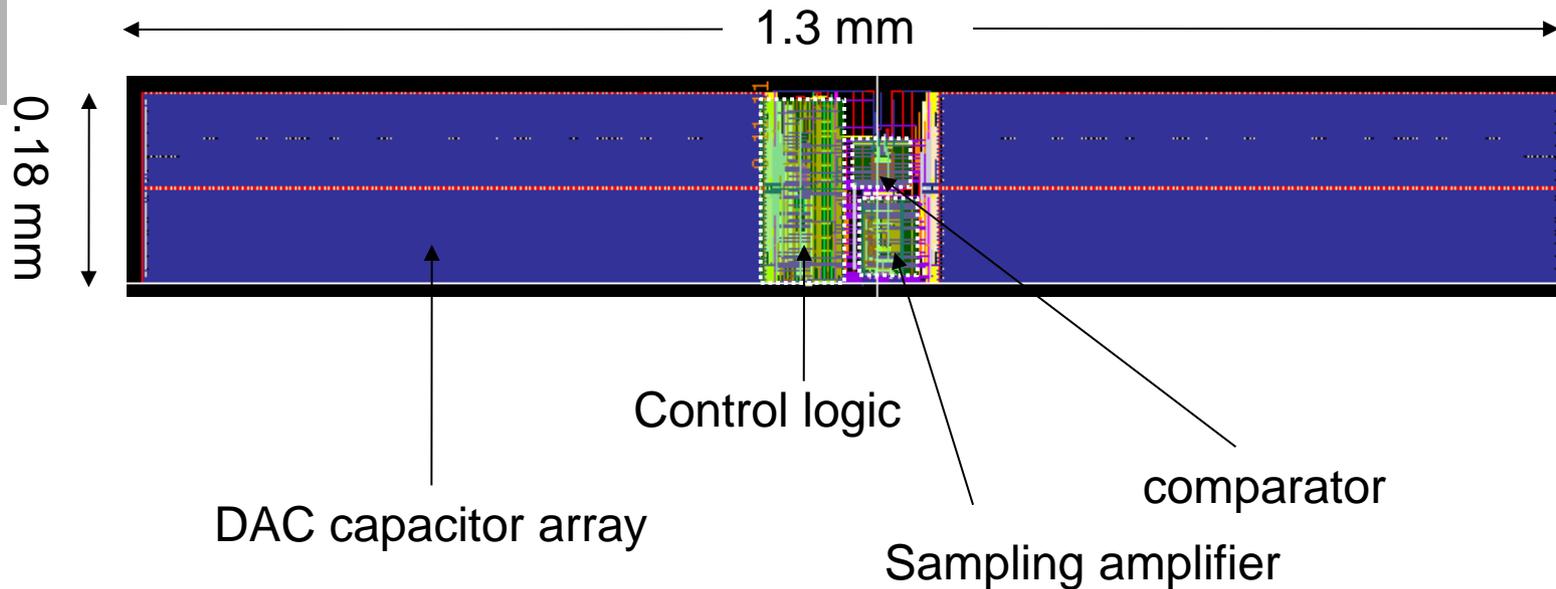


Specification:

- Resolution 12 bit
- Sampling frequency 20 MHz
- Power supply voltage 1.2V
- Input Signal Range $\pm 0.8 \text{ V} \rightarrow 1 \text{ LSB} = 390 \mu\text{V}$

ADC design progress

12 Bit Asynchronous SAR ADC with Charge Redistribution DAC

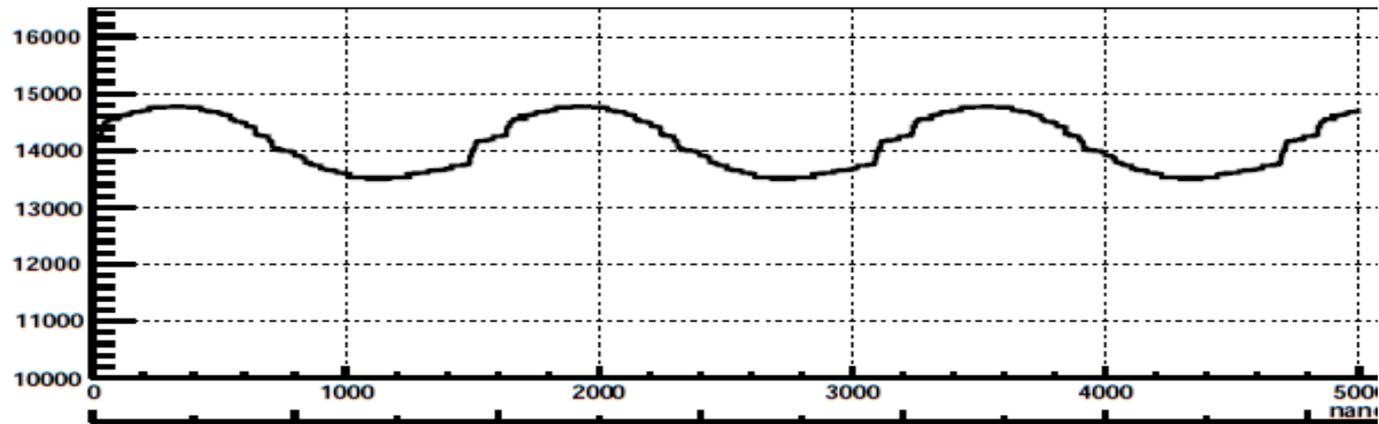


Specification:

- Resolution 12 bit
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ADC progress: Measurement result

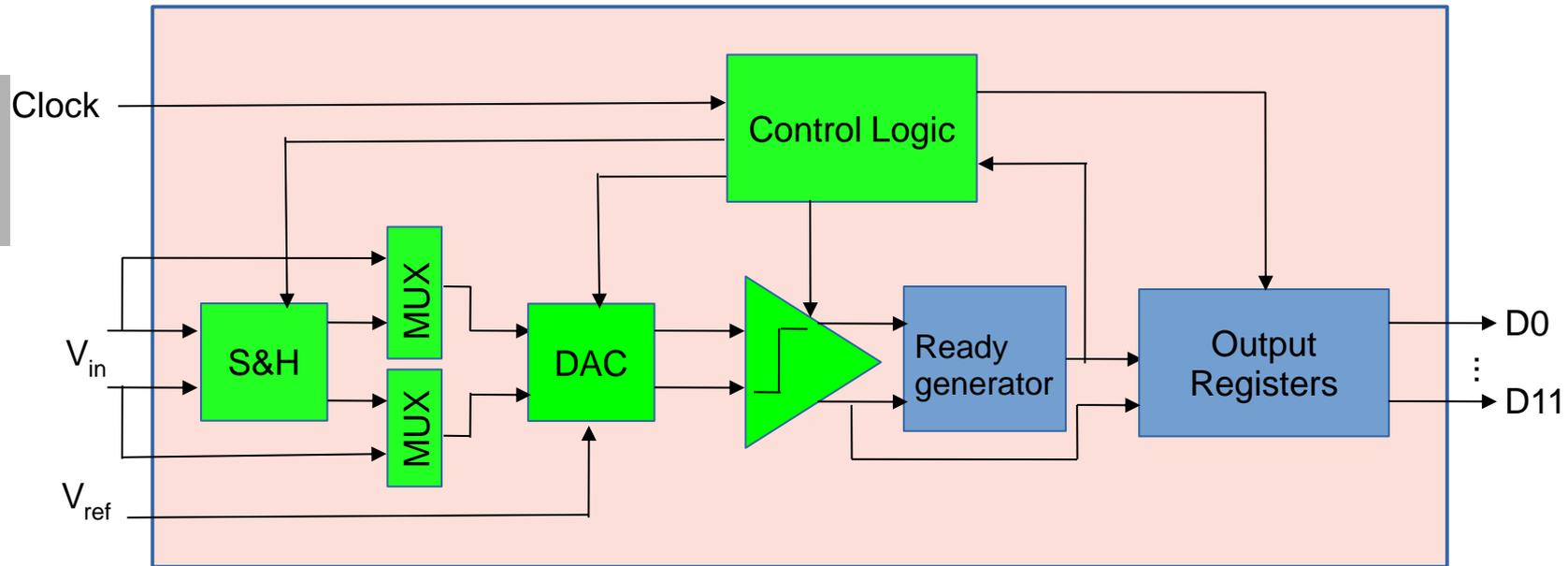
Measurements show that the ADC is working basically



However

- The sampling Frequency < 8 MHz . The comparator is slower due to the parasitic RC of layout
- Had problems reproducing this with simulations using extracted parasitics, works now problem: comparator speed
- The last 4 LSBs are not stable, sometimes bits are missing: problem with comparator ready signal

ADC progress: The redesign



Redesign of the ADC

- The comparator will be faster to achieve 20 MHz sampling frequency
- Insert adjustable delay in the control logic for debugging.
- The input can be fed into the comparator directly if the noise from the S&H is really a problem
- The redesign will be taped out in July 2016



Summary

- Gotthard-1.5(&1.4) characterized
 - Noise: 125 e for HG0, 175 e for G0
 - Dynamic range up to 1.35×10^4 12.4 keV ph
 - Settling time: 500 ns – 600 ns limited by a resistor
 - Coupling in high gain: 6.8% for HG0, 3.9% for G0
 - Charge loss in neighbouring channel due to switching/precharge: 2.4×12.4 keV ph
- Next submission in July
 - New analogue front end with High DC gain pre-amplifier
 - ADC complete redesign with faster comparator and variable delay after comparator ready signal
- Next steps
 - MPW with memory end of this year/early next year
 - Engineering run mid 17