Status of test kit and ABCN' work

29 March 2016

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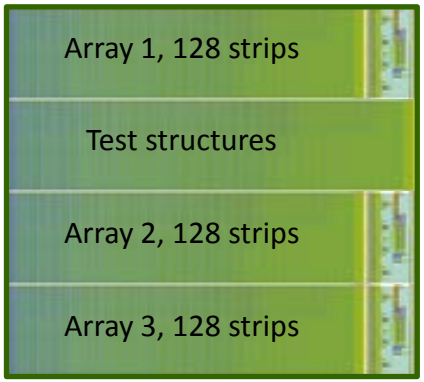
with help from many colleagues

Proposal for testing CHESS-2 test structures

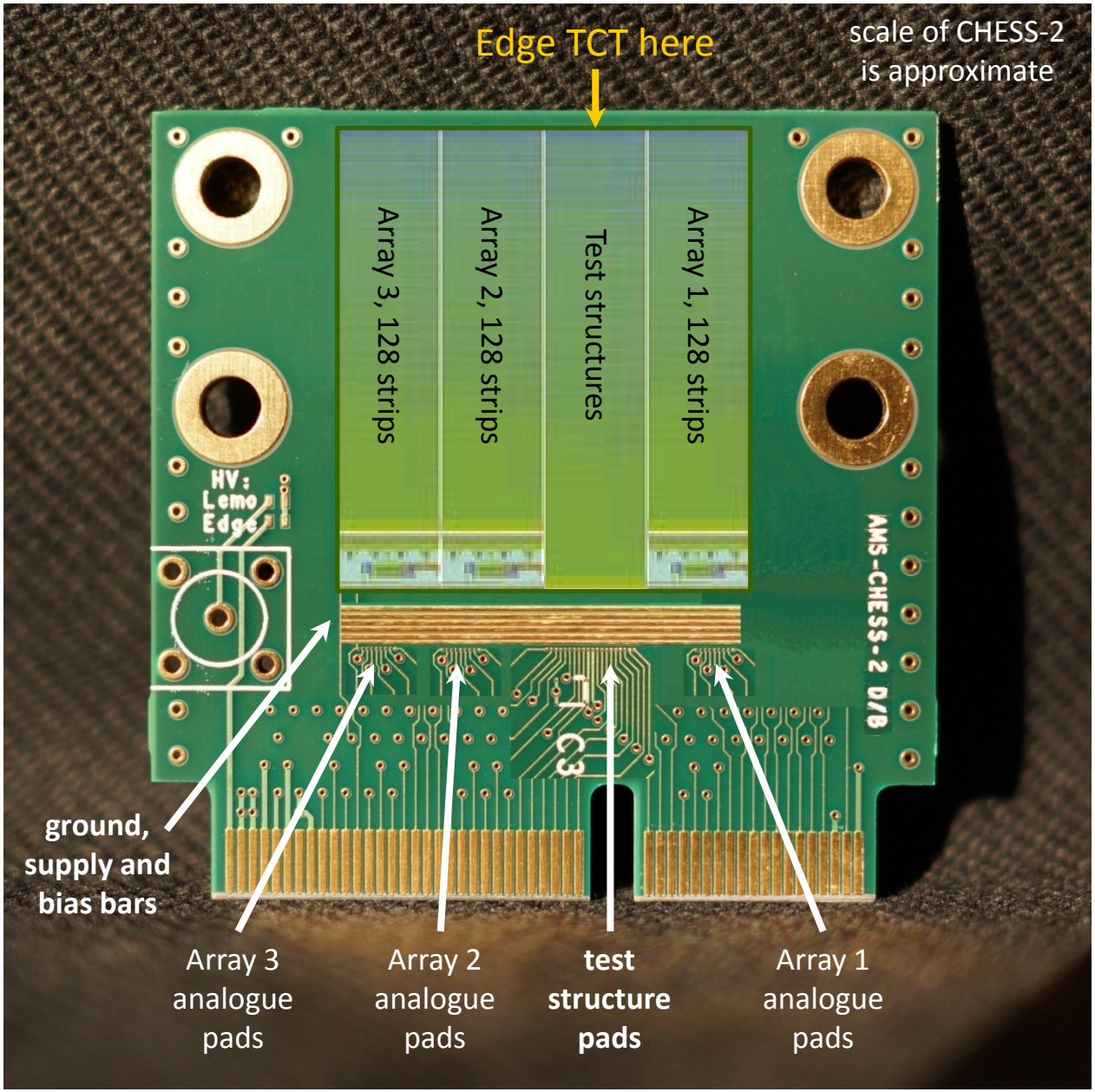


- CHESS-2 will have analogue structures similar to the kinds that CHESS-1 will have.
  - Amplifiers, pixel arrays (near edge??)

- We already have a motherboard able to test a variety of these kinds of devices: AMS CHESS1, TJ CHESS1
- In these cases we just needed to re-make a daughter card.

- **Does it make sense to develop an analogue daughter card specifically for the analogue parts of CHESS2?**

CHESS-2 analogue daughterboard sketch



Proposal for testing CHESS-2 test structures

- **Benefits**
  - Many groups have Atlys+motherboards and have used them successfully.
    - Other groups can obtain motherboards as well
  - Separates out testing of the digital and system aspects of the strip-like sections
    - Also debugging SACHI interfaces and the full S-curve and threshold-setting software
- Downside
  - Would potentially end up with chips that could not then be subsequently tested in Arrays 1, 2, and 3.

Questions about CHESS-2 test structures

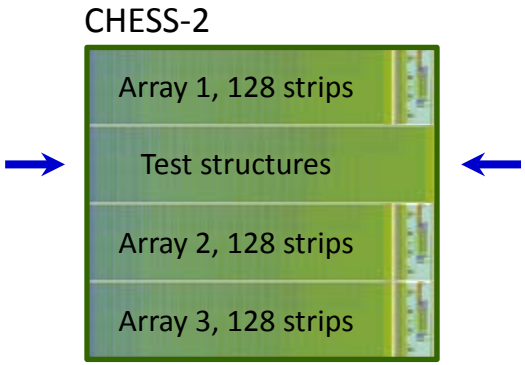
It would be great if the following could be included in slides at the CHESS-2 design review.

This is the info needed to see if an analogue-only CHESS-2 daughterboard could be run with the CHESS-1 motherboard.

1. List of the pads for the test structures – pad names and a short notation of in/out/type e.g. pixel output / power supply "3.3V analogue supply" / bias voltage.
2. Do the test structures require any SACI control? We believe not?
3. Do the test structures receive any bias from other parts of the chip? For example, from an on-chip bias DAC block within Array 1 or Array 2?
4. Will the main strip arrays still have some analogue outputs as discussed last year? If yes, how many pads per array?

5. Are there any bond pads related to test structures (including bias/ground/supplies) along this edge, or close to it? (hoping not)

6. Are all of the test structures for Edge TCT along this edge? (hoping yes)



7. Are all the bond pads for test structures along this edge, or close to it? (hoping yes)

8. Are there any test structures for Edge TCT along this edge? (hoping not)

ABCN' – summary of last 2 meetings

Meetings

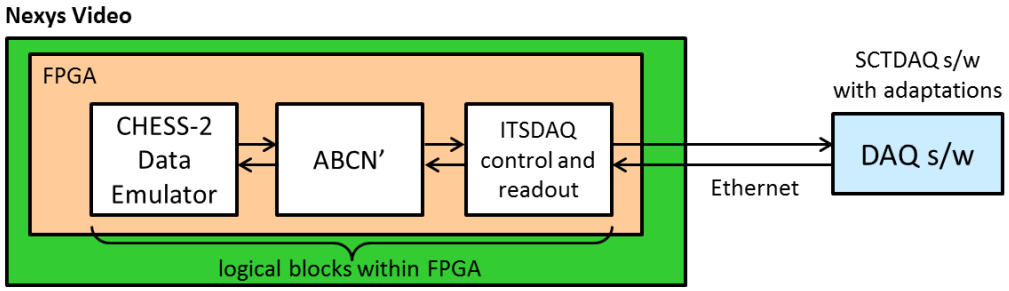
- Regular meetings are Thursdays 15:30 Geneva time
- Next meeting will be Thursday 7 April (no meeting on 31 March)
- Most recent minutes (done as annotated slides): 1, 2, 3

Summary of discussions and decisions

- The high-level development tasks have been outlined. Initial tasks have been assigned and are progressing (see minutes 3)
- The serial interface to the ABCN' will be the same as the ABC130 (not Star), using the L0/CMD and L1/R3 lines.
    - It's already known and stable
    - Most DAQ infrastructure for this already exists in ITSDAQ firmware and SCTDAQ software. Adapting is still needed for the CHESS-2 data format.
    - We already have a source code block example for controlling the CHESS-2 data emulator, controlled by the L0/CMD line (the "TMU", some adapting needed)

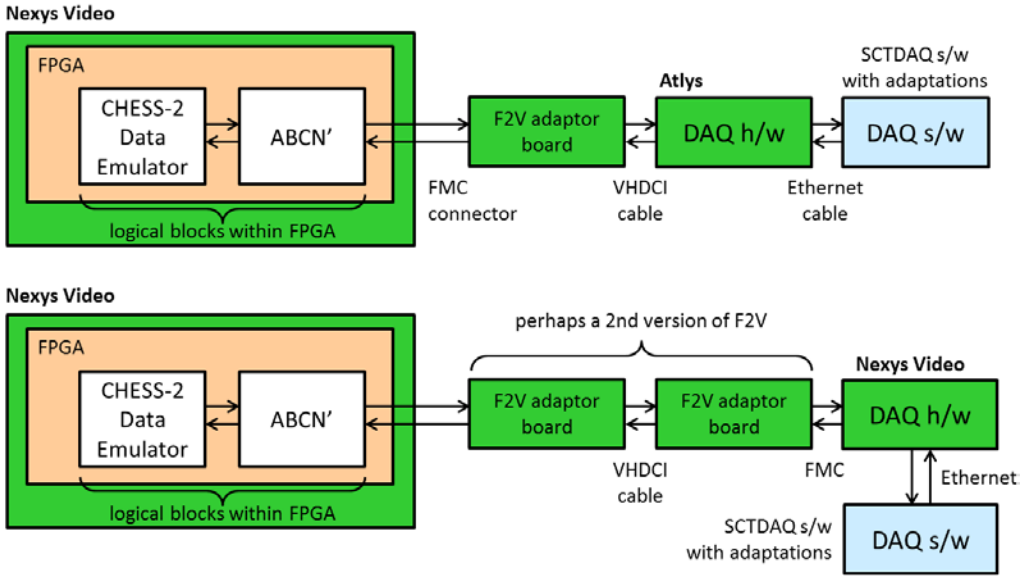
ABCN' – updated hardware summary, 1/2

Phase 1



All in one FPGA

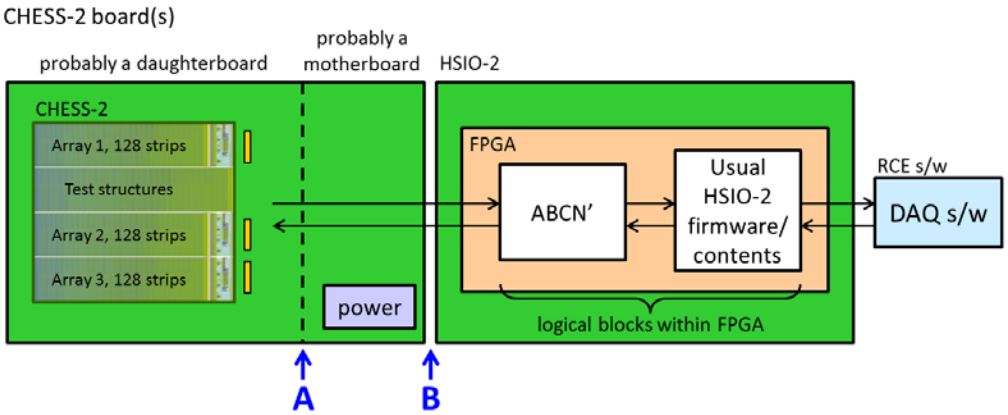
Phase 2



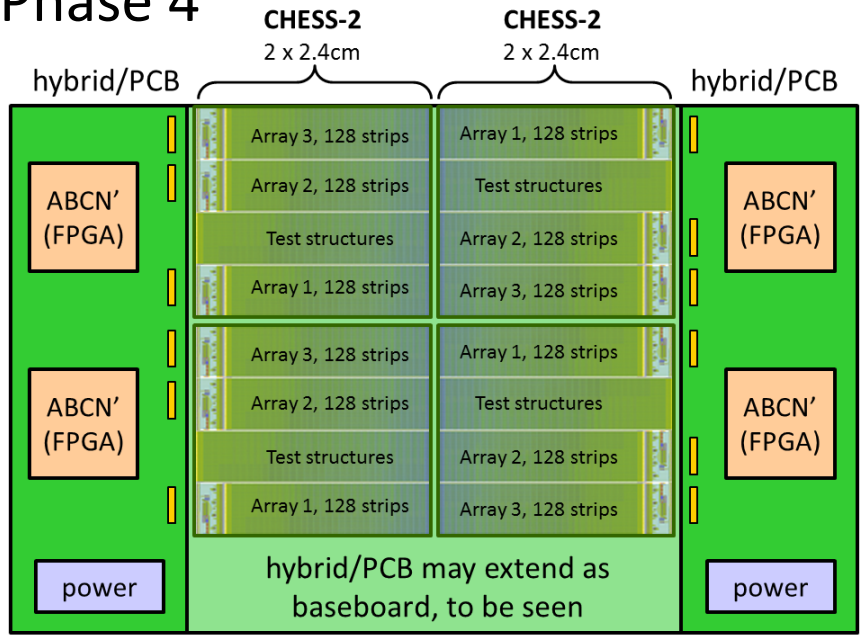
From last ABCN' meeting: agreed it is important to test timing at interface between ABCN' and DAQ, so this step is needed (either with Atlys or Nexys Video as DAQ)

ABCN' – updated hardware summary, 2/2

Phase 3



Phase 4



From last ABCN' meeting: agreed it's important that **B** is a standardised interface such as FMC.

Ideally, this would be an HPC FMC where the pins are set up so that an LPC FMC would have access to 2 of the 3 of the CHESS-2 arrays.

A could be an edge connector à la CHESS-1?

CMOS demonstrator module

(same as presented at CMOS meeting of 15th March)