

Charge Collection Measurements in irradiated AMS CHES 1 and TowerJazz CHES 1 PonP HVCMOS Prototypes

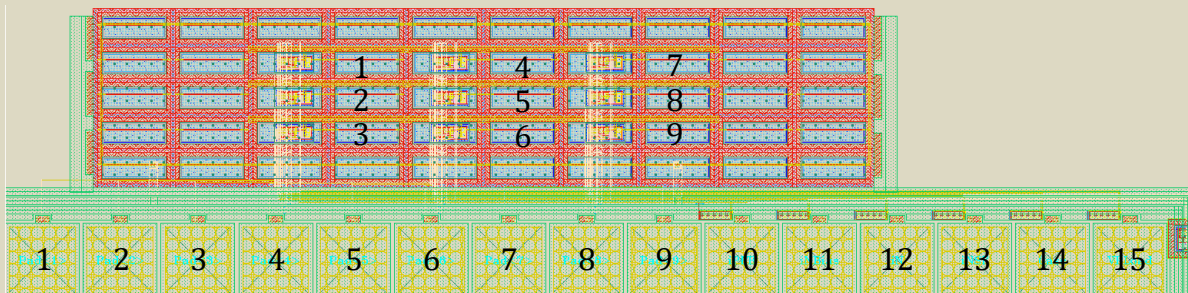
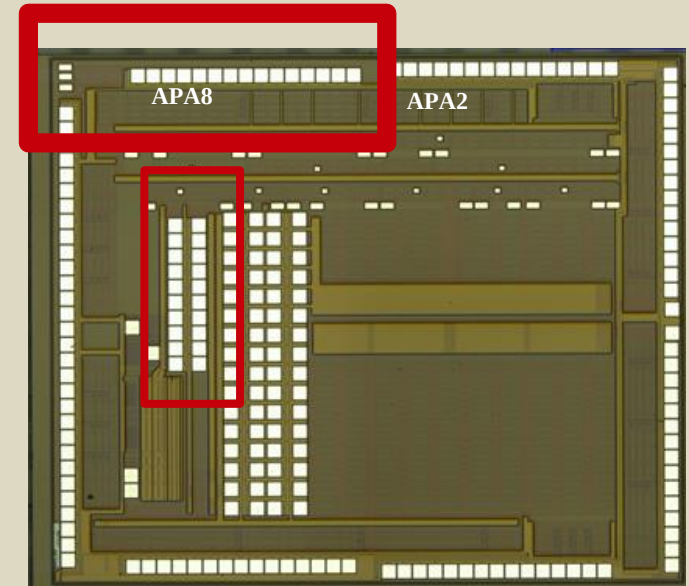
ATLAS Strip CMOS Regular Meeting, 12 April 2016

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AMS CHESS 1 Sample

- 350 nm, 20 Ω , max. bias voltage 120 V, active pixels
- Irradiated at CERN PS in November 2015
 - low fluence (1 sample) – 3.3×10^{14} neq cm^{-2}
 - high fluence (1 sample) – 4.8×10^{14} neq cm^{-2}
 - annealed 80 min at 60°C
- Active pixel array for edge TCT:
 - APA08: 3x3 pixels, $800 \times 45 \mu\text{m}^2$
- Isolated amplifier array
 - comparison of responses at different fluences



exemplary layout of a 3x3 APA ($200 \times 45 \mu\text{m}^2$)

Global DAC Settings

- Chip DACs in irradiated samples have to be tuned
 - For VPFB > 2500 mV no signal output
- Greater laser power compared to unirradiated sample needed

CONFIG 7

VPLOAD	2100
VCASC	2600
VNSF	570
VN	1000
VBIAS	340
VPFB	2664

CONFIG 8 (standard)

VPLOAD	2100
VCASC	2600
VNSF	750
VN	1000
VBIAS	150
VPFB	2700

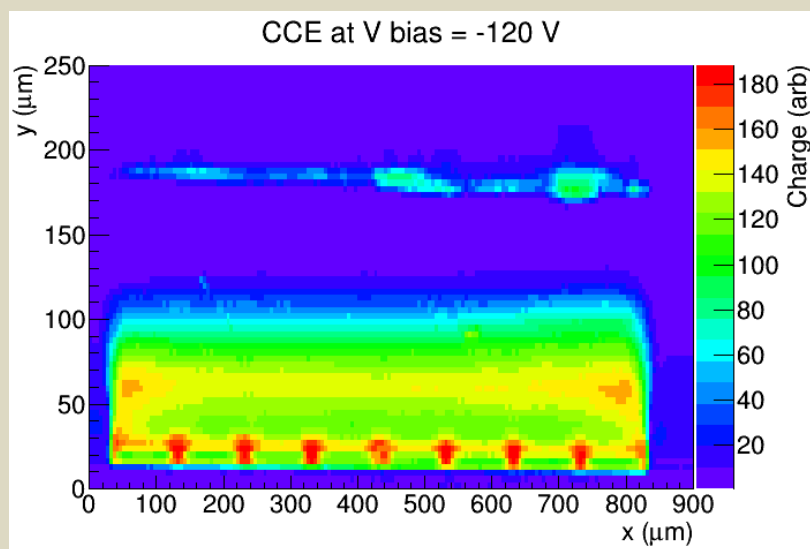
CONFIG IRRAD

VPLOAD	2100
VCASC	2600
VNSF	570
VN	1000
VBIAS	300
VPFB	2500

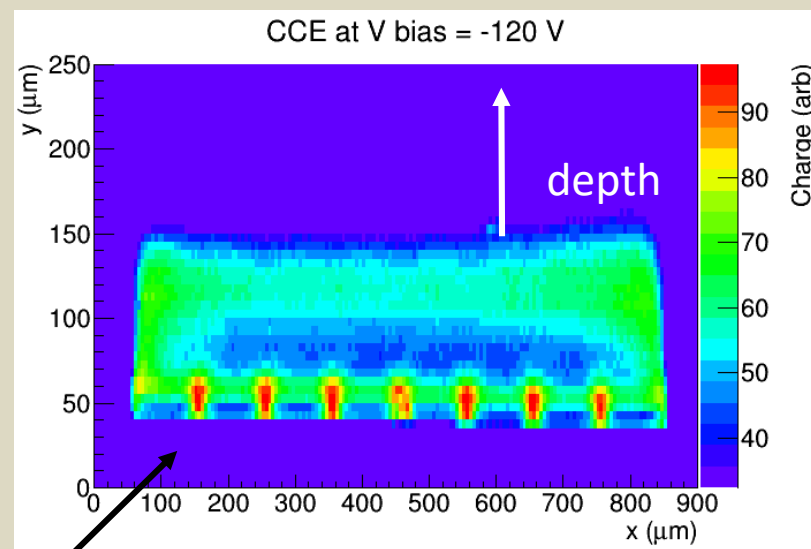
Low Fluence 2d E-TCT Scans

APA08 pixel 5

before annealing



after annealing

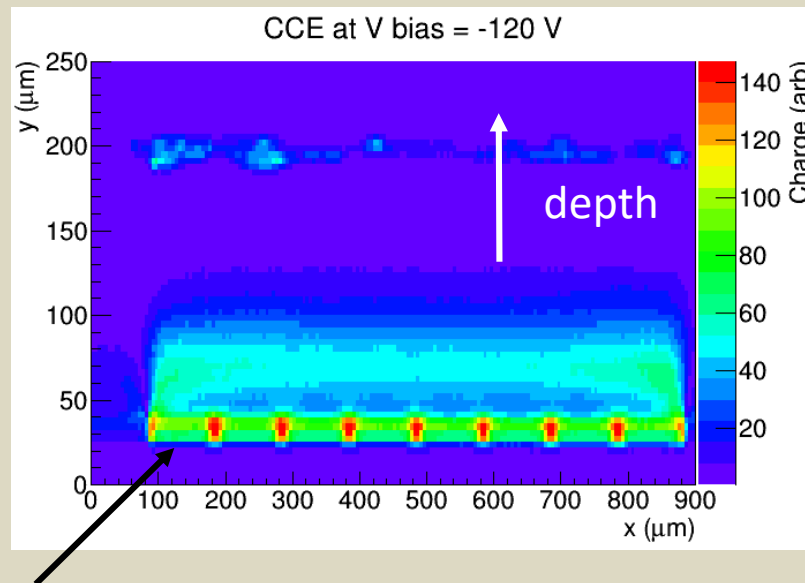


chip surface

High Fluence 2d E-TCT Scans

APA08 pixel 5

after annealing

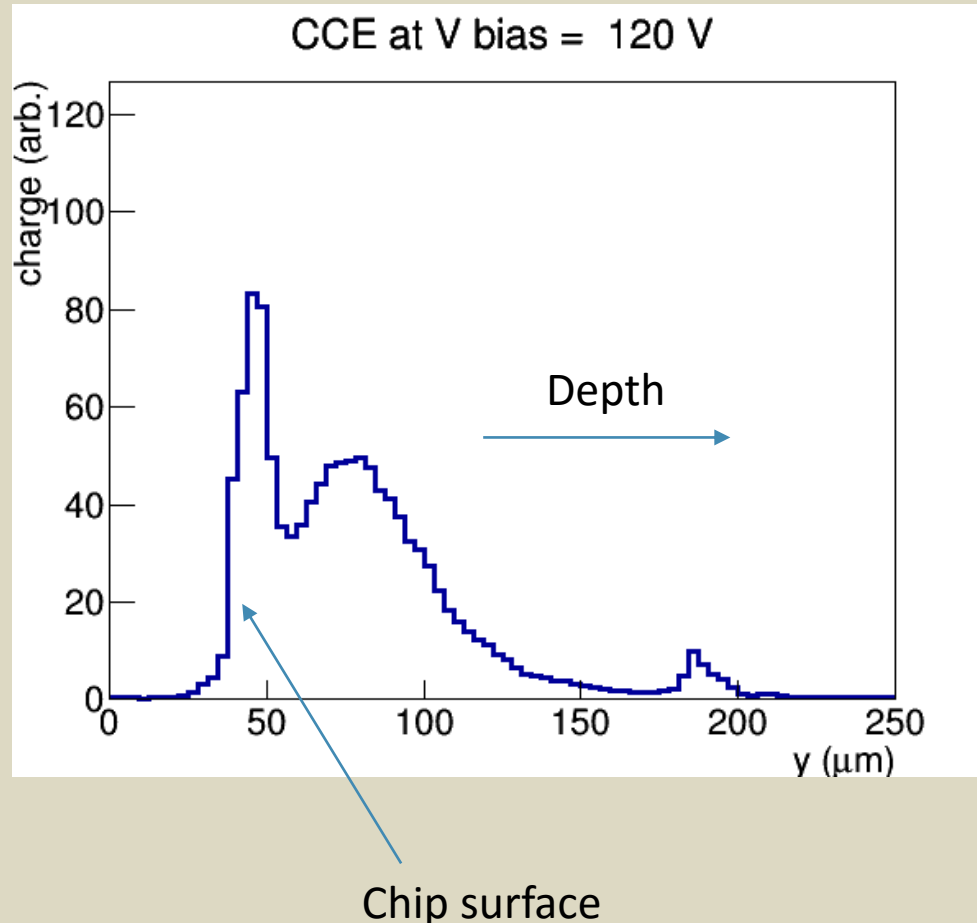


chip surface

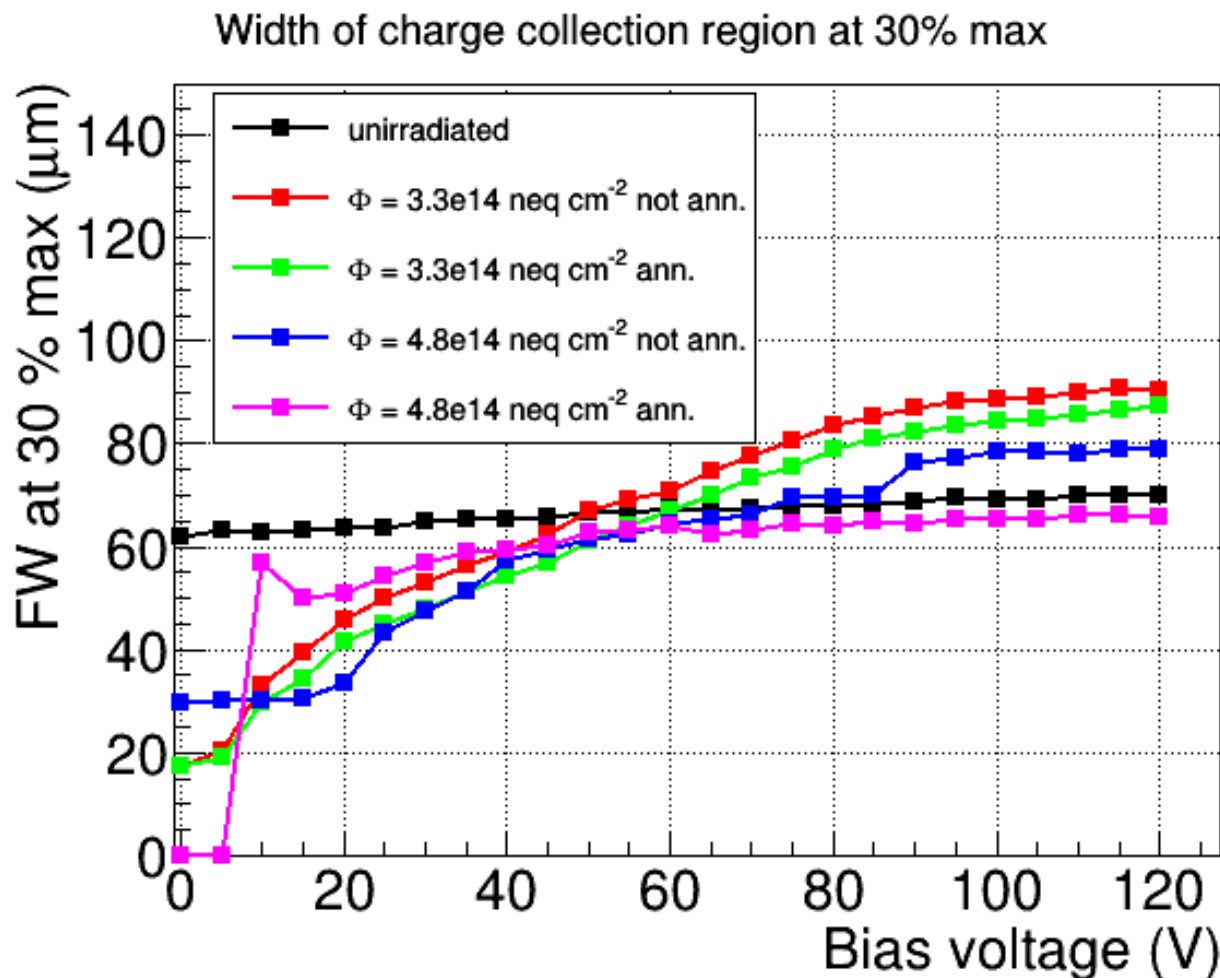
VPFB had to be changed
2500 mV $\rightarrow$ 2600 mV
after annealing

Size of the Depleted Region

- Width of depleted region calculated as Full Width at 30 % of charge collection profile
- Measured for different fluences and before/after annealing

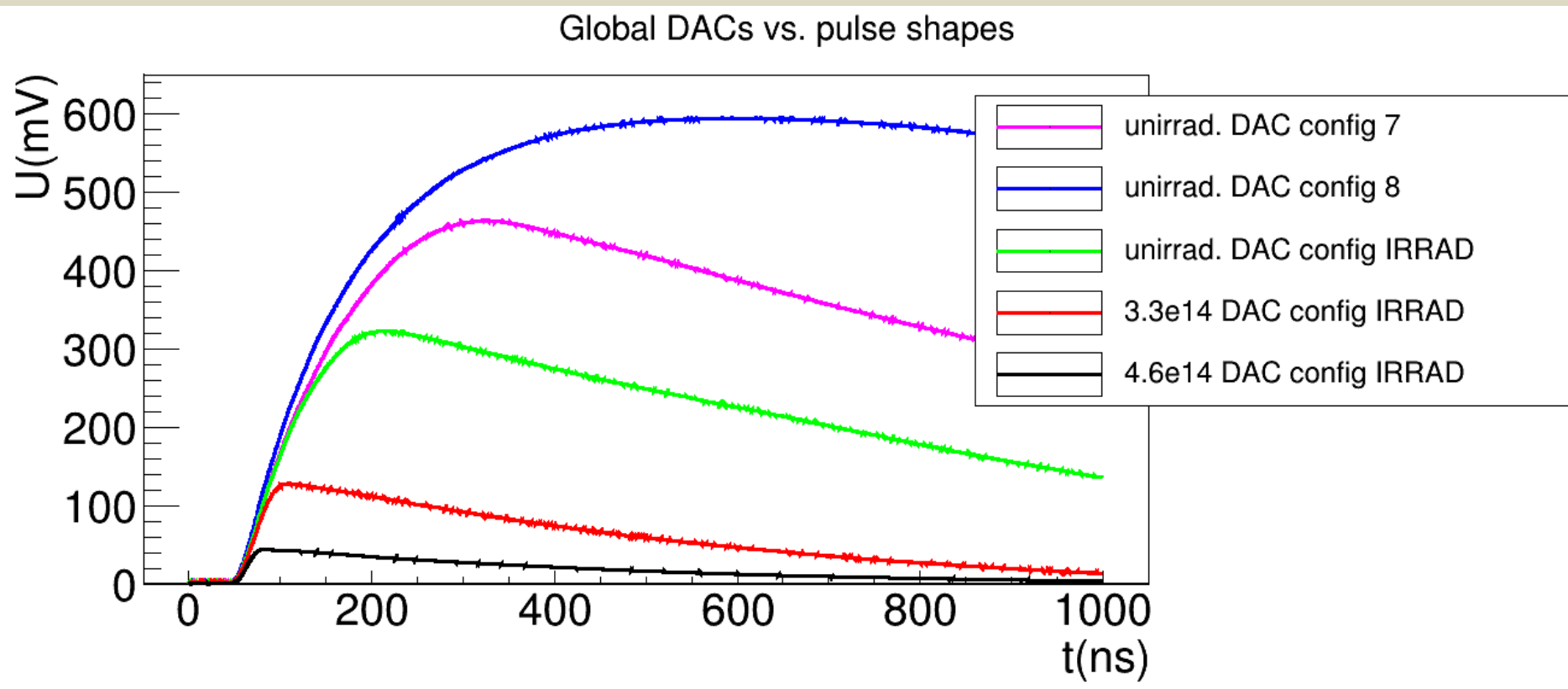


APA08 Depletion Depth vs. Bias



Reminder: Pixel Gain after Irradiation

- Pulse shape on 3 different samples measured (unirrad., low fl., high fl.)
- Same amount of light injected
- 120 V bias



Reasonable amount of charge collected from the sensor
→ Gain reduces after irradiation

Gain on Isolated Amplifiers

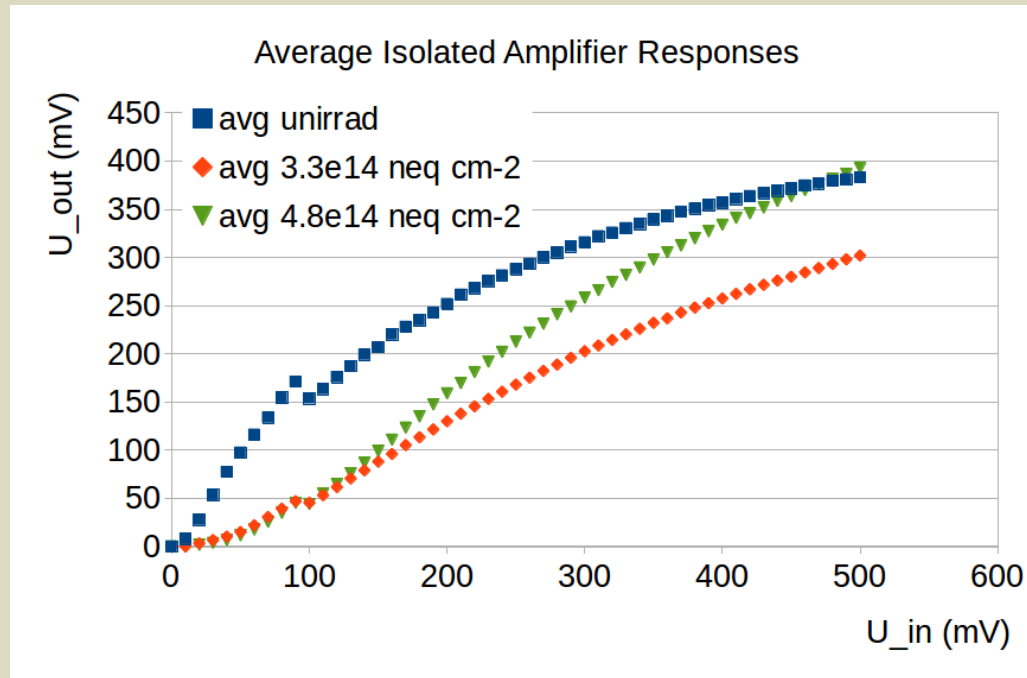
- Cross check gain evolution with fluence on isolated amplifiers
 - 3 – 5 bonded isolated amplifiers on each sample (variation on chip 20 %)
- External pulse injection via 4 nF capacitance:
 - pulse amplitude 0 – 500 mV
 - step function, ON time 10 μ s, frequency 1 kHz

DAC CONFIG

VPLOAD	2100
VCASC	2600
VNSF	570
VN	1000
VBIAS	340
VPFB	2200

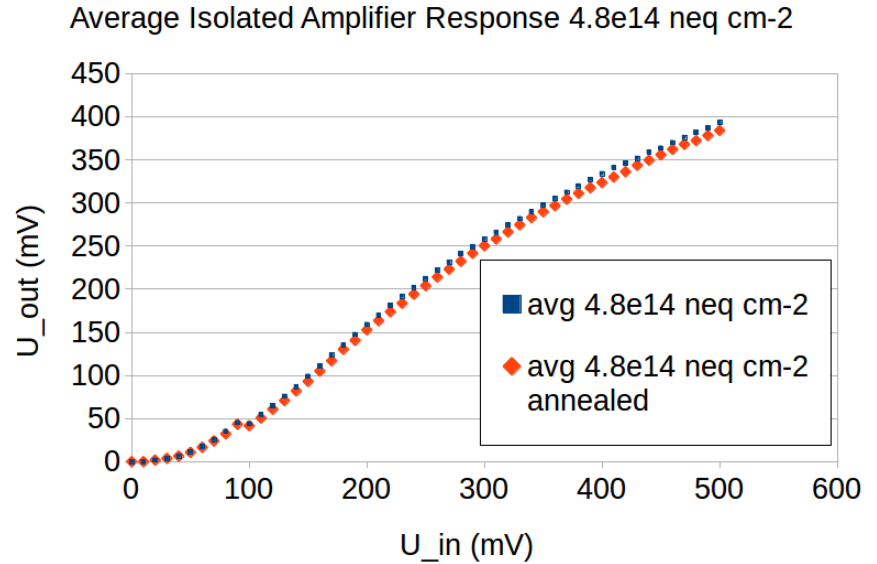
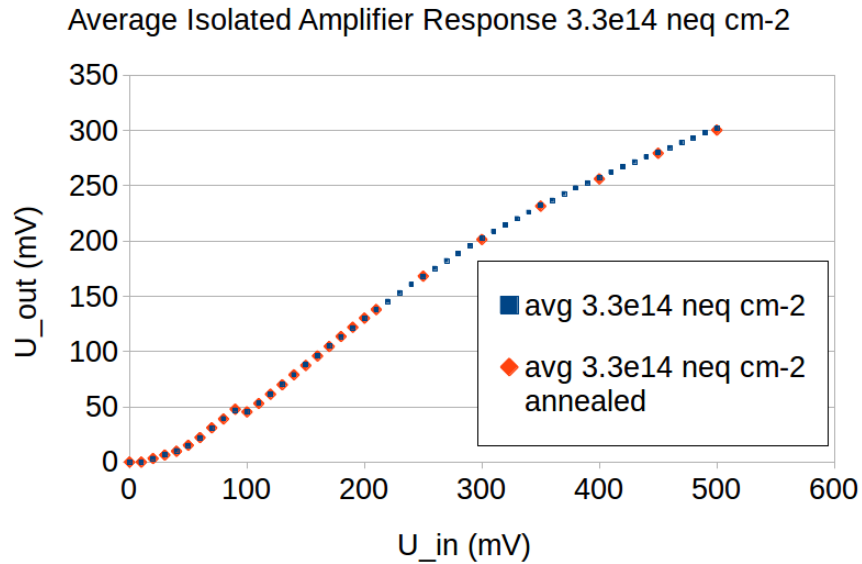


Gain on Isolated Amplifiers



- Factor 3 difference between unirrad. and irradiated samples in the low amplitude domain
- Can to some extent explain the drop in the gain after irradiation
- Does not explain the variation between low and high fluence

Annealing on Isolated Amplifiers



- No changes in the isolated amplifier response after annealing

TowerJazz CHESS 1 Sample

- 180 nm process
 - epitaxial layer 1 kOhm cm, thickness 20 μm – for charge collection
 - 2 chip designs: PonP, PonN – substrate type
 - small collecting electrodes
 - electronics in deep p-well
-
- We measure bulk properties with E-TCT

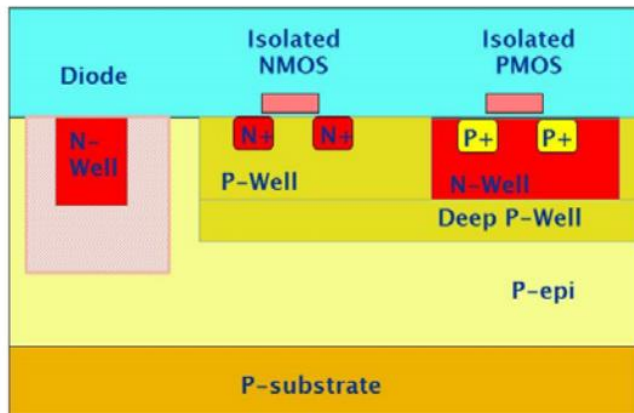


Figure 1. Cross-section of a PonP pixel

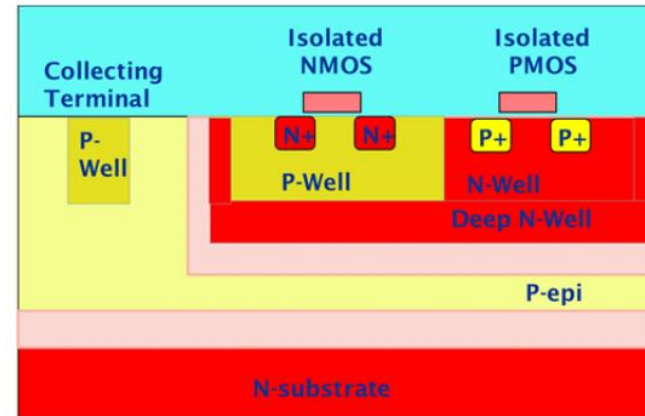
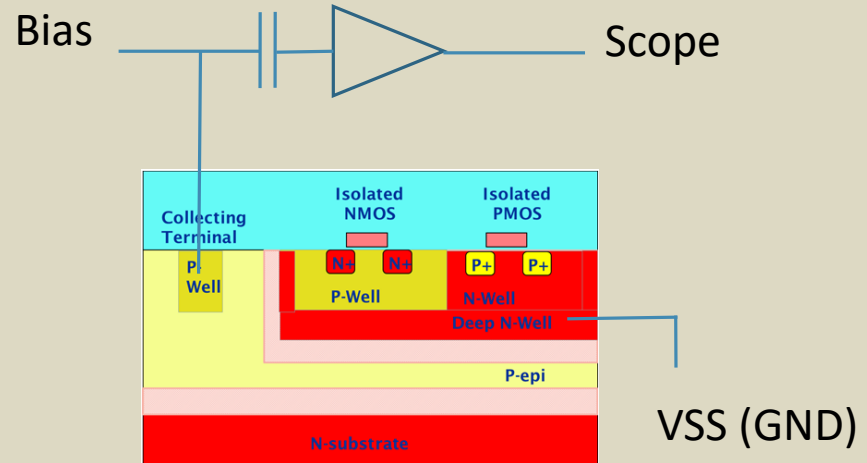


Figure 2. Cross-section of a PonN pixel

TowerJazz CHESS 1 PonN



structure 28
passive pixel array
pixel size $40 \times 40 \mu\text{m}^2$



Surrounding
8 pixels

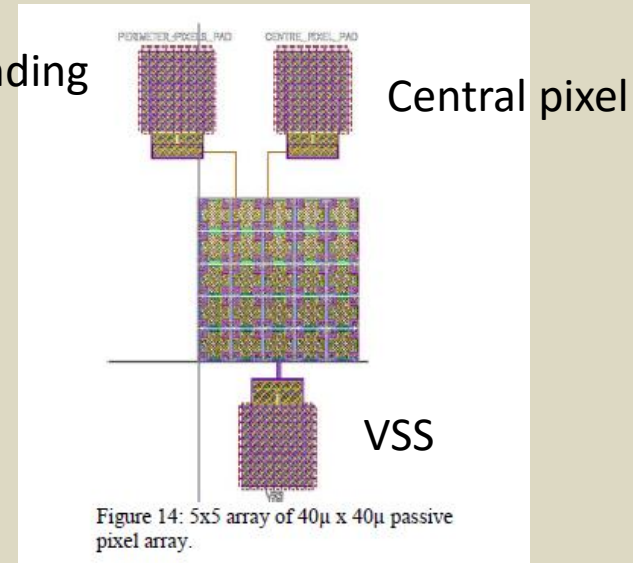
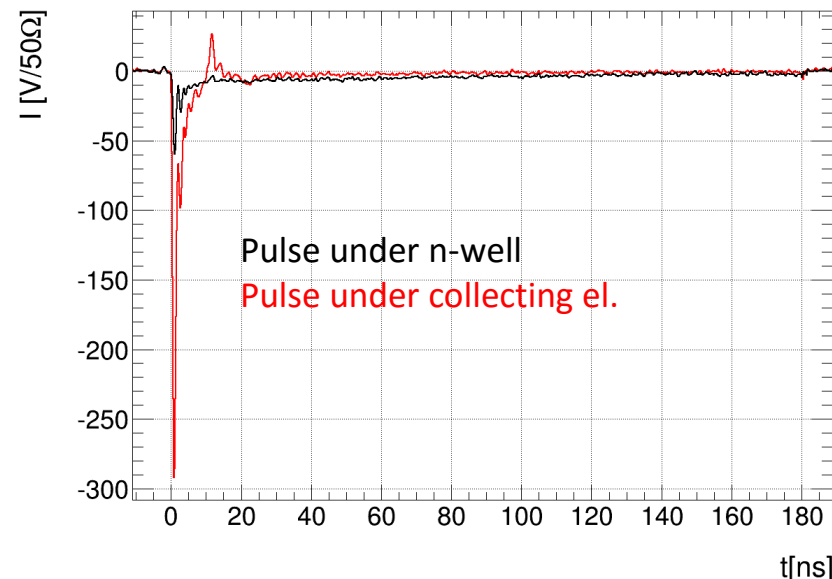
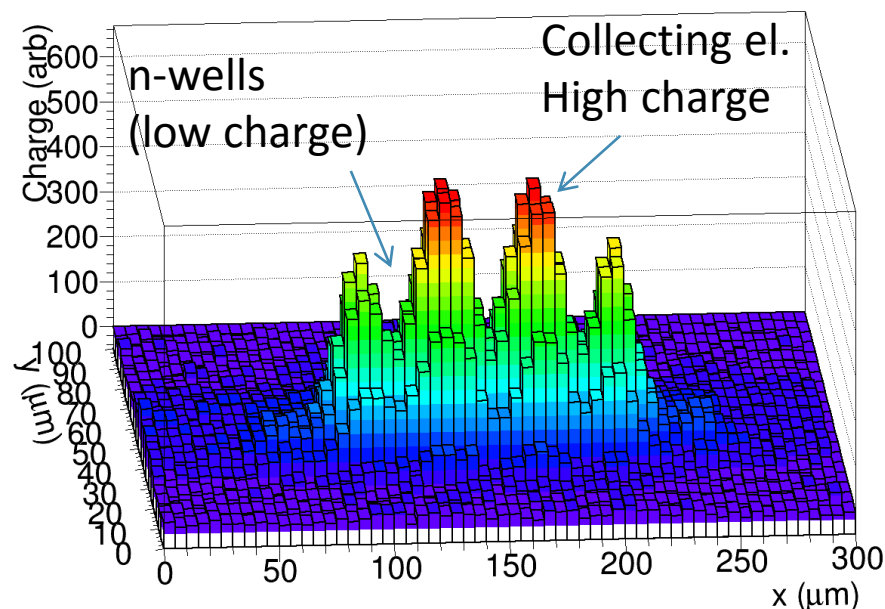


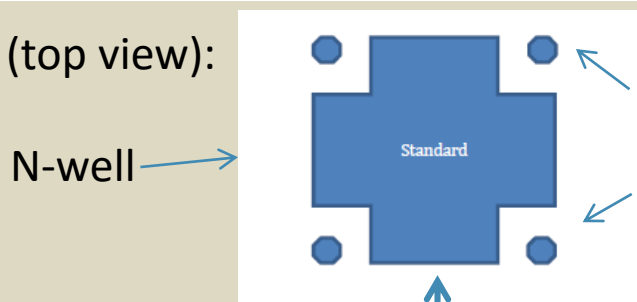
Figure 14: 5x5 array of $40 \mu\text{m} \times 40 \mu\text{m}$ passive pixel array.

Charge Collection PonN

- high currents: 7 μA when collecting electrode at -1.5 V
- bias -1.5 V, 9 pixels read out, charge (25 ns integration)

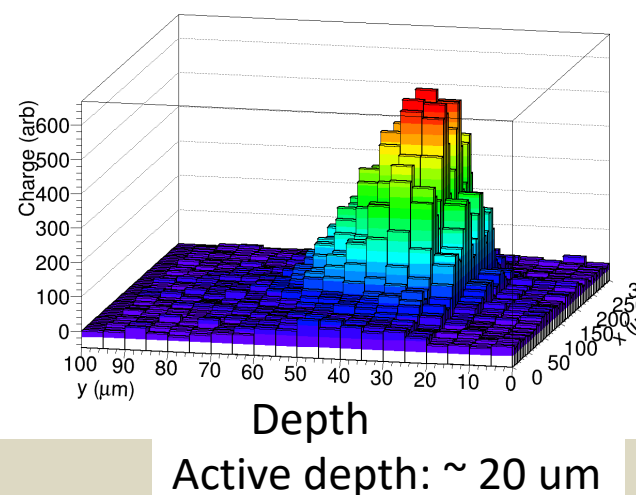


Pixel (top view):

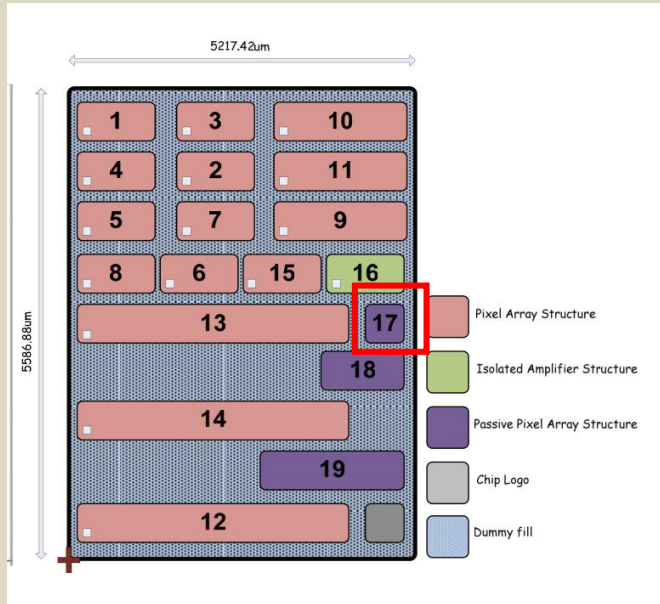


Collecting electrodes

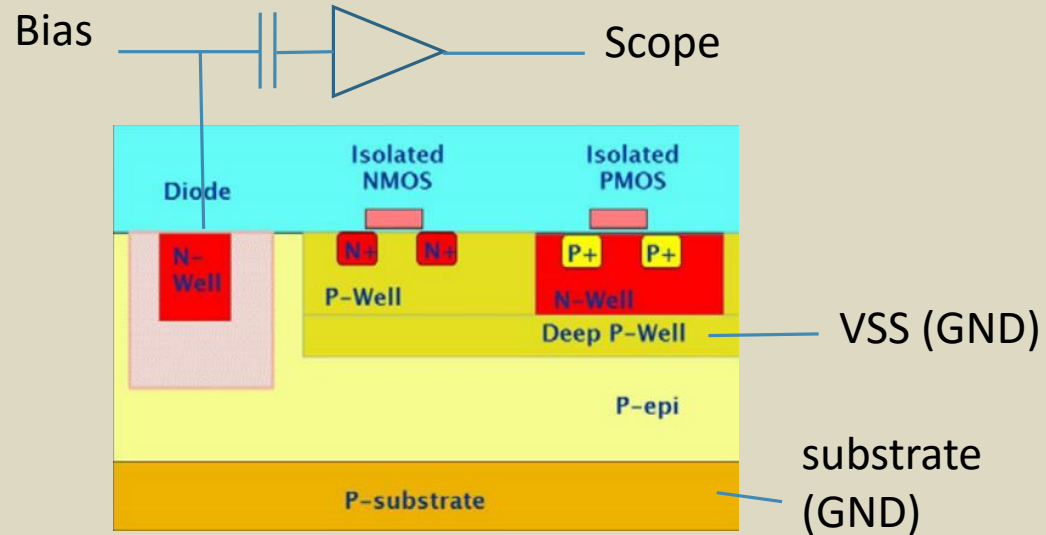
Laser beam direction



TowerJazz CHESS 1 PonP



structure 17
passive pixel array
pixel size $40 \times 40 \mu\text{m}^2$



not correct bias configuration for active pixels

Surrounding
8 pixels

Central pixel

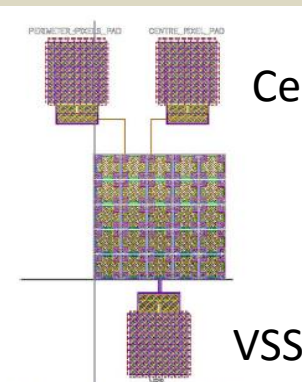
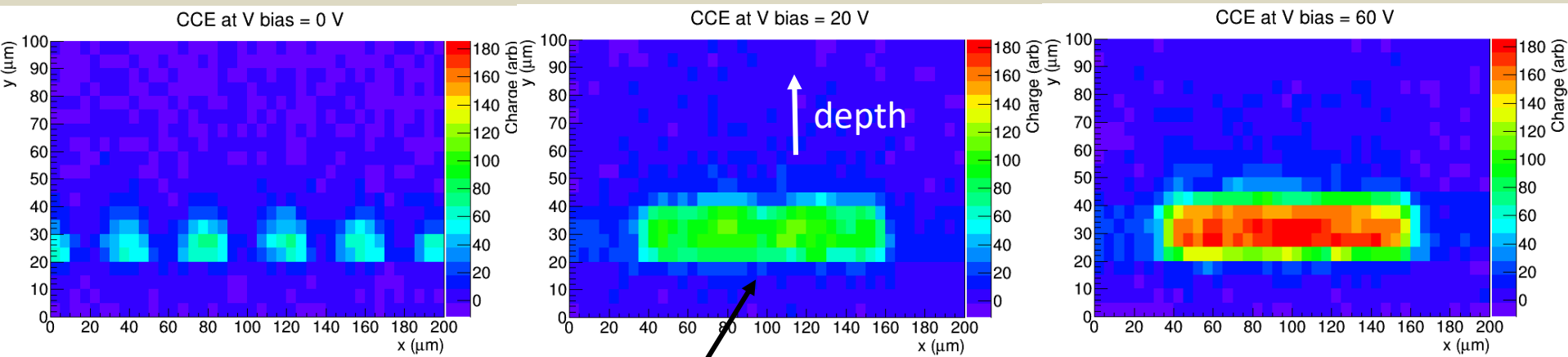


Figure 14: 5x5 array of $40 \mu \times 40 \mu$ passive pixel array.

Charge Collection PonP

- bias voltage up to 60 V (current $< 1 \mu\text{A}$) – not correct bias configuration for active pixels
- 9 pixels read out, charge (25 ns integration)

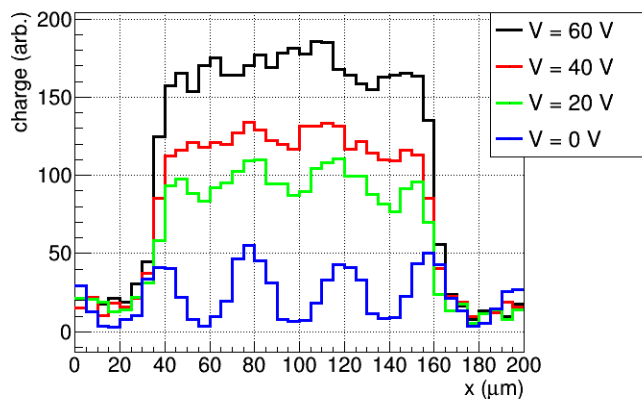


cross section x

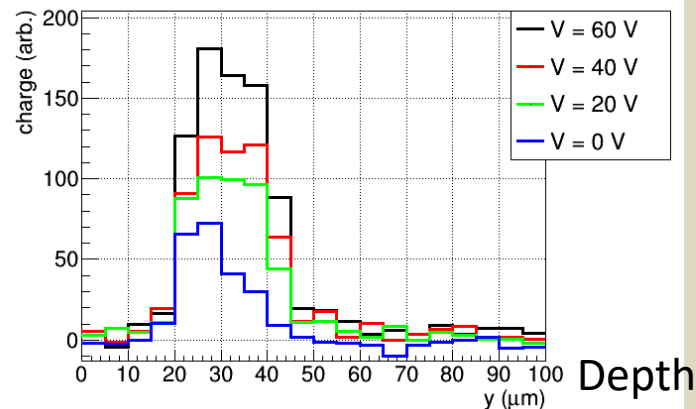
chip surface

cross section y

CCE at $y=30 \mu\text{m}$

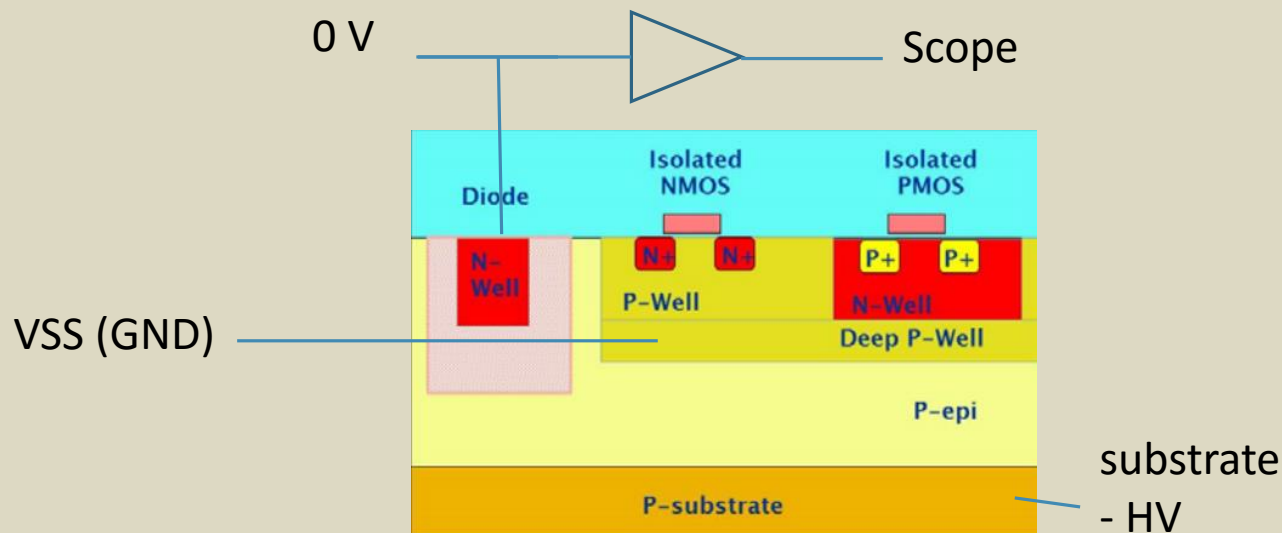


CCE at $x=120 \mu\text{m}$



Active depth: approx. 20 μm

Correct bias configuration for PonP



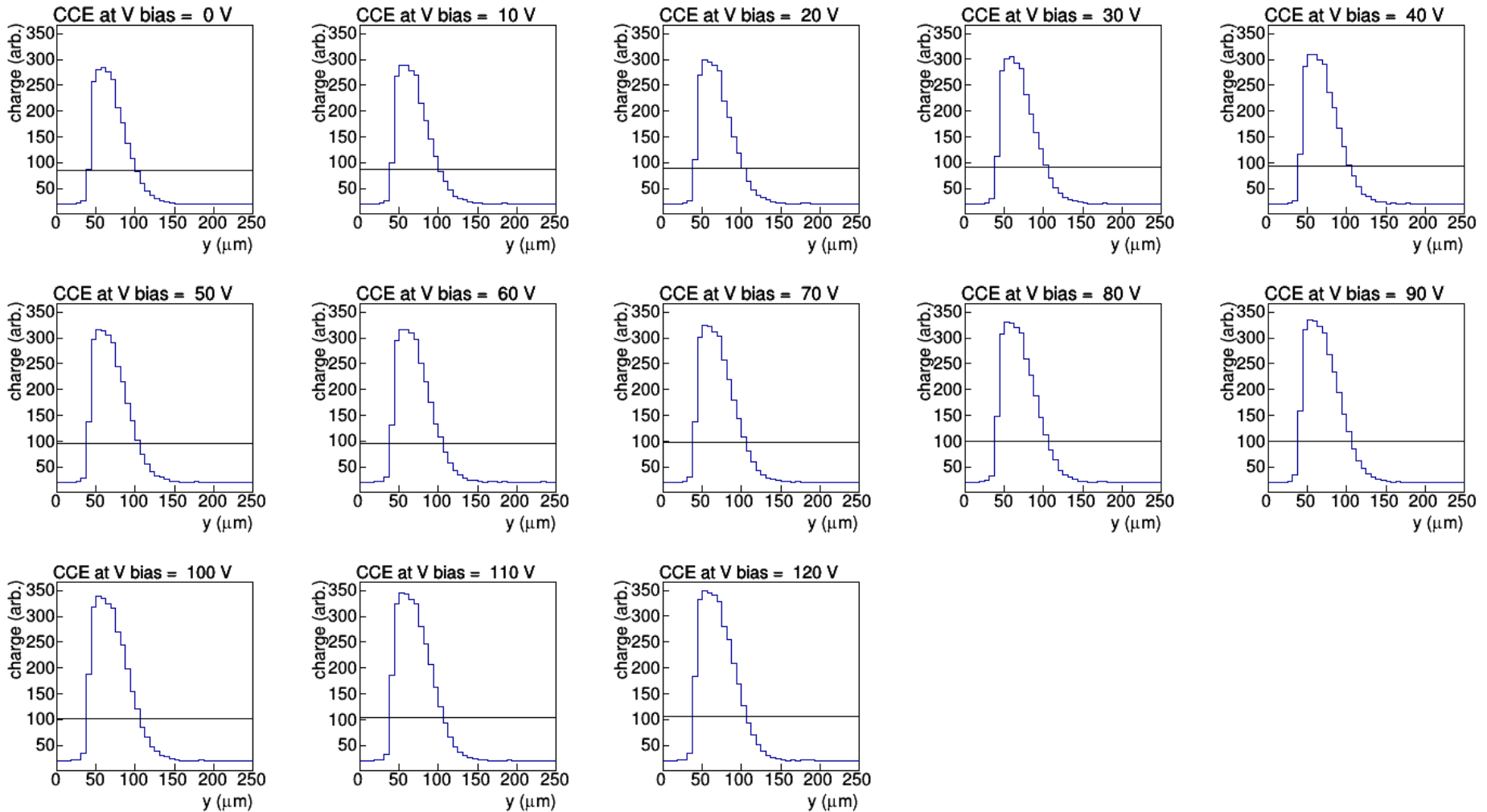
High leakage current
 $1\ \mu\text{A}$ at $-2.5\ \text{V}$



- AMS CHESS 1
 - measured charge collection in proton irradiated sample + annealing
 - isolated amplifier tests indicate gain drop after irradiation, however not conclusive
- TowerJazz CHESS 1
 - first E-TCT measurements done with PonN and PonP
 - observed signal from the entire epitaxial layer
 - Feature sizes in agreement with design values
 - High leakage currents

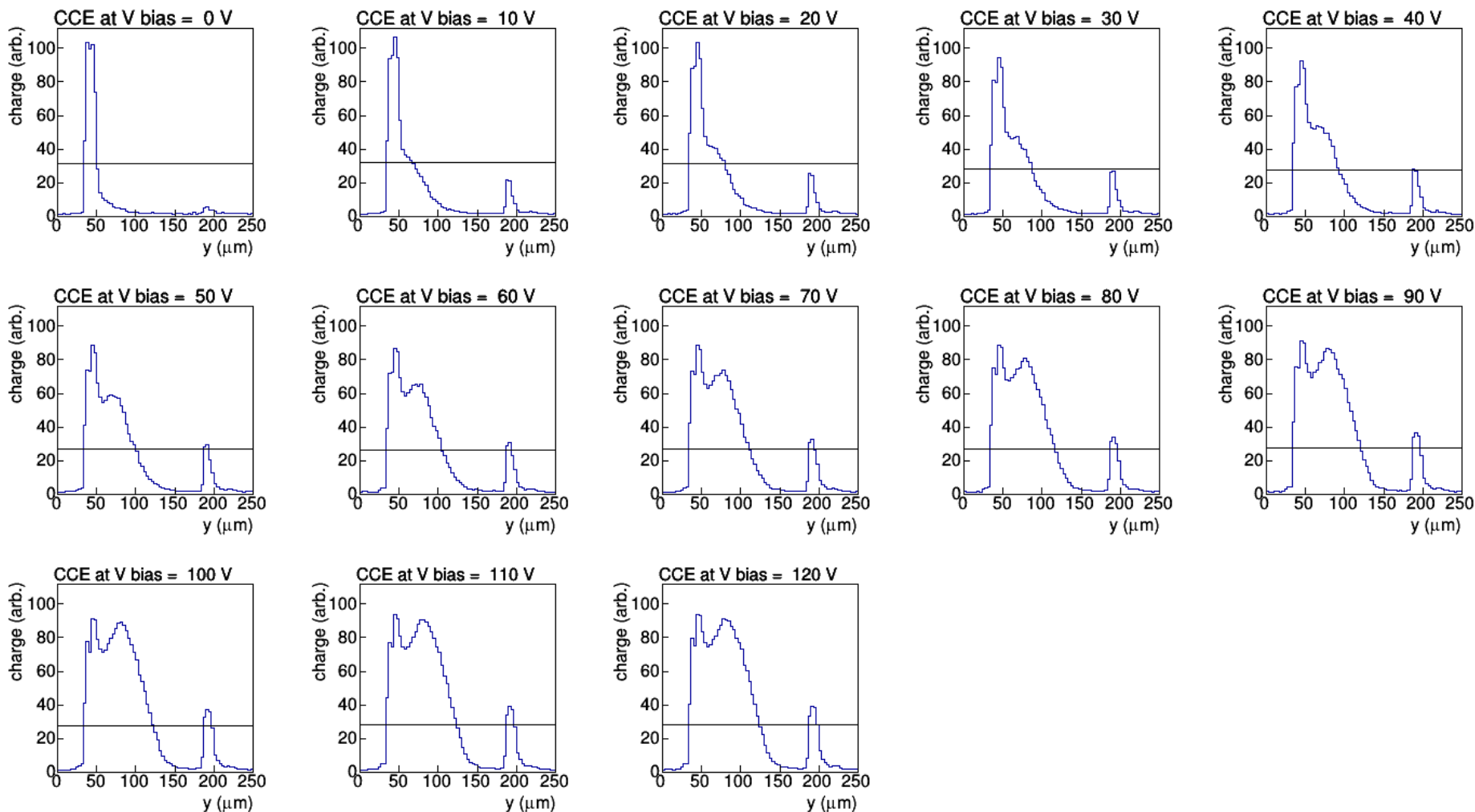
AMS Charge collection profiles – unirradiated

unirradiated



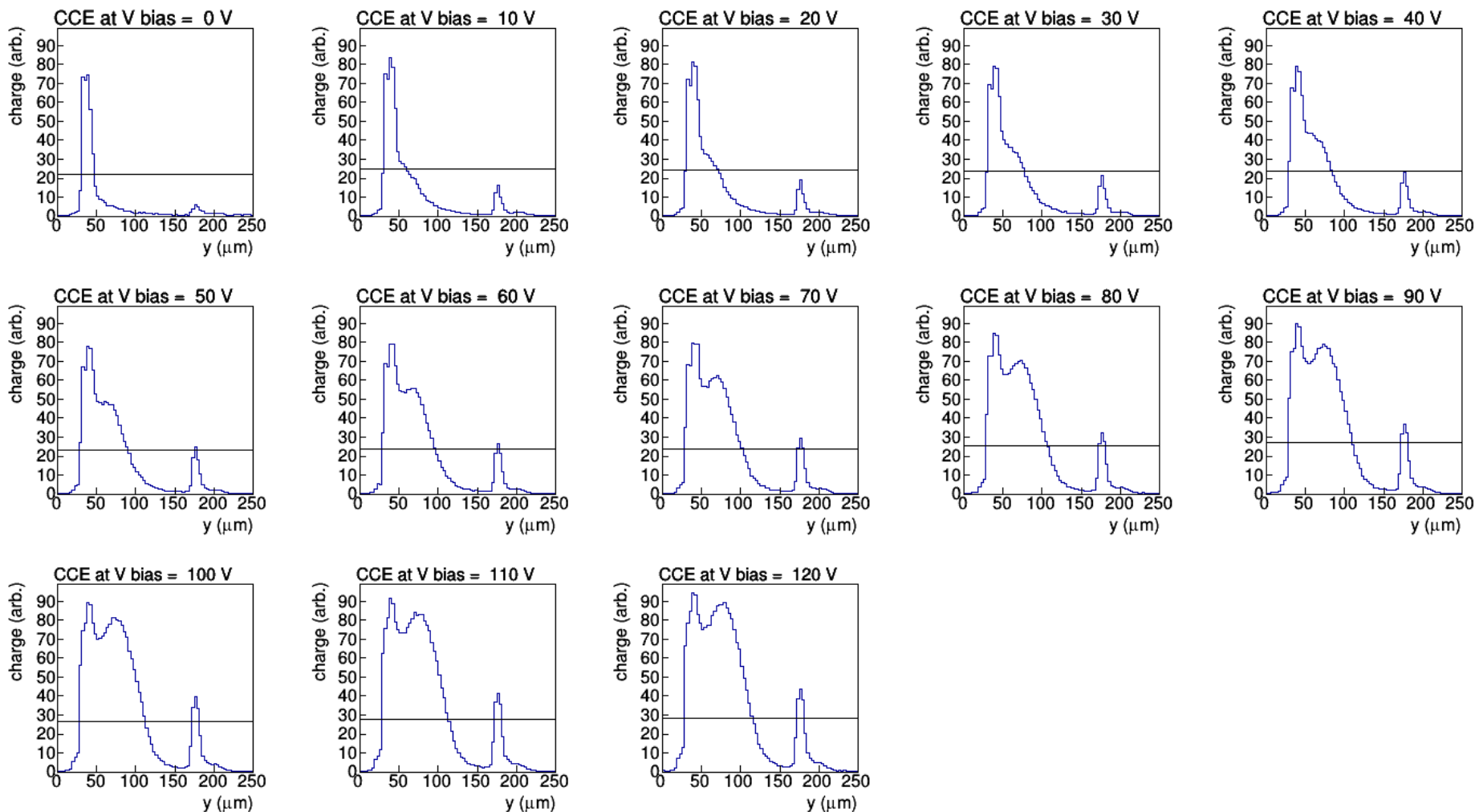
AMS Charge collection profiles – 3.3e14

3.3e14 neq cm⁻², not annealed



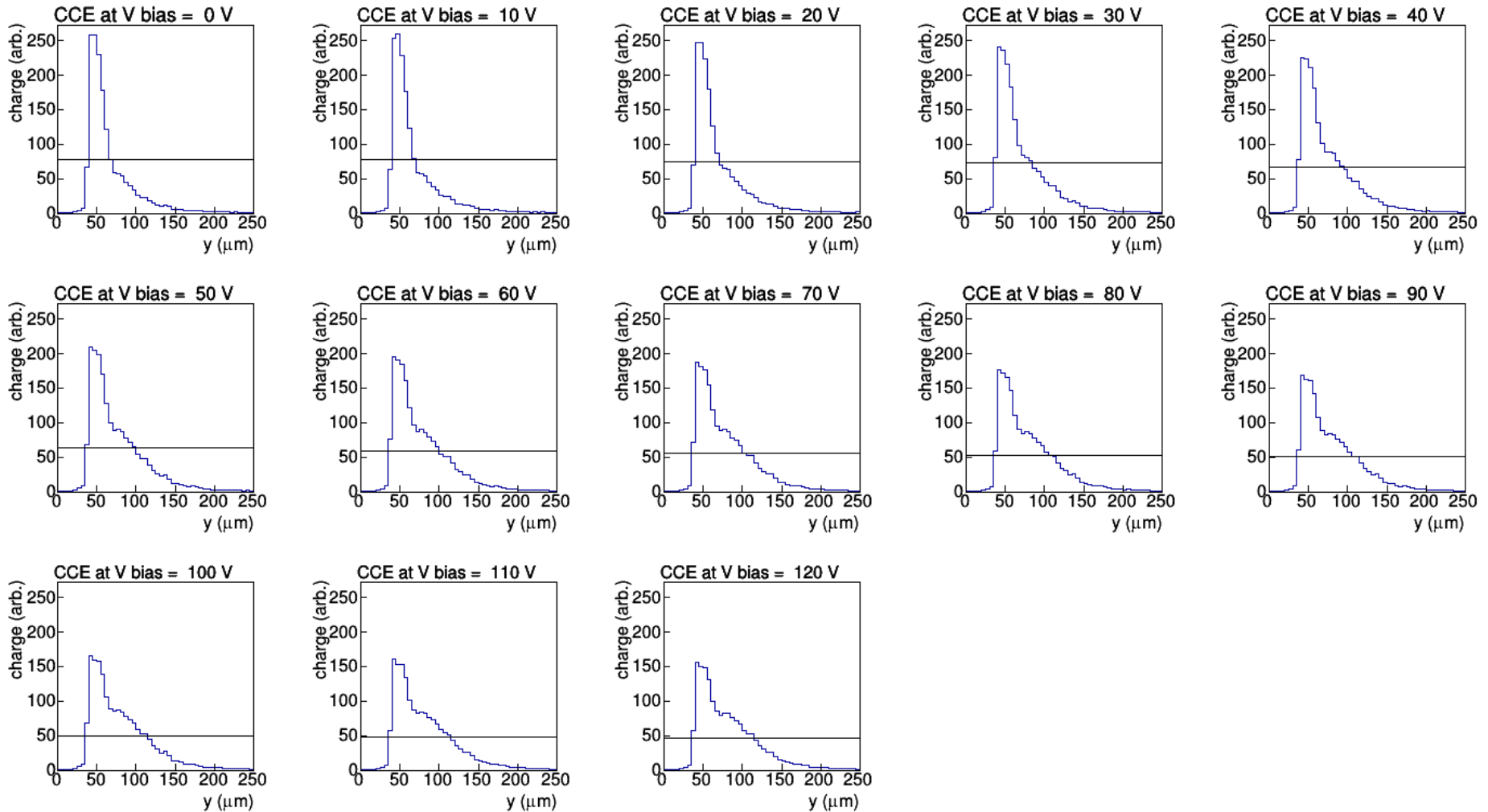
AMS Charge collection profiles – 3.3e14

3.3e14 neq cm⁻², annealed



AMS Charge collection profiles – 4.8e14

4.8e14 neq cm⁻², not annealed



AMS Charge collection profiles – 4.8e14

4.8e14 neq cm⁻², annealed

