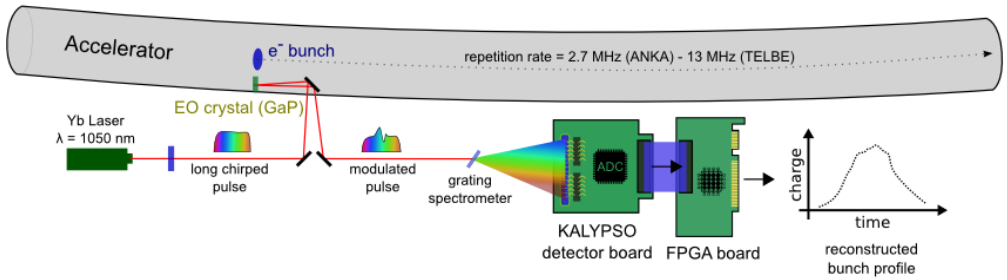
KALYPSO: a 2.7 Mfps linear-array detector for visible to NIR radiaton

Motivation:

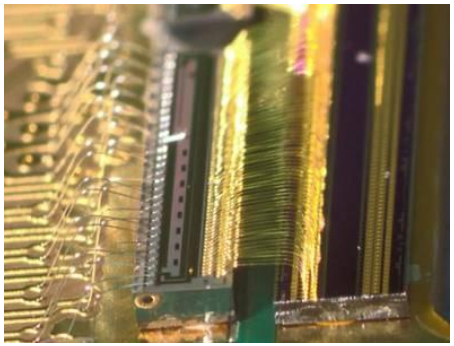
- To be used in new-generation of beam diagnostics setups (LINAC, synchrotrons)



Goal:

- A linear-array detector with **continuous** frame-rate in the **MHz** range

Technological challenges:



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4th ARD ST3 Workshop, 13-15 July 2016, Berlin

Institute for Data Processing and Electronics

KALYPSO: a Mfps linear array detector for visible to NIR radiation

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Motivation

Scientific motivation

Scientific goal:
Study the e⁻ bunch dynamics at linear accelerators (XFEL, TELBE) and synchrotrons (ANKA, DELTA)

"Ideal" linear
- Visible / N
- High frame-rate: MHz range
- Synchronization with accelerator machine and other detectors not easily implemented

KALYPSO 2.1 architec

Architecture & technological challenges

InGaAs sensor (Xenics):
- 256 pixels, 50 um pitch

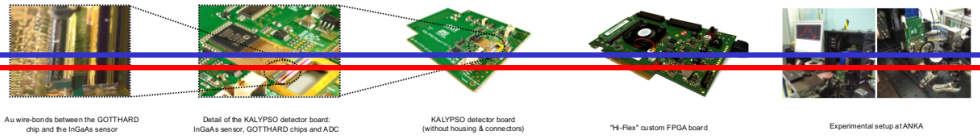
Si sensor (PSI):
- 256 pixels (diced), 50 um pitch

2x GOTTHARD 1.6:
- Charge sensitive preamplifier
- 128 inputs, 8 analog outputs
- Max line-rate: 2.7 MHz
- Designed at PSI

RF Clock (62.5 MHz)
Fast trigger (2.7 MHz)
Slow trigger (0.1 Hz)
PLL

Hi-Flex custom FPGA board:
- Xilinx Virtex 7, Speedgrade-2
- PCI-Express Gen3 x16 lanes (throughput of up to 13 GB/s)
- DDR3 memory interface (4 GB)

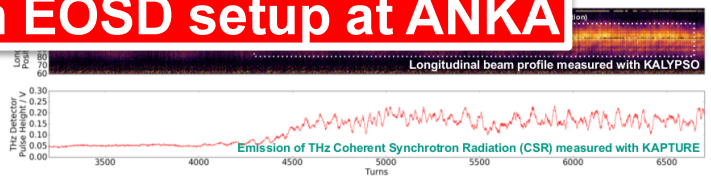
Custom GPU-based DAQ:
- Real-time data analysis
- Fast feedback to accelerator machine



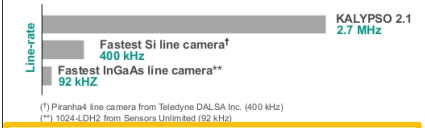
Au wire-bonds between the GOTTHARD chip and the InGaAs sensor | Detail of the KALYPSO detector board: InGaAs sensor, GOTTHARD chips and ADC | KALYPSO detector board (without housing & connectors) | "Hi-Flex" custom FPGA board | Experimental setup at ANKA

Results with EOSD setup at ANKA

KALYPSO at ANKA:
- First measurements done with InGaAs sensor
- Single-shot measurement at a line-rate of 2.71 MHz
- Continuous acquisitions over long observation times (> 10^6 shots, several seconds)
- Bunch substructures can now be resolved!



Comparison with commercial solutions



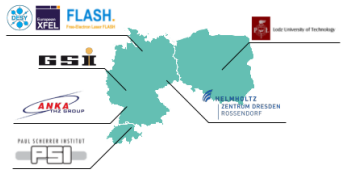
(†) Piranha4 line camera from Teledyne DALSA Inc. (400 kHz)
(**) 1024-LDH2 from Sensors Unlimited (92 kHz)

Future work: ASIC

Future work

First test chip submitted this week:
- UMC 110 nm (together with PSI)
- 48 channels pixels
- New Charge-Sensitive-Amplifier stage (higher gain, PSRR)
- Correlated Double Sampling stage
- Fully-differential
- Frame-rate > 5 Mfps (output stages working at 10 Mfps)

Partners



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National Research Center of the Helmholtz Association

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