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PSI

Paul Scherrer Institut

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GotthardII development status

XDAC Meeting, 14.12.2016

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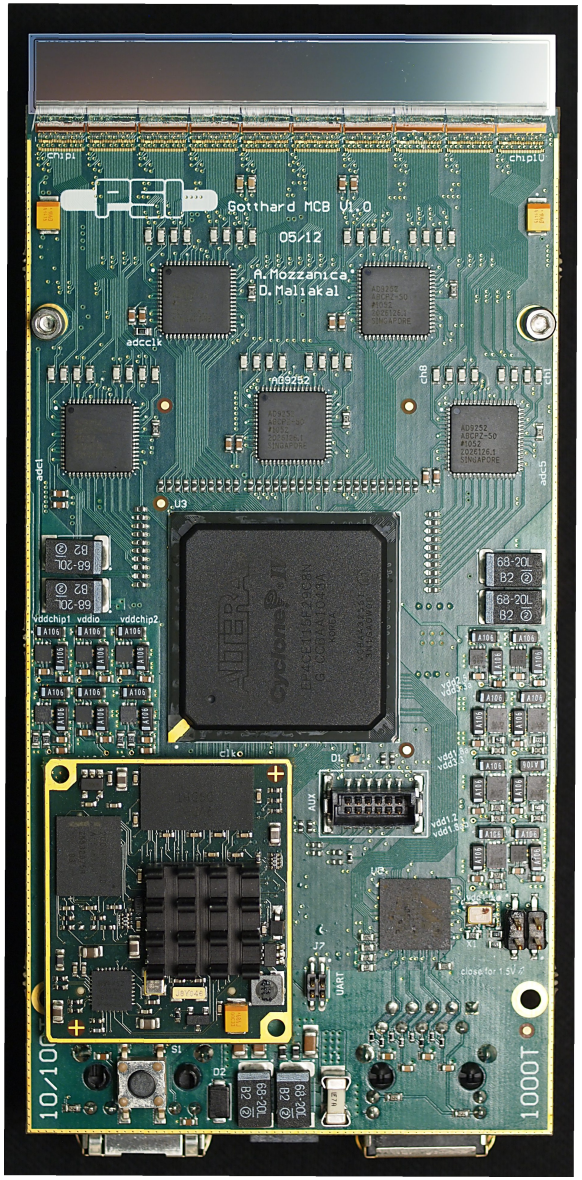
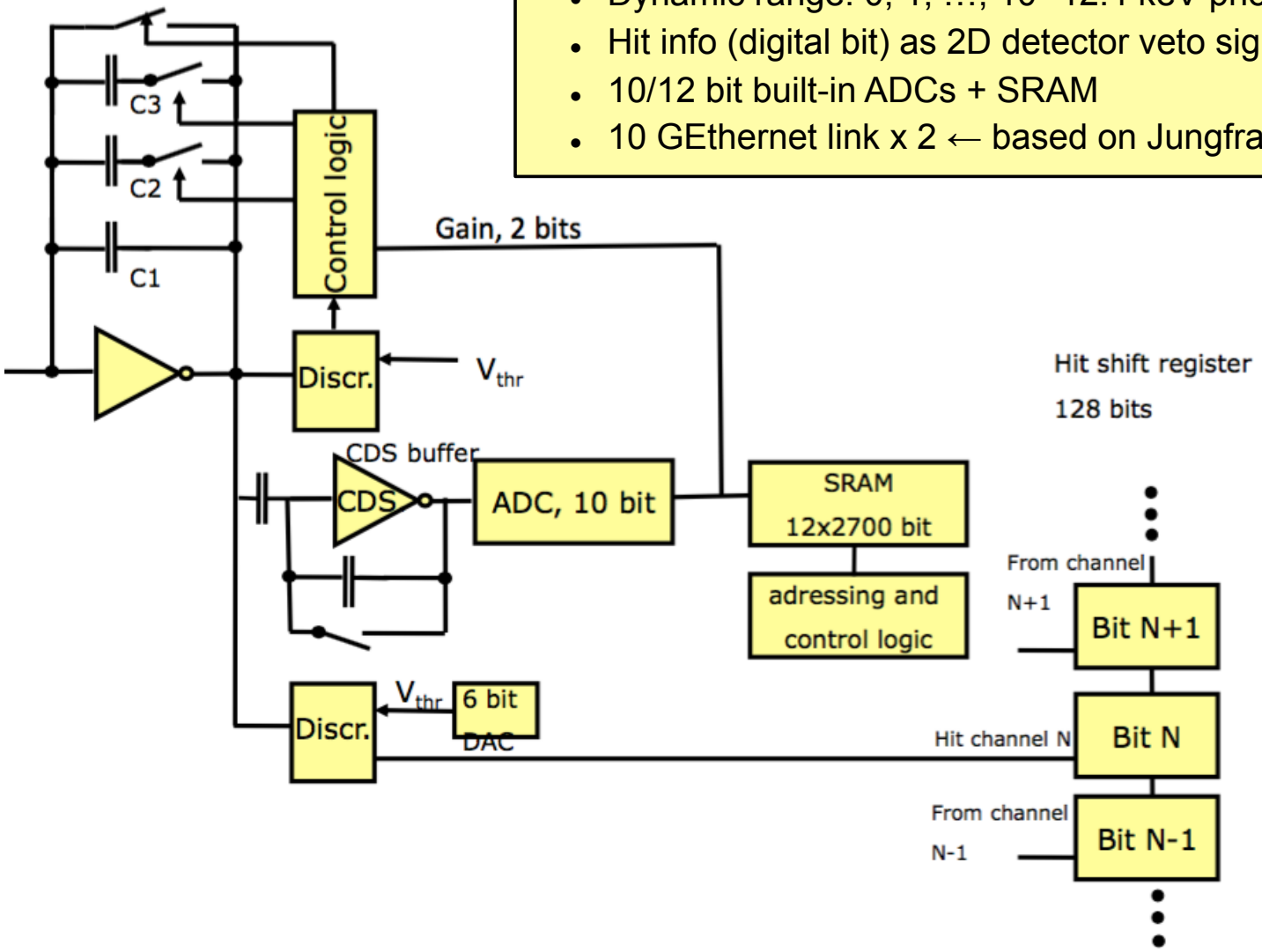
Reminder: GotthardI



- 67mm x 130mm
- 50 μm pitch, 1280ch/module (same as MYTHEN)
- 10 chips, 4 analog outputs per chip
- 40 ADC channels @32Mhz,14bits
- Gbit Ethernet data transfer for readout
- 100M Ethernet for slow control/setup
- Fast readout (1MHz) with ~600 bunches per EU-XFEL train measurable (memory for ~350)
- 60kHz continuous frame rate
- Integration in detector class for software control (same as Jungfrau)
- Developed in collaboration with Desy
- Start with GotthardI and replace it with GotthardII

Reminder of Gotthard-II: Schematic

- 4.5 MHz frame rate ← bunch structure of the Eu-XFEL
- Dynamic range: 0, 1, …, 10^4 12.4 keV photons
- Hit info (digital bit) as 2D detector veto signal
- 10/12 bit built-in ADCs + SRAM
- 10 GEthernet link x 2 ← based on Jungfrau read-out



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Outline

- Analogue Front End
  - Gotthard-1.4(&1.5) front-end problems
  - New analogue Front End Gotthard-1.7 first results
- ADC
  - Old ADC problems
  - New ADC, first results
- Current status

New FE and ADC were submitted in MPW in July

Received back beginning of December

results brand new and preliminary…

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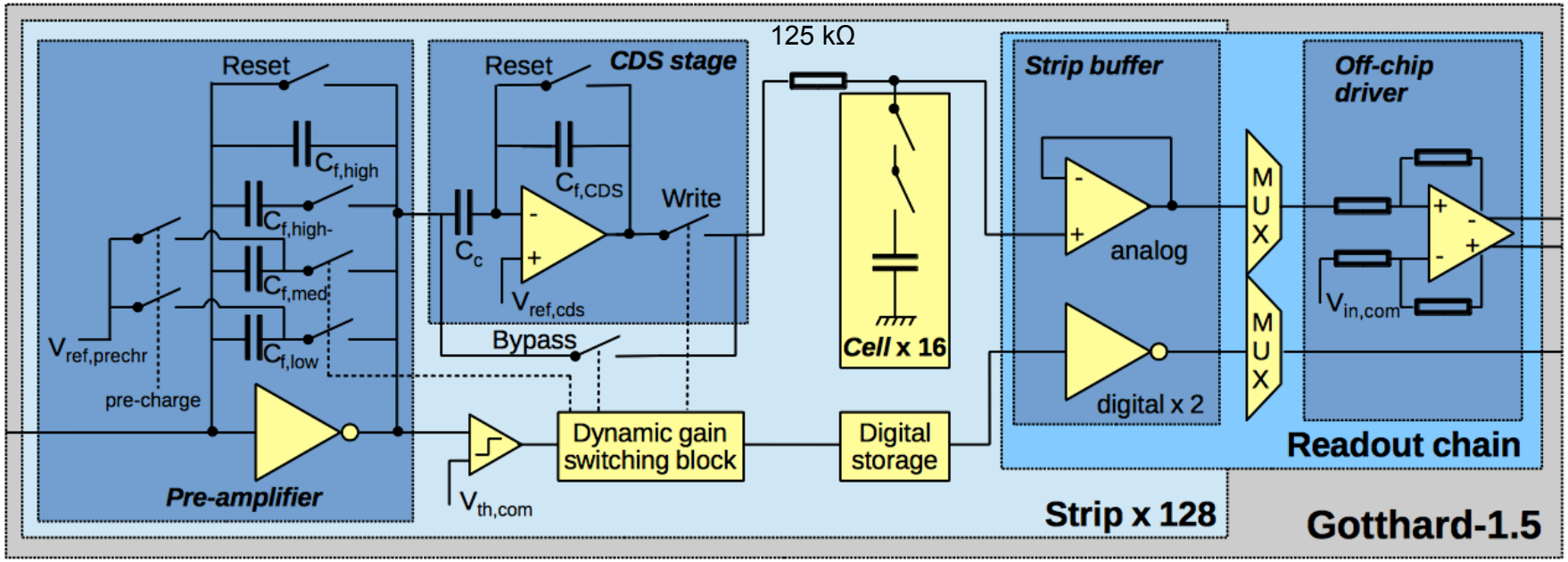
Gotthard-1.4&1.5 Architecture

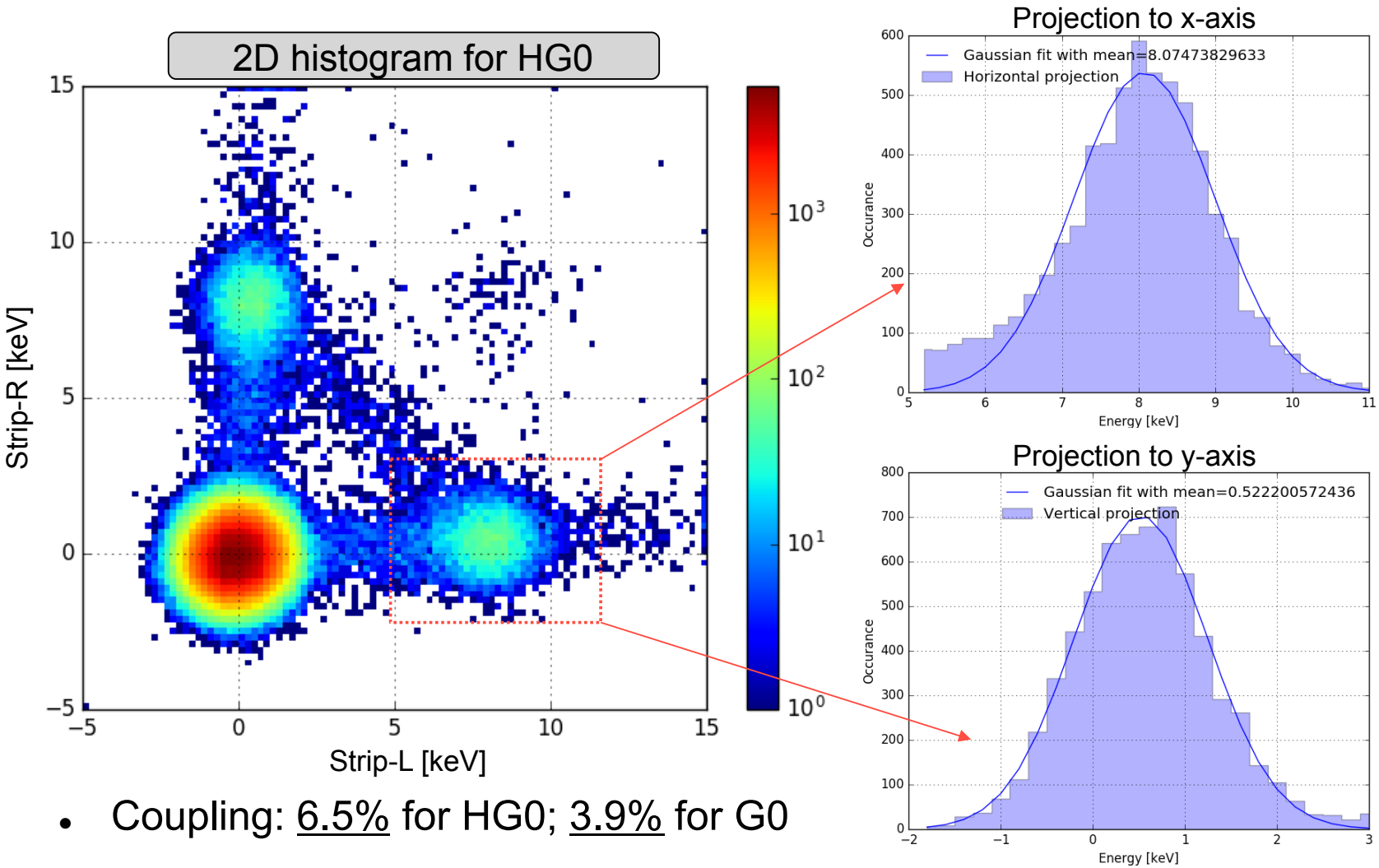
- To convert the GotthardI design from IBM 130nm to UMC 110nm
  we used the Jungfrau design and just scaled preamp
- The noise performance was good (175 e^- in G0), but the speed was too slow
  (forgot to remove the 125k resistor) and the capacitive cross talk
  due to the too low DC gain was too high

- Decided to submit new analogue FE with high DC gain



Coupling in 1.4&1.5: Low rate X-ray measurement

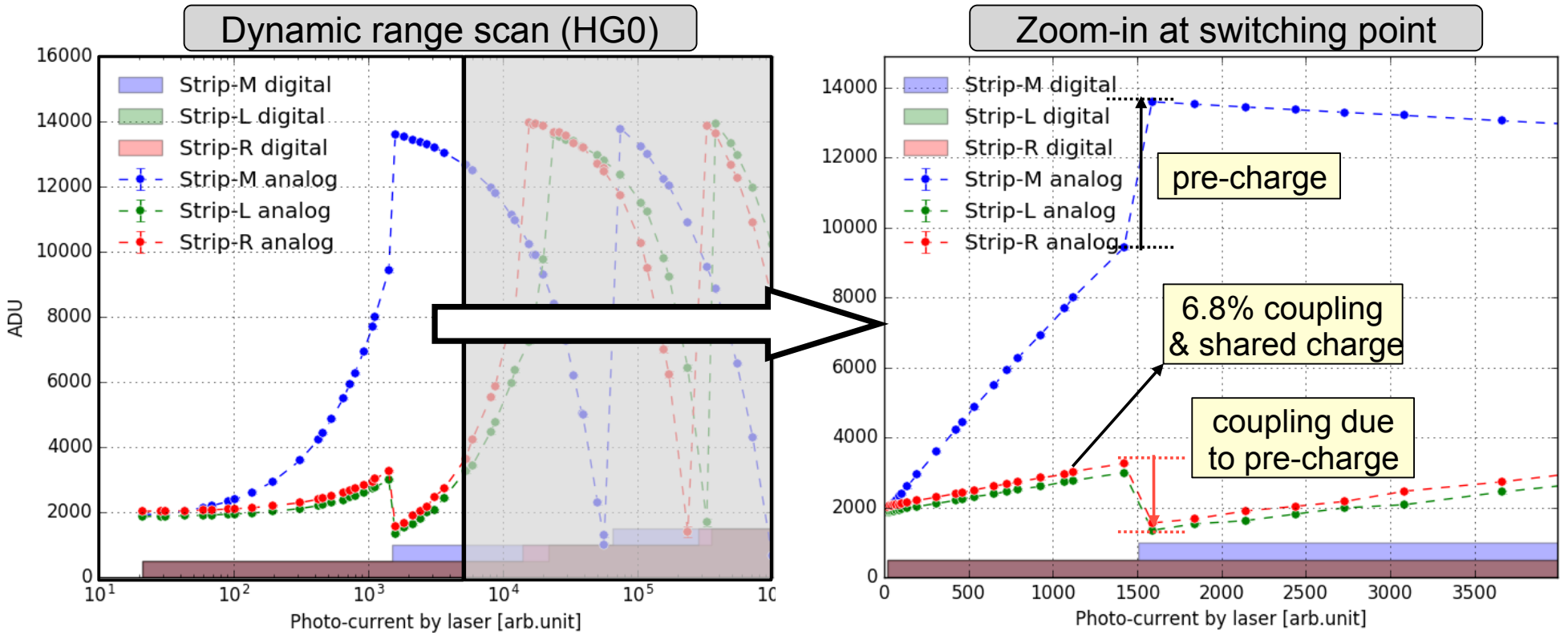
- Low rate X-ray measurement: 0 or 1 ph entry



- Coupling: 6.5% for HG0; 3.9% for G0

Coupling in 1.4&1.5 to neighbouring channels

- Laser injection into a single channel
- Charge in neighbouring strip in high gain: 6.8% coupling
- Charge loss (4.6 photons) in neighbouring strips when channel switches



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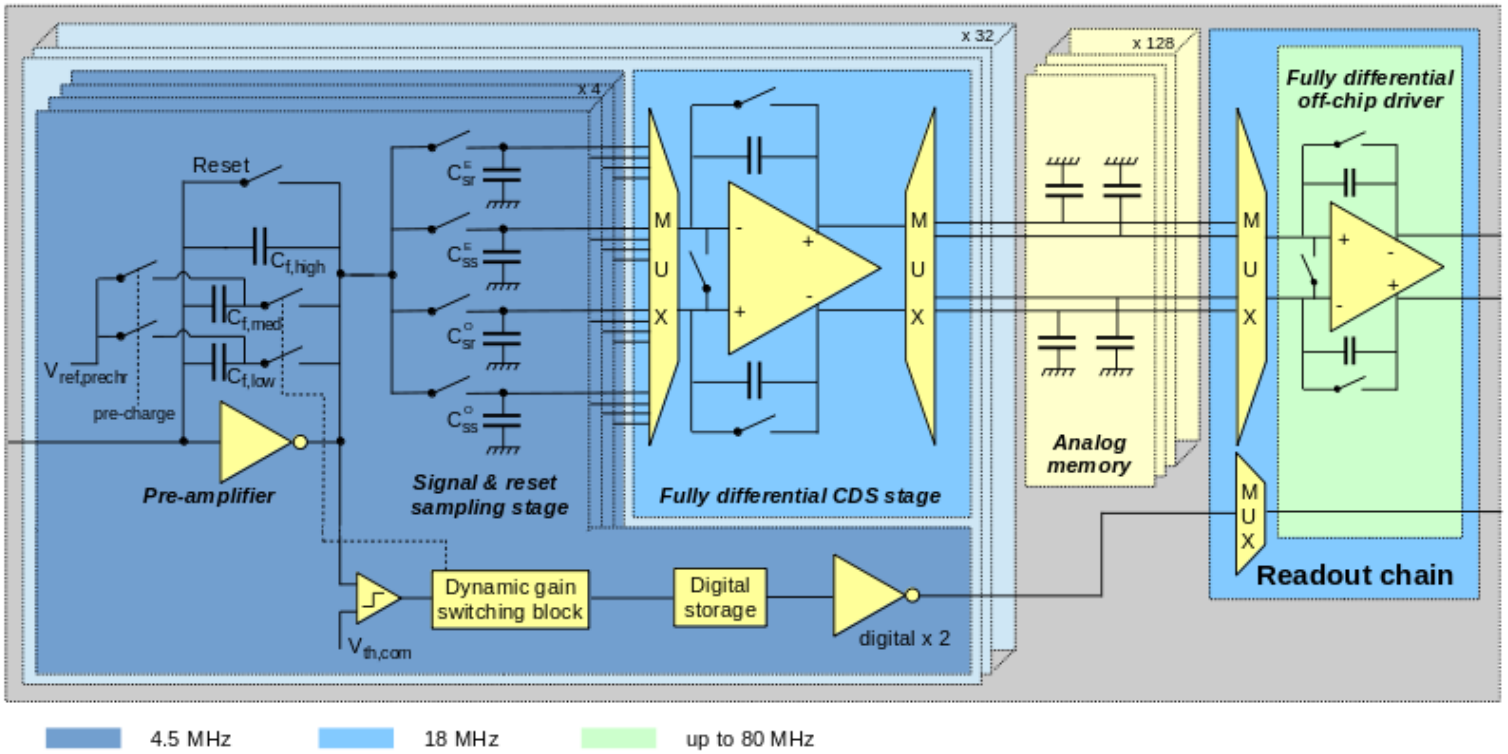
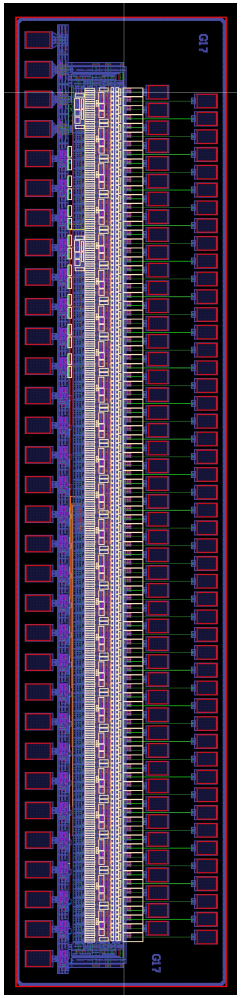
New FE: Gotthard-1.7

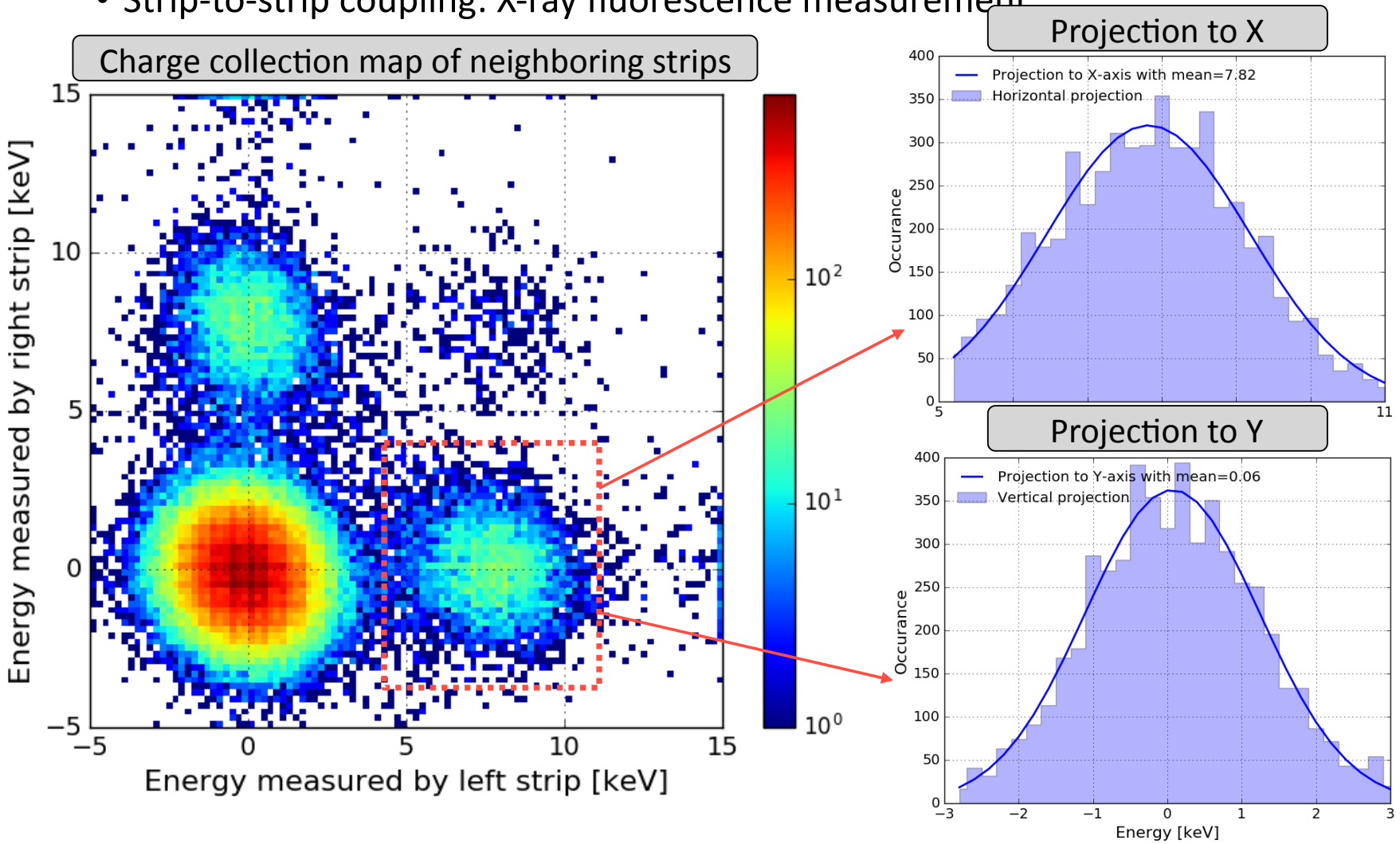
- Development of high DC gain, fully differential front-end G-1.7
  - High DC gain pre-amplifier (750-950 for Vdd=1.2-1.4 V)
  - Continuous CDS sampling at > 18 MHz
  - Differential output fits to ADC





Coupling in Gotthard-1.7

- Strip-to-strip coupling: X-ray fluorescence measurement



- G-1.7: ~ 0.8% (G-1.5: 6.8%)

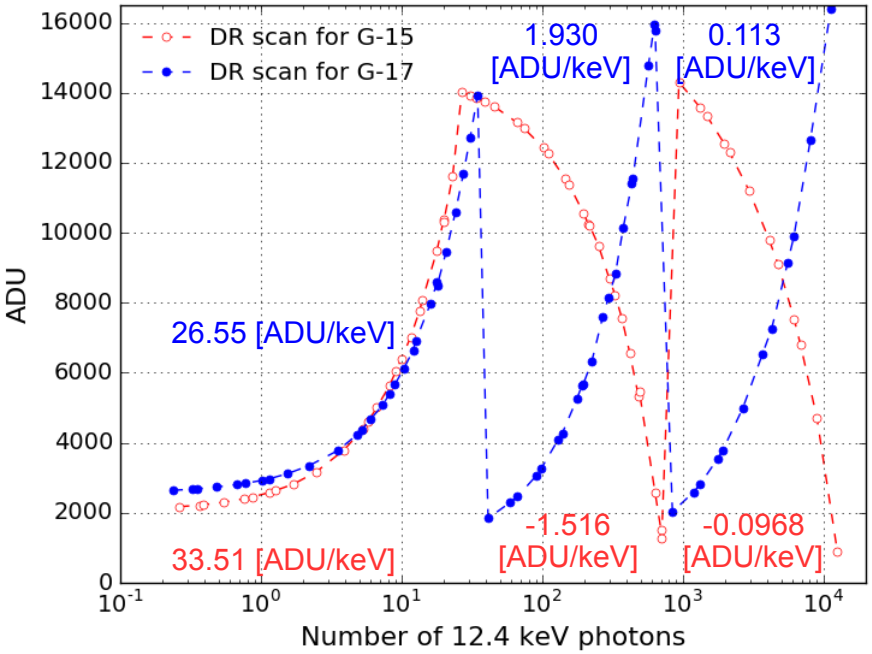
High DC gain reduces strip-to-strip coupling!

$$Coupling = \frac{1}{A} \cdot \frac{C_{int}}{C_f + C_{para}}$$

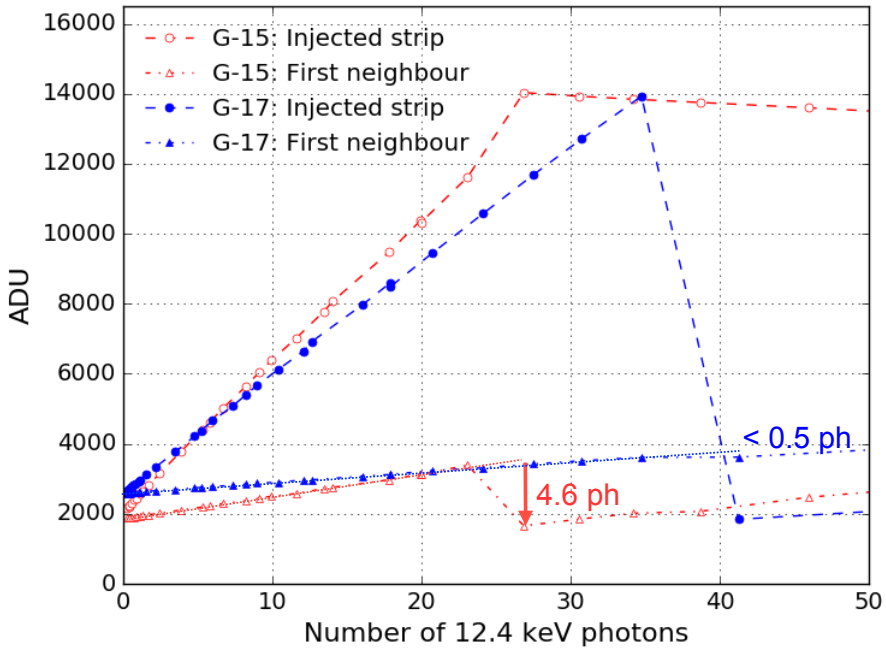
Dynamic range and coupling in G-1.7

- Dynamic range: Infrared laser injection into center of a strip
  - G-1.5: 12570 x 12.4 keV photons, G-1.7: 11260 x 12.4 keV photons

Dynamic range scan with laser



Coupling after gain switching



- "Charge loss" to neighbouring strip after gain switching
  - G-1.5: ~ 4.6 x 12.4 keV photons, G-1.7: ~ 0.47 x 12.4 keV photons

Significant reduction in coupling reduces the complexity of calibration!

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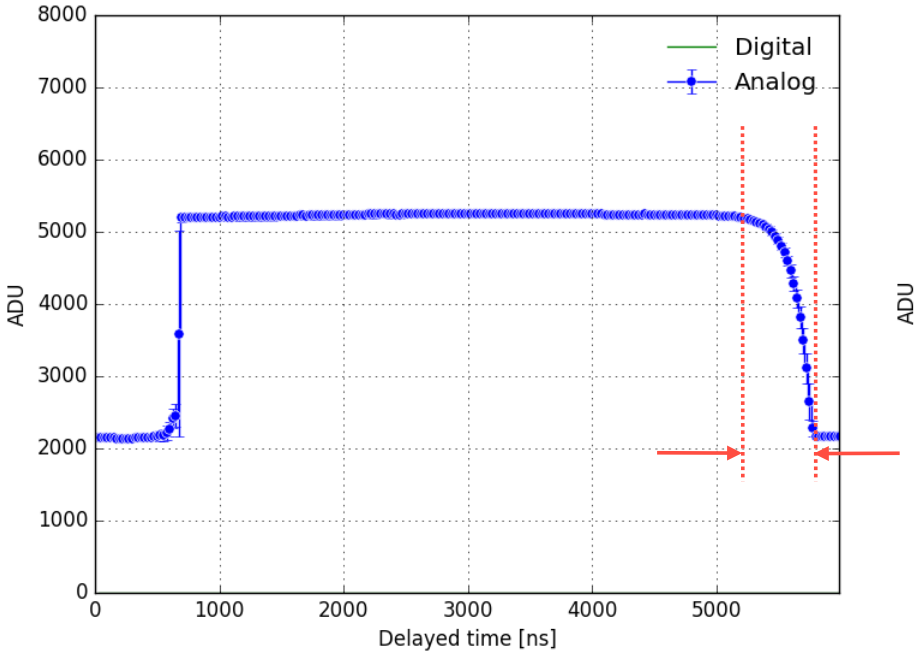
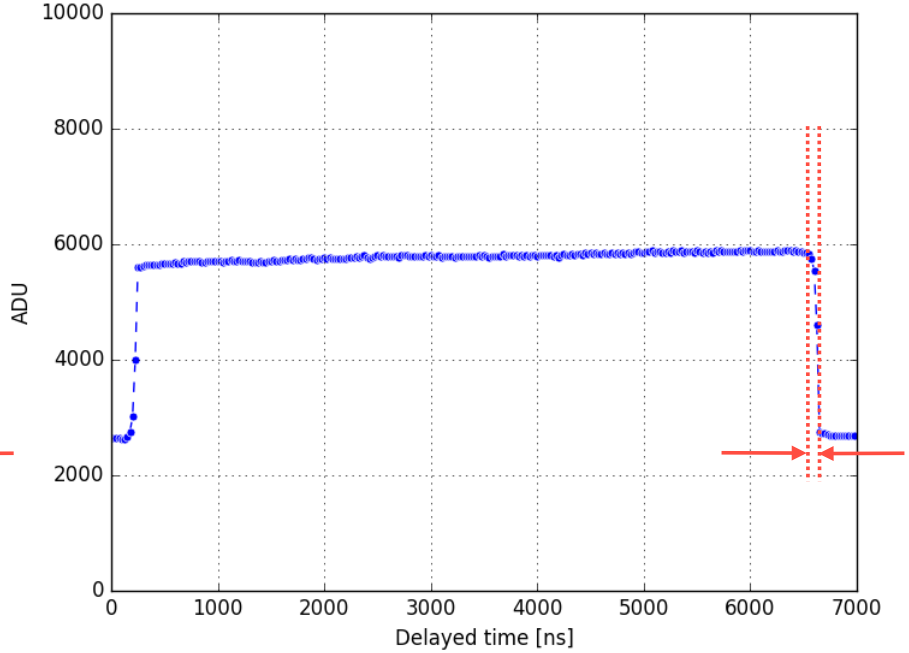
Settling time in Gotthard-1.7

- Settling time: Laser delay scan
  - G-1.5: 500-600 ns → limited by a serial resistor
  - G-1.7: ~ 50-75 ns for signal settling
    - For 100-150 ns integration time, enough time for charge collection

Delay scan for G-1.5



Delay scan for G-1.7



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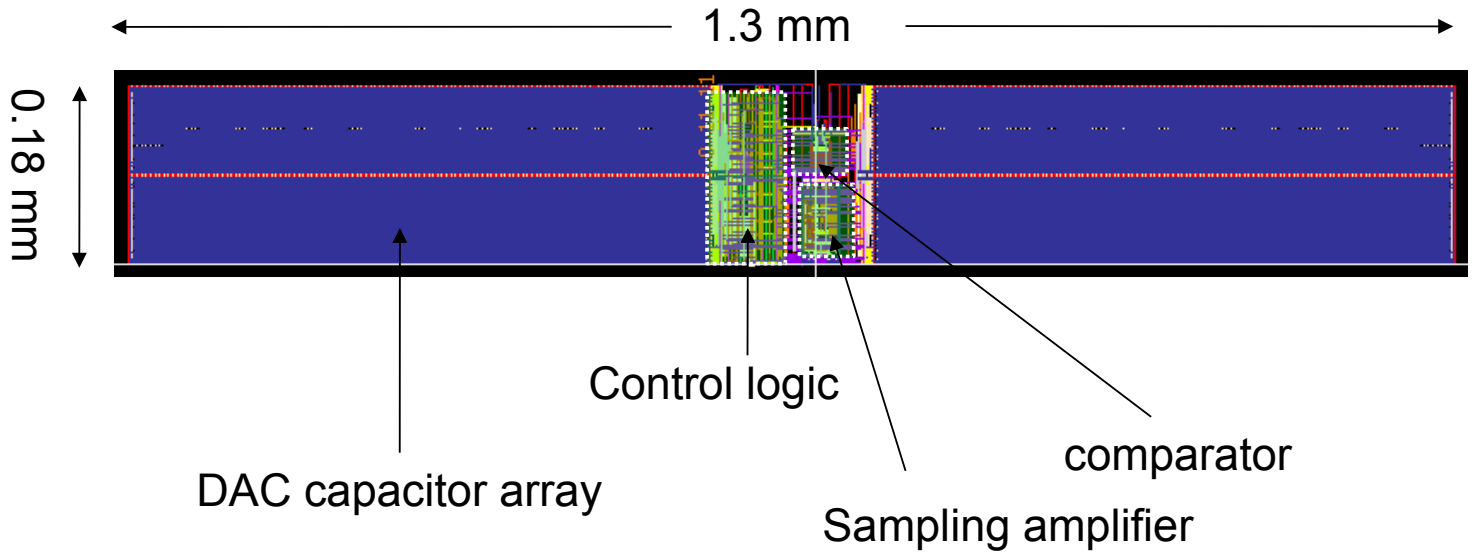
Old ADC design problems



Specification:

- Resolution 12 bit
- Sampling frequency 20 MHz
- Power supply voltage 1.2V
- Input Signal Range ±0.8 V -> 1 LSB = 390 µV

However:

- Sampling frequency was <8MHz, comparator too slow due to parasitics in layout
- Last 4 bits not stable, problem with comparator ready signal

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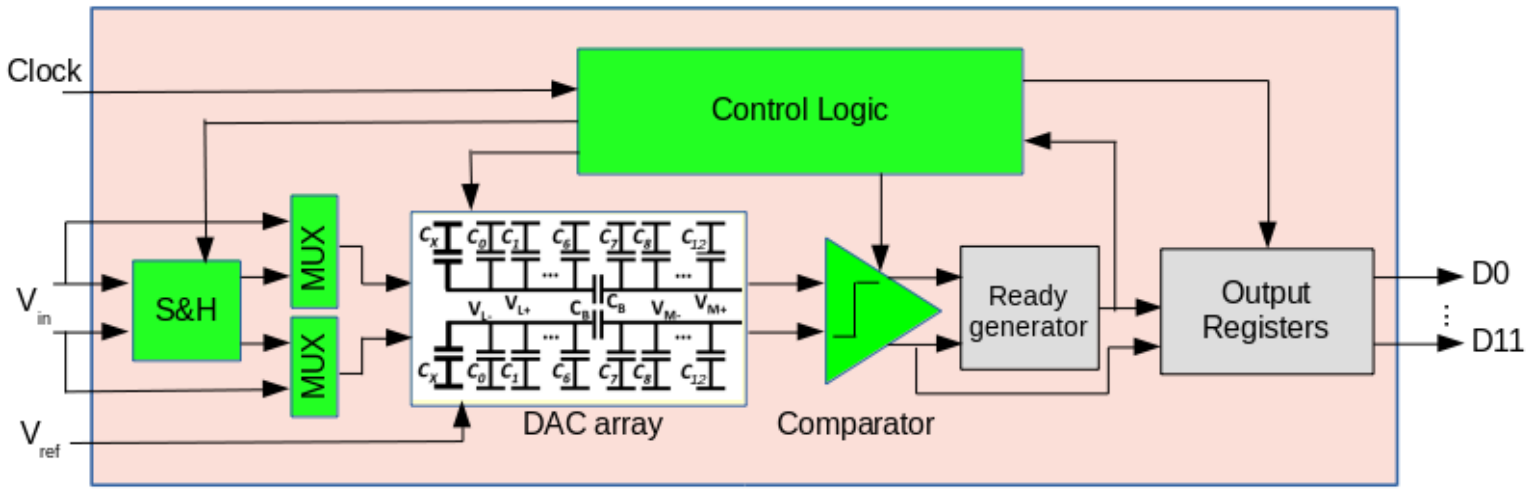
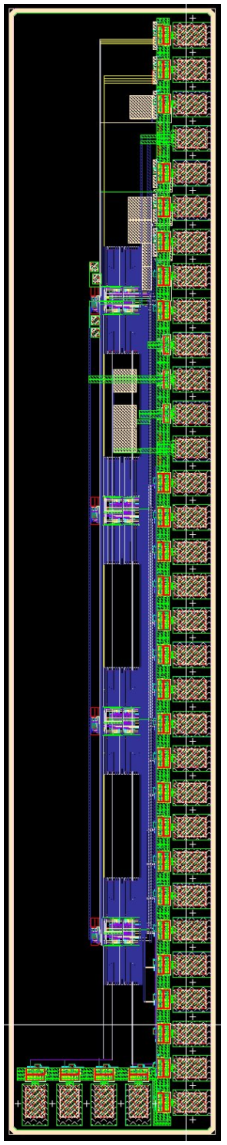
New ADC-0.2 12-bit

- Speed of comparator: > 20 MHz sampling rate (one ADC for 4 channels)
- Split-capacitor DAC array → total capacitance and charging time ↓
- Adjustable delay in control logic for DAC & comparator synchronization
- Area of 180 x 520 µm^2 per ADC (old ADC 180 x 1300 µm^2)

Schematic of ADC-0.2





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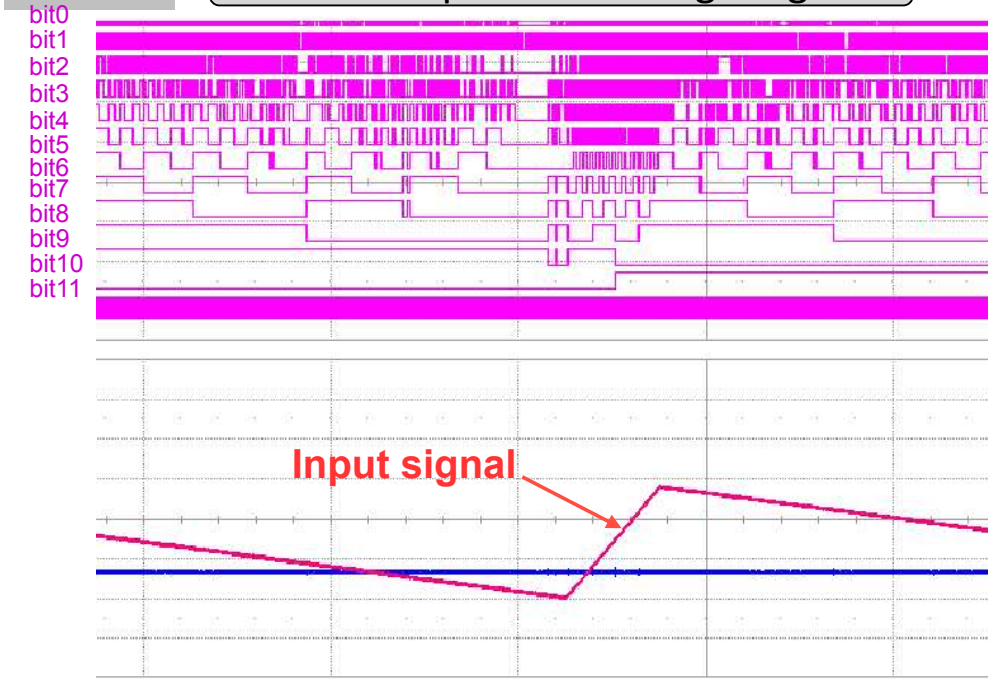
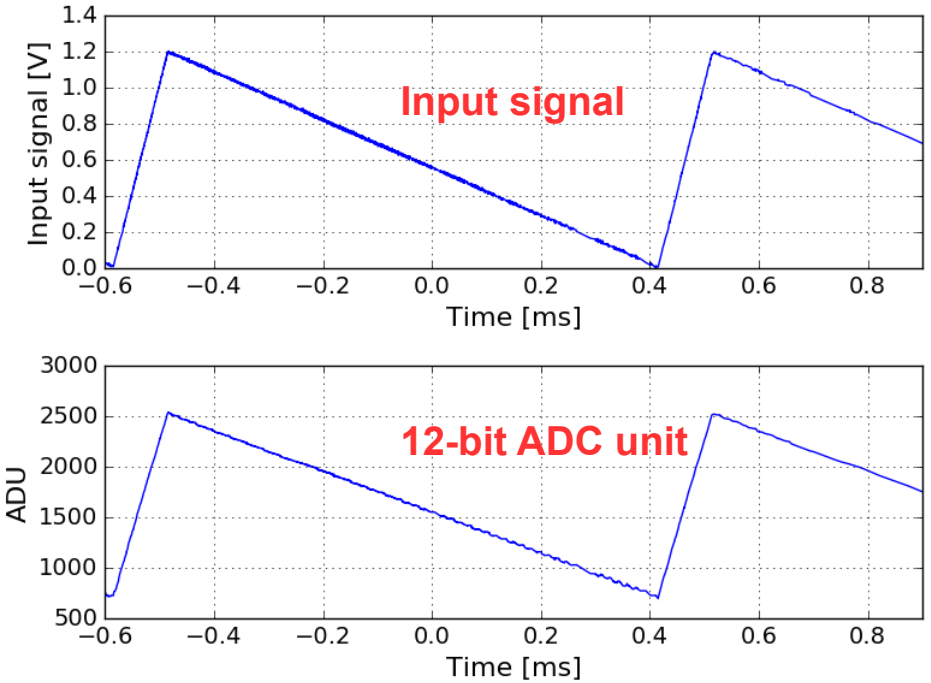
Very first test of ADC-0.2

- ADC 12-bit output
  - 20 MHz ADC clock used
  - Triangle analogue waveform (0 V – 1.2 V) with1 kHz as input

12-bit output for a triangle signal



ADC unit vs. input signal



- Basic functionality of ADC-0.2 demonstrated
- Further tests necessary on: noise, linearity, missing codes, etc.

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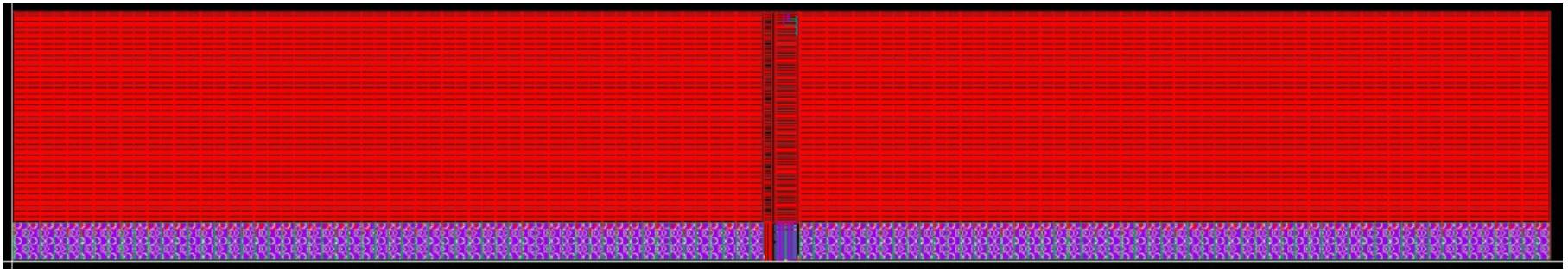
Progress with memory

- Implemented SRAM in ASIC (both schematic and layout, LVS and DRC work)
  - 14 bit per channel: 2 gain bit + 12 bit from ADC for analogue value
  - 1 SRAM unit for 8 channels x 14 bit/channel = 112 bit width
  - 2700 x 112 SRAM unit
  - Area of 380 x 2350 μm^2 per SRAM unit

SRAM layout for 8 channels



- On-going work:
  - Design of the timing and control logic between ADC and memory is in progress

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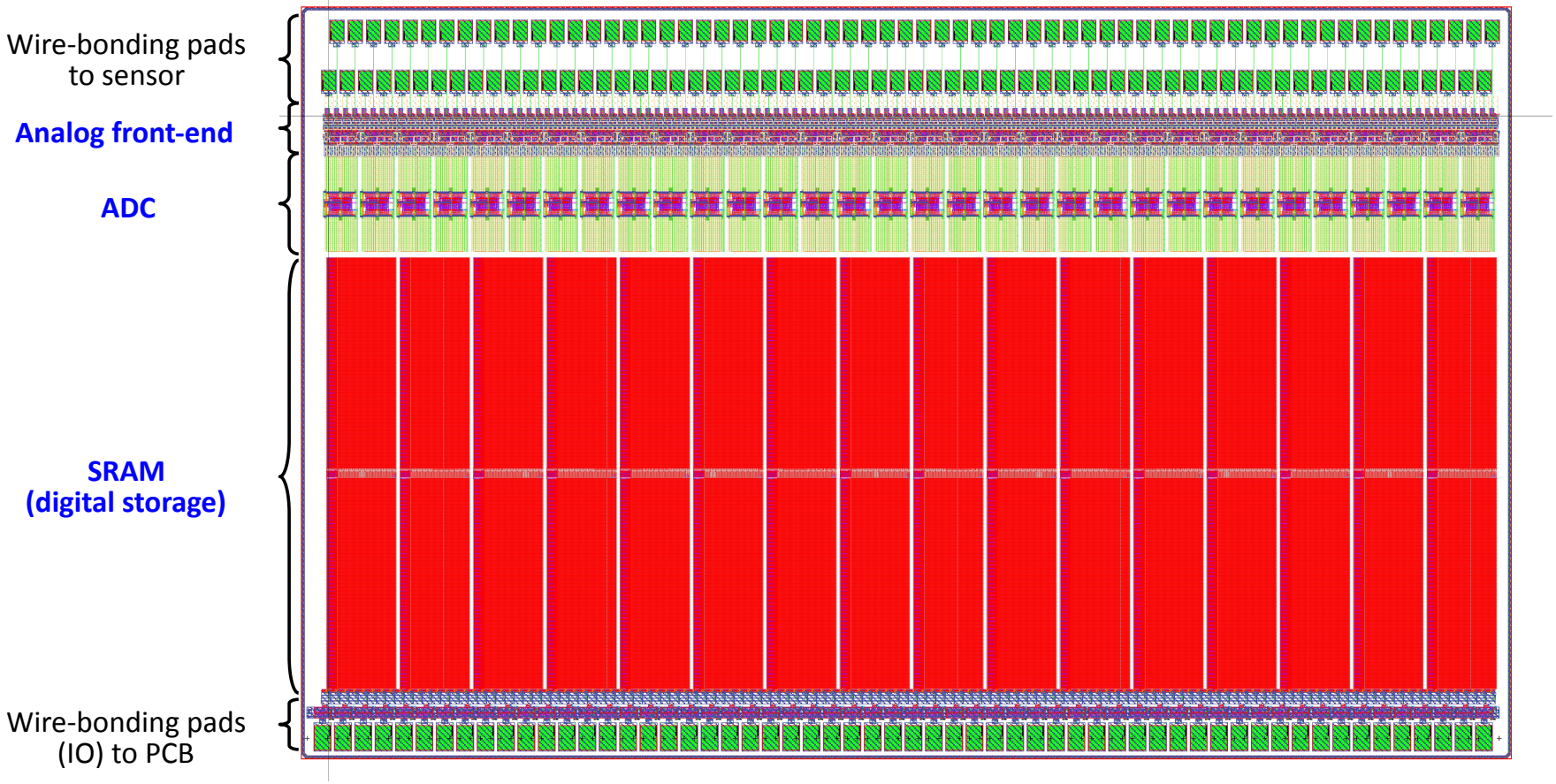
Towards the full scale chip

- Realize the timing and control logic between ADC and SRAM in ASIC
- Integration of analog front-end, ADC and SRAM into a prototype
- Submission of prototype end Feb./early March

Prototype layout



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Summary

- New analogue FE and ADC testing started
  - Looks very promising, full characterisation needs more time
- Next MPW submission in February
  - Full chain: FE, ADC memory
- Engineering run second half 17
- Are on a good way to have first modules end 17/early 18