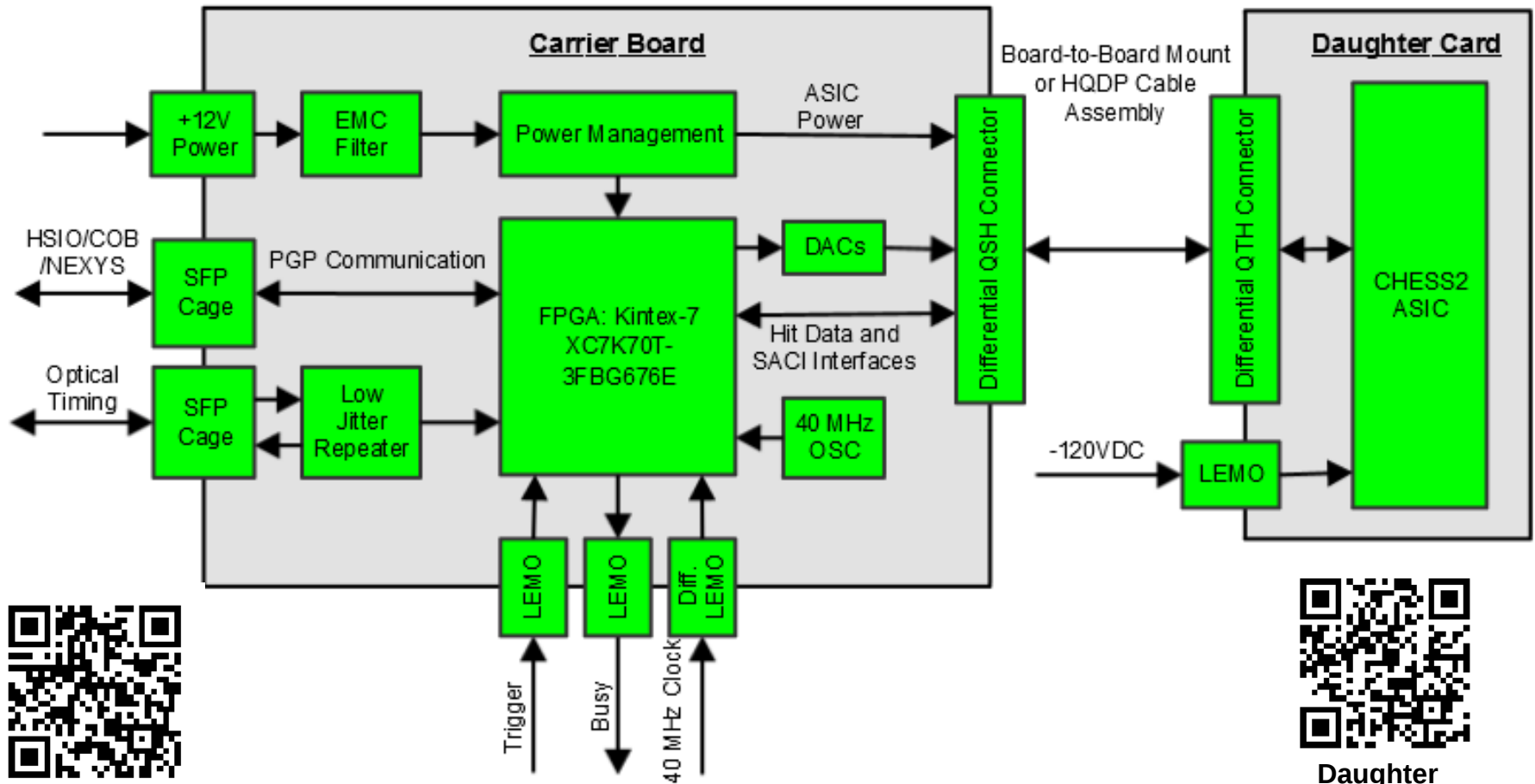


CHES2 DEV Board: Status Report

Larry Ruckman

19 June 2016

System Block Diagram (NEW)

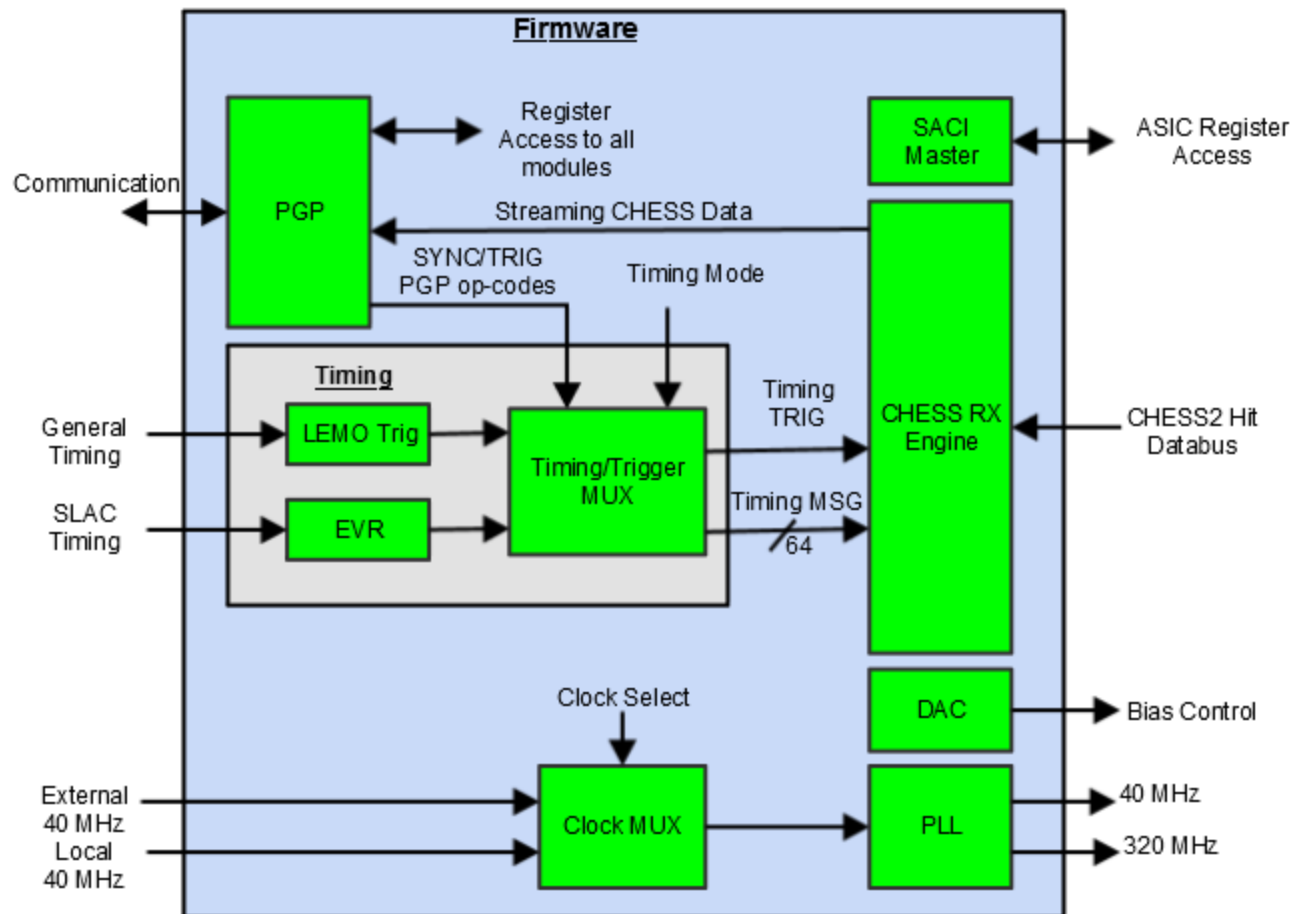


Carrier Board Schematics



Daughter Board Schematics

Base Firmware Block Diagram (NEW)



- Hardware:
 - Daughter Card:
 - Back into Schematics Design Review
 - ASIC pinout documentation has still been changing since last Friday.
 - Starting the layout this week
 - Carrier Card:
 - Schematic Design Review: Completed
 - Waiting for the daughter card layout
- Firmware:
 - Based on carrier card design review:
 - Simplified the timing interface
 - Remove FMC connector
 - All communication through SFP interface
- Software plan:
 - No Updates

Backup Slides



CHES 2 Test Readout Requirements

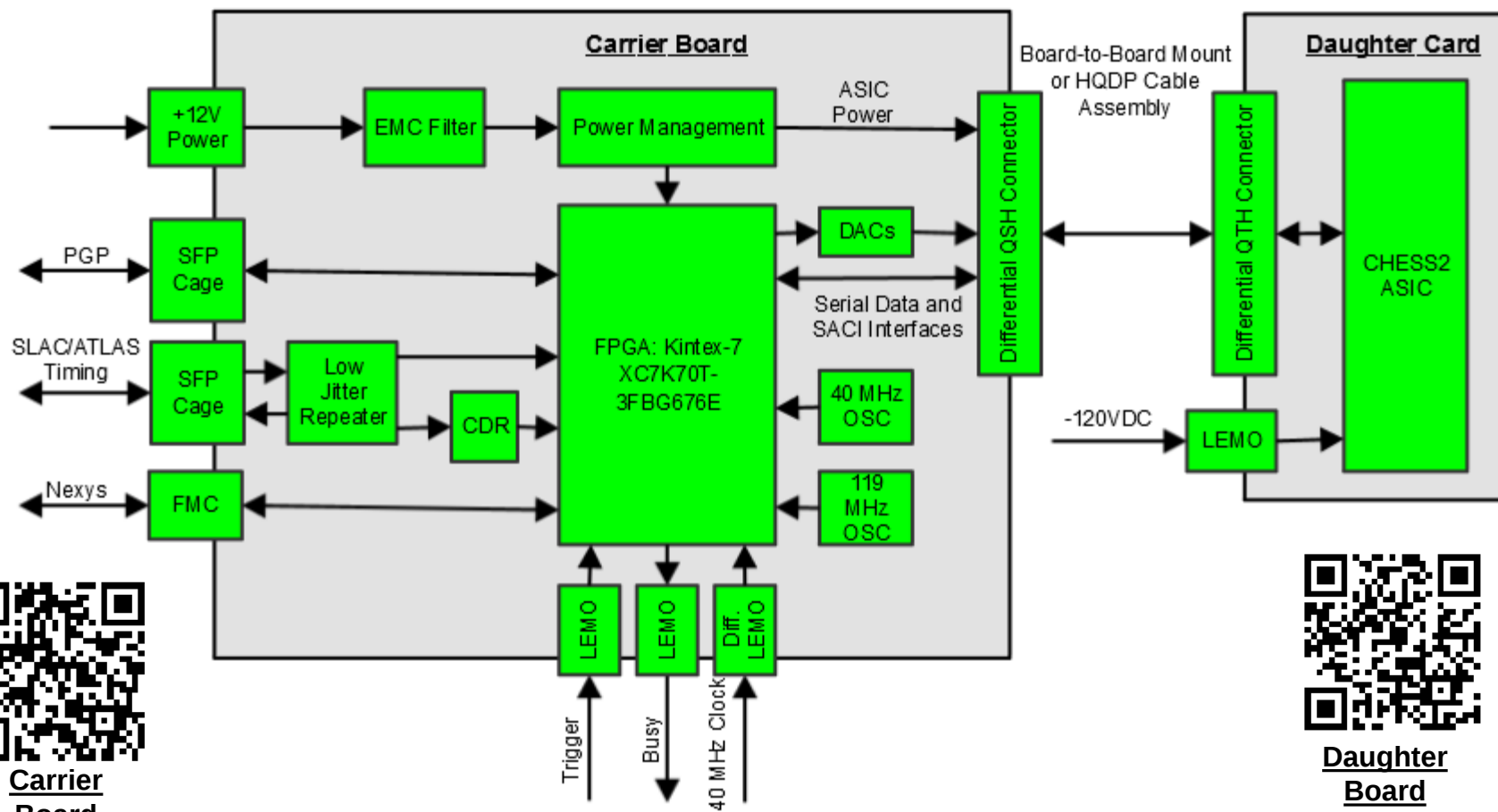
- Support full 3+1, Pair only, 1+Test chip configurations
- Detachable passive daughter card for irradiation
- Flexible connection scheme to support edge TCT, test beam setups (in particular cold daughter board regime)
- Convenient HV and LV powering scheme
- Flexible timing control for multi-chip operation
- Generic control/data interface for compatibility with main backend readout schemes of RCE and NEXYS video
- Ideally, also allow easy extension to ABCN', HCC* and GBT emulation.

- Continue the successful Daughter+Motherboard (carrier) scheme as CHESS-1, with additional considerations:
 - Support full 3+1, and partial Pair or 1+test config
 - Daughter->Motherboard direct connection or short flex cable (especially for test beam with cold box)
 - More attention for cooling access on daughter board
- Data volume from full 3+1 is significant and better dealt with on Motherboard with a Kintex FPGA: *beneficial for flexibility to incorporate ABCN', HCC*, GBT emulation ?*
- Interface to backend readout with just one SFP fiber link should be the most flexible generic form for evolution.

Mother Board Design Requirements

- Low Cost:
 - Want: < \$1k
 - Need: < \$2k
 - Not including optics, ASICs, cabling
- LV powering to generate all voltages from input 12V
- Support multiple timing system (SLAC, ATLAS, etc)
- Initial baseline 3.125 Gbps PGP Backend Communication
 - Native to RCE based HSIO-II/COB
 - Can be adopted to other FPGA cards such as NEXYS
- Must support direct mounting or cabling of the daughter board
- Access to test structure signals: *needs more investigation as best on mother-board or daughter-board ?*

System Block Diagram (OLD)



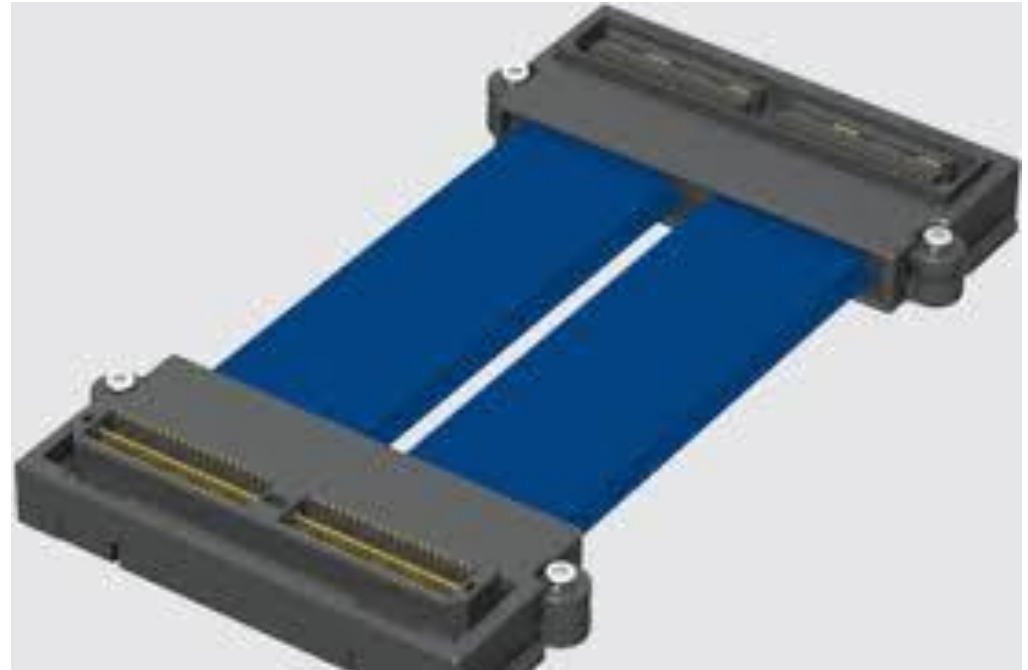
Carrier Board Schematics



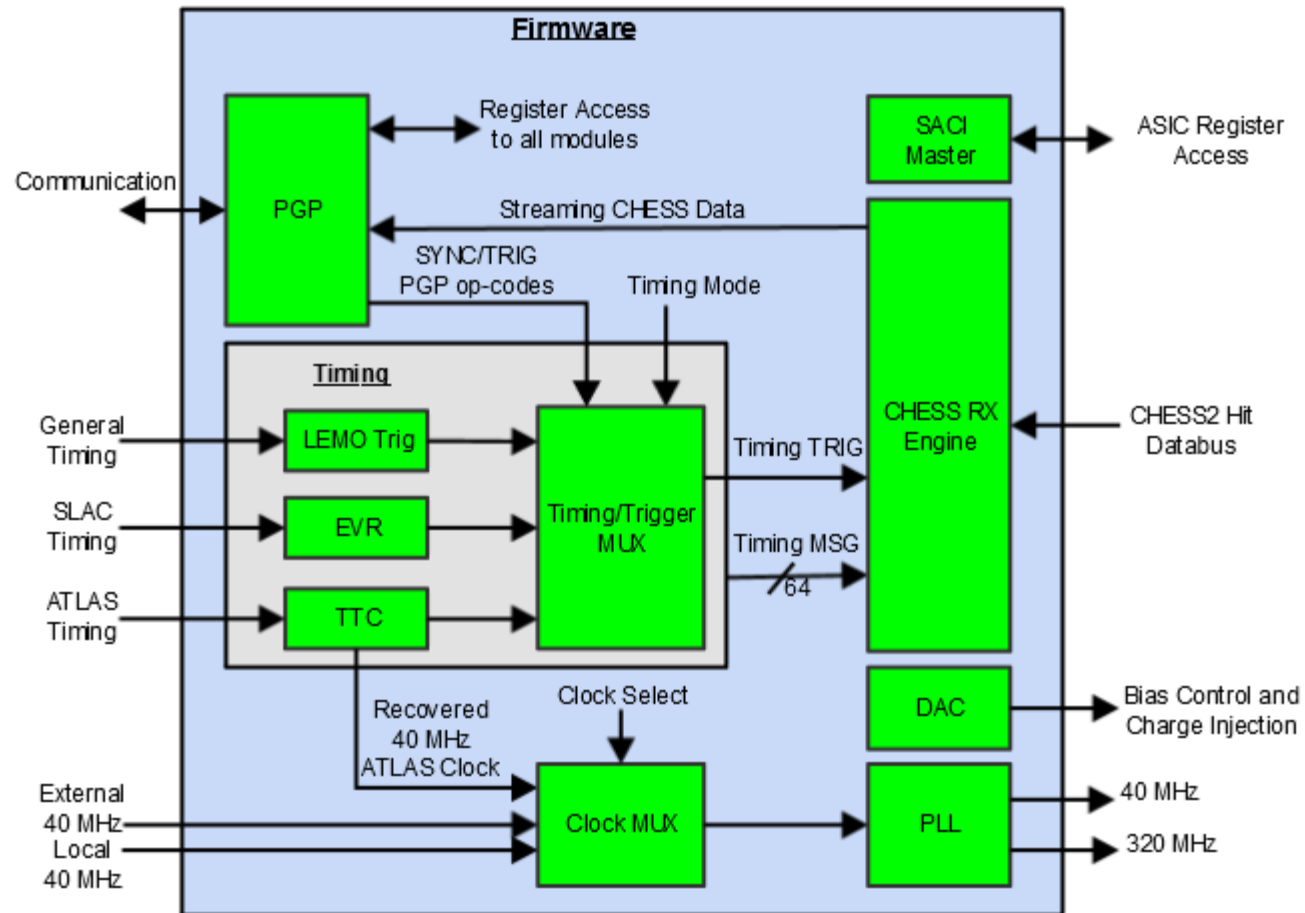
Daughter Board Schematics

Board to Board Connector

- HQDP is a COTS Cable
 - Available from Samtec.com
 - 800 mA per pin
 - 100 Ω Differential
 - 30 AWG twinax micro ribbon
 - Rated for 19.0 Gbps over 0.25m cable
- Custom ordered length
 - Up to 1.0m



Base Firmware Block Diagram (OLD)



Timing Modes (OLD)

1. LEMO Triggering

- TimingMessage:
 - Increments every 320 MHz clock cycle
 - Resets to 0x0 when PGP OP-Code 0xAA detected
- TimingTrig:
 - Same as LEMO trigger input with firmware one-shot deglitching

2. PGP Triggering

- TimingMessage:
 - Increments every 320 MHz clock cycle
 - Resets to 0x0 when PGP OP-Code 0xAA detected
- TimingTrig:
 - Triggered when PGP OP-Code 0x55 detected

3. SLAC Timing/Triggering

- TimingMessage:
 - BIT[31:00] = Ticks
 - BIT[63:32] = Fiducials
- TimingTrig:
 - Triggered on programmable EVR OP-Code

4. ATLAS Timing/Triggering

- TimingMessage:
 - BIT[07:00] = Event Reset Counter
 - BIT[31:08] = Event Counter
 - BIT[39:32] = Bunch Reset Counter
 - BIT[51:40] = Bunch Counter
 - BIT[63:52] = 0x0
- TimingTrig:
 - TTC-RX Trigger

Timing Modes (NEW)

1. LEMO Triggering

- TimingMessage:
 - Increments every 320 MHz clock cycle
 - Resets to 0x0 when PGP OP-Code 0xAA detected
- TimingTrig:
 - Same as LEMO trigger input with firmware one-shot deglitching

2. PGP Triggering

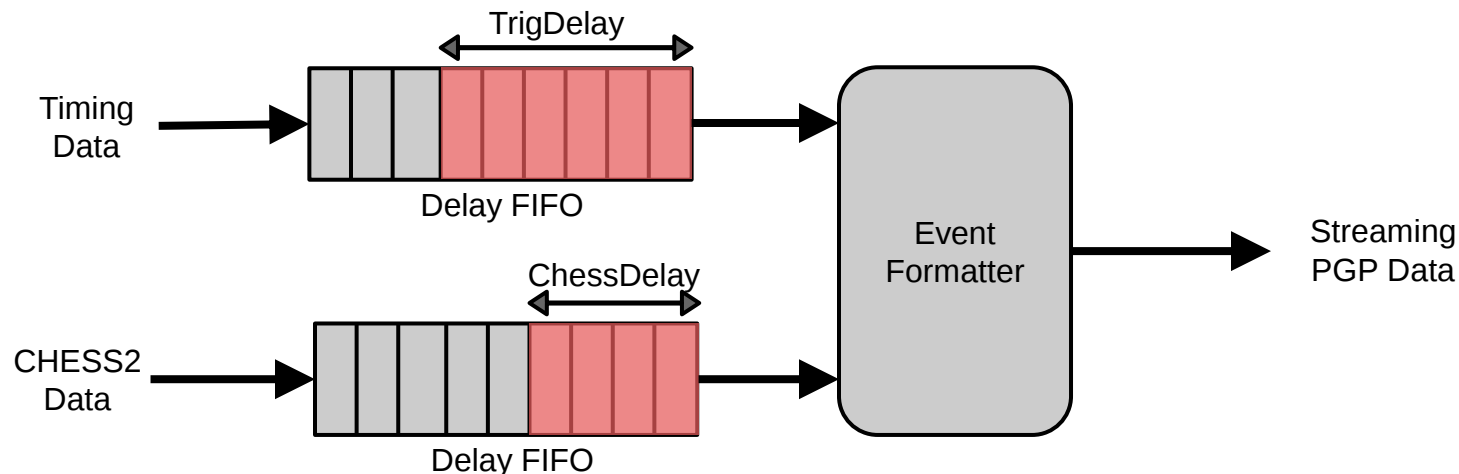
- TimingMessage:
 - Increments every 320 MHz clock cycle
 - Resets to 0x0 when PGP OP-Code 0xAA detected
- TimingTrig:
 - Triggered when PGP OP-Code 0x55 detected

3. SLAC Timing/Triggering

- TimingMessage:
 - BIT[31:00] = Ticks
 - BIT[63:32] = Fiducials
- TimingTrig:
 - Triggered on programmable EVR OP-Code

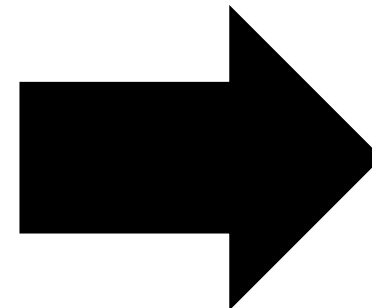
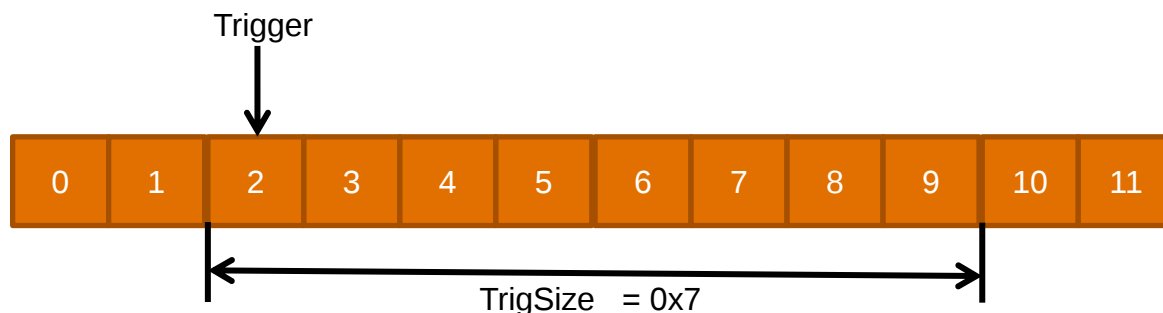
Trigger/Timing Diagram

- Programmable delay FIFOs
 - Up to 12 us delay per delay FIFO module
 - In units of 1/320MHz
- Event Formatter combines the CHESS data and timing data into a streaming data

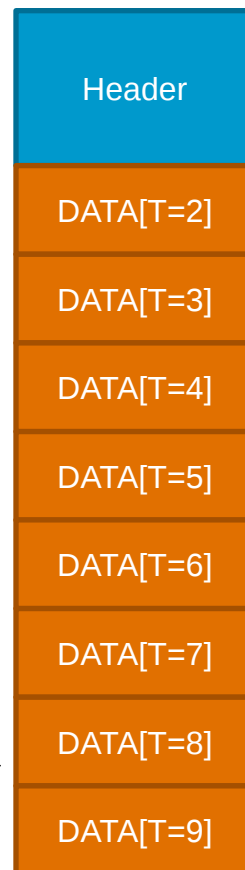


Event Formatter: Readout Sequence

- Waits for trigger
- When triggered
 - Puts the 64-bit timing message into the header
 - Programmable number of CHESS data samples per event frame



Frame Format



Header Word Format

HDR[0]

- BIT[1:0] = Virtual Channel ID
 - Statically set to 0x0
- BIT[7:2] = Destination ID = lane + Z
 - Software programmable
- BIT[31:8] = Transaction ID
 - Increments every packet
- BIT[47:32] = Acquire Counter
 - Increments every timing trigger
- BIT[55:48] = OP Code
 - Software programmable
- BIT[59:56] = Element ID
 - Statically set to 0x0
- BIT[63:60] = Destination ID = Z only
 - Software programmable

• HDR[1]

- BIT[31:0] = Frame Number
 - Increments every packet
- BIT[63:32] = Ticks
 - Lower 32-bits of timing message

• HDR[2]

- BIT[31:0] = Fiducials
 - Upper 32-bits of timing message
- BIT[47:32] = sbtemp[0]
 - Statically set to 0x0
- BIT[63:48] = sbtemp[1]
 - Statically set to 0x0

• HDR[3]

- BIT[15:0] = sbtemp[2]
 - Statically set to 0x0
- BIT[31:16] = sbtemp[3]
 - Statically set to 0x0
- BIT[63:32] = Frame Type
 - Software programmable

- Header Format Based on existing LCLS PGP header format

Data Word Format

BIT[06:00] = ASIC[0], ROW[6:0]
BIT[11:07] = ASIC[0], COL[4:0]
BIT[12:12] = ASIC[0], Multi-Hit Flag
BIT[13:13] = ASIC[0], Data Valid Flag
BIT[15:14] = 0x0
BIT[22:16] = ASIC[1], ROW[6:0]
BIT[27:23] = ASIC[1], COL[4:0]
BIT[28:28] = ASIC[1], Multi-Hit Flag
BIT[29:29] = ASIC[1], Data Valid Flag
BIT[31:30] = 0x0
BIT[38:32] = ASIC[2], ROW[6:0]
BIT[43:39] = ASIC[2], COL[4:0]
BIT[44:44] = ASIC[2], Multi-Hit Flag
BIT[45:45] = ASIC[2], Data Valid Flag
BIT[63:46] = 0x0