CHESS2 DEV Board:
Status Report

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U.S. DEPARTMENT OF ENERGY
Office of Science

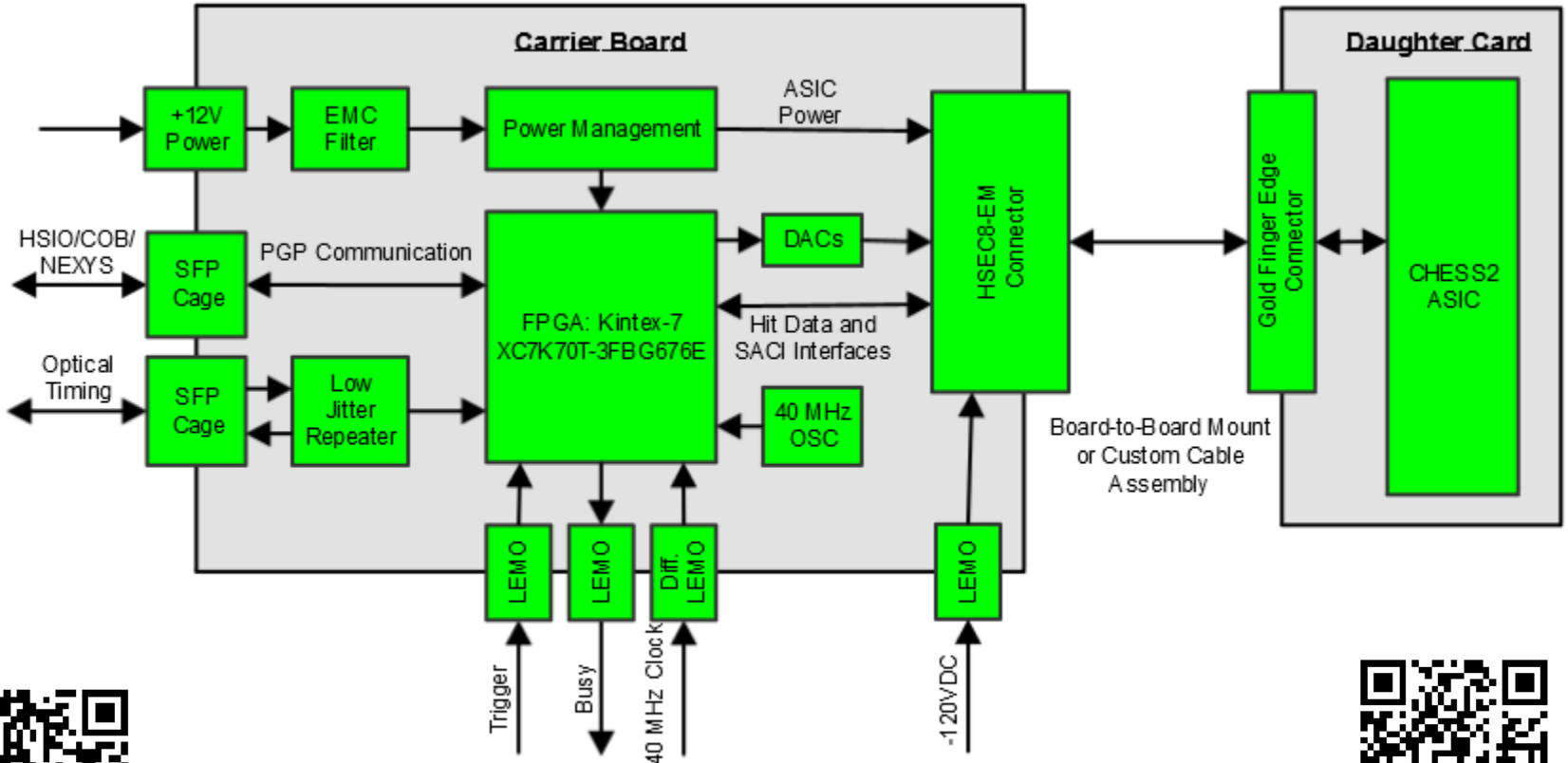
SLAC NATIONAL ACCELERATOR LABORATORY

Status

- Hardware:
  - Daughter Card:
    - Layout on hold
    - Still finalizing requirements
  - Carrier Card:
    - Layout on hold
    - Still finalizing requirements
- Firmware:
  - No Updates
- Software plan:
  - No Updates

Backup Slides

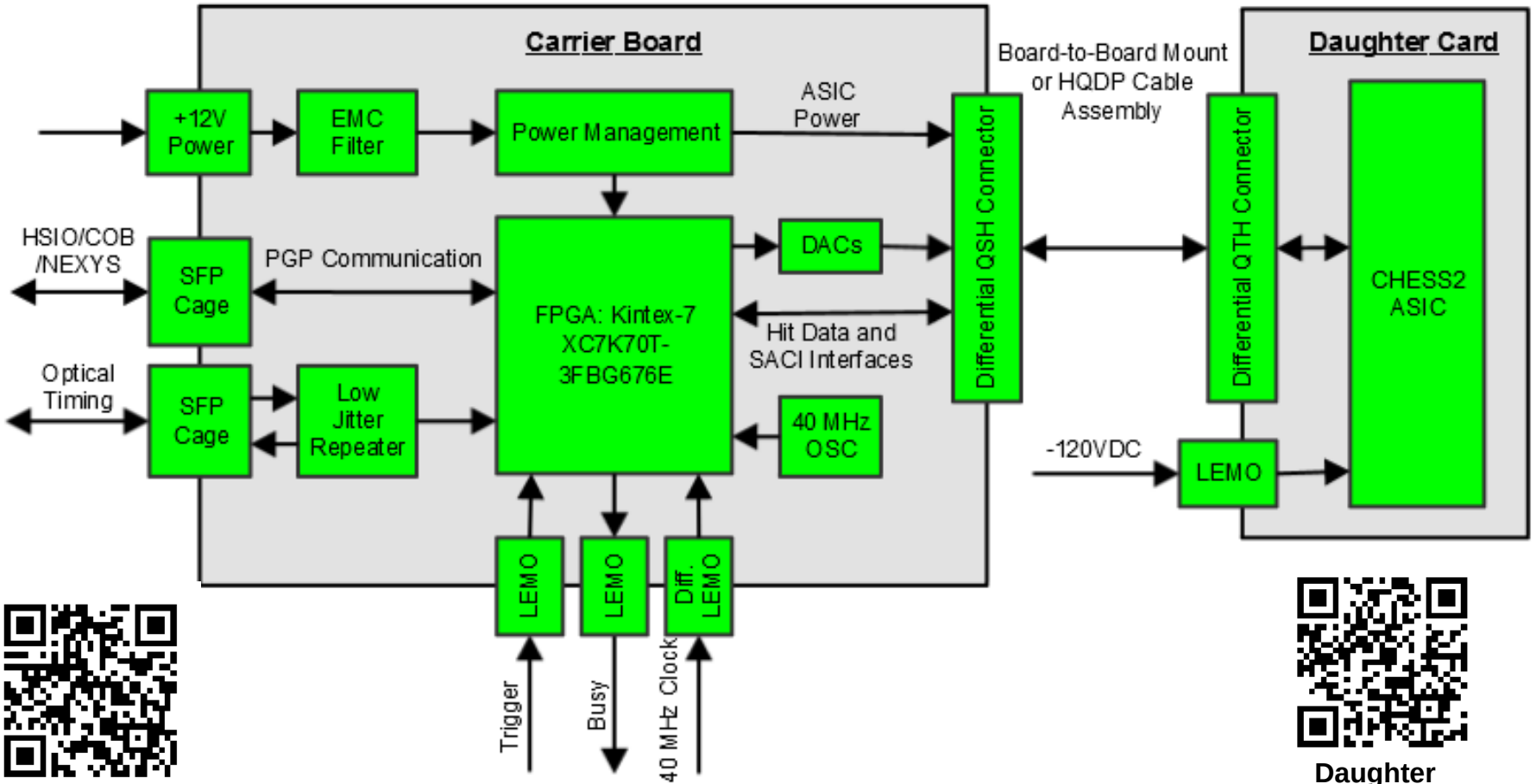
System Block Diagram (NEW)



Carrier Board Schematics

Daughter Board Schematics

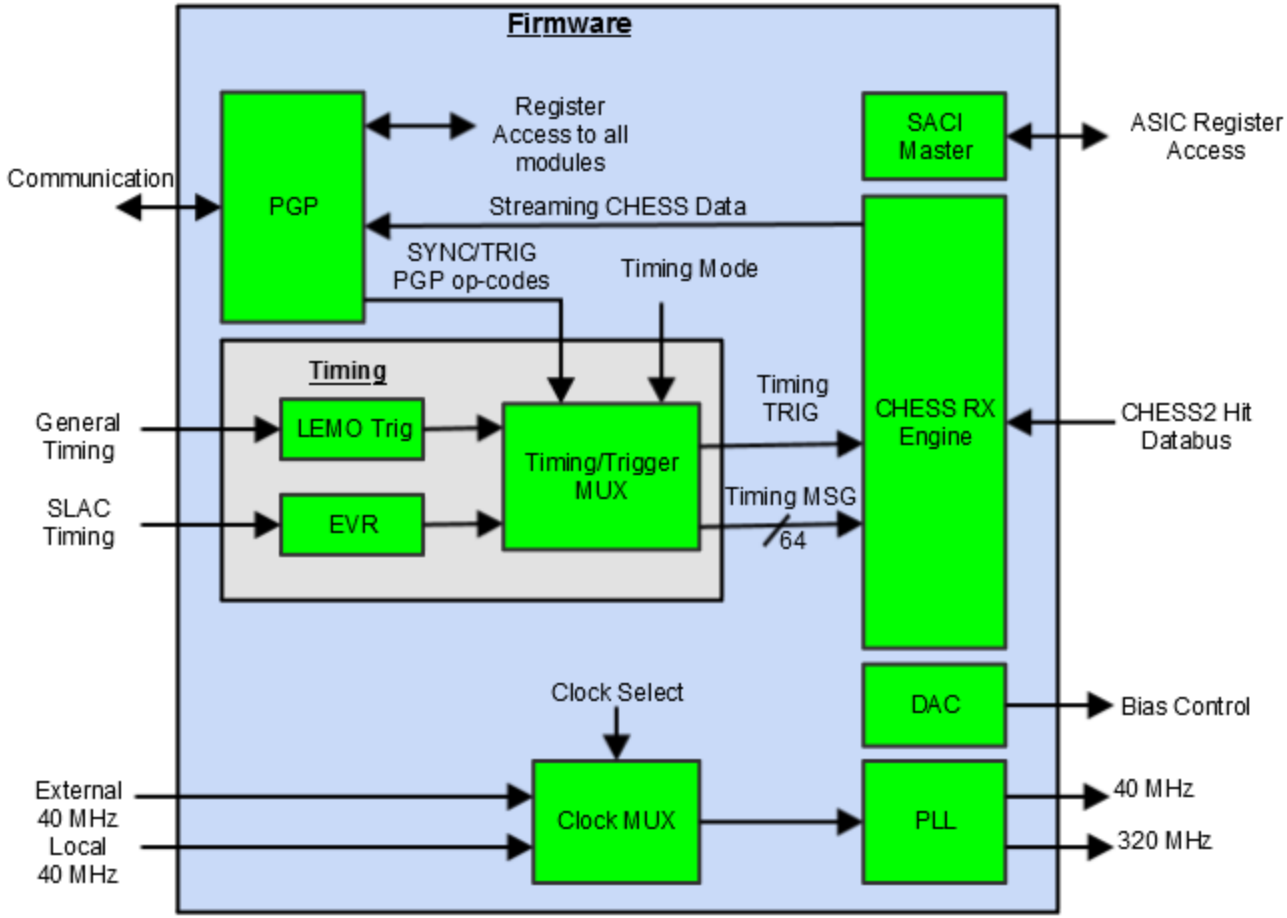
System Block Diagram (OLD)



Carrier Board Schematics

Daughter Board Schematics

Base Firmware Block Diagram

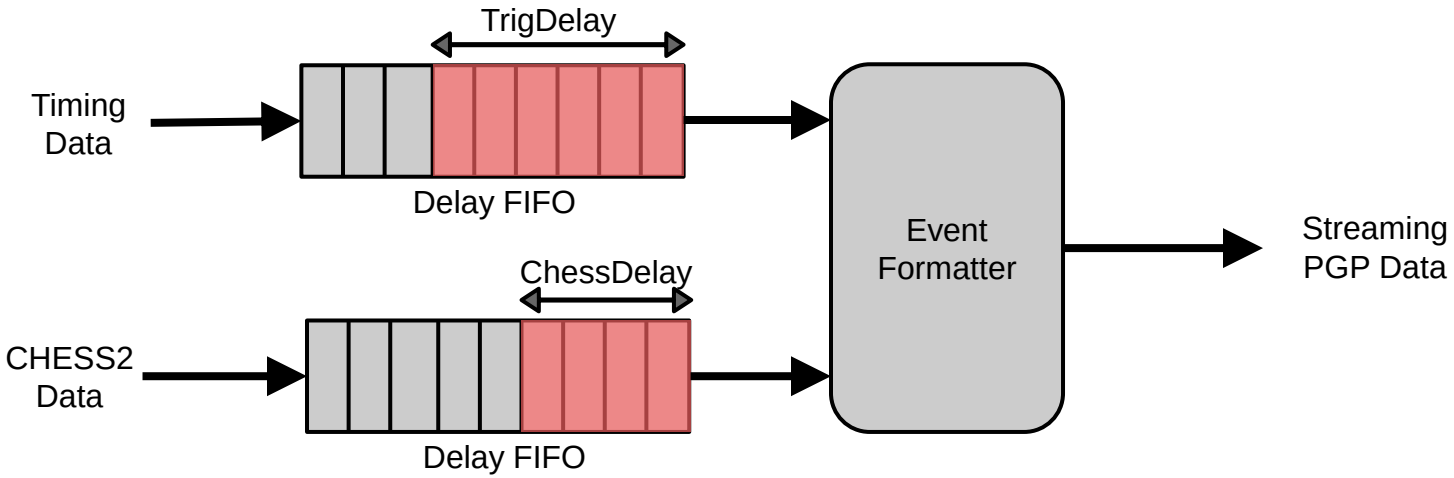


Timing Modes

1. LEMO Triggering
   - TimingMessage:
     - Increments every 320 MHz clock cycle
     - Resets to 0x0 when PGP OP-Code 0xAA detected
   - TimingTrig:
     - Same as LEMO trigger input with firmware one-shot deglitching
2. PGP Triggering
   - TimingMessage:
     - Increments every 320 MHz clock cycle
     - Resets to 0x0 when PGP OP-Code 0xAA detected
   - TimingTrig:
     - Triggered when PGP OP-Code 0x55 detected
3. SLAC Timing/Triggering
   - TimingMessage:
     - BIT[31:00] = Ticks
     - BIT[63:32] = Fiducials
   - TimingTrig:
     - Triggered on programmable EVR OP-Code

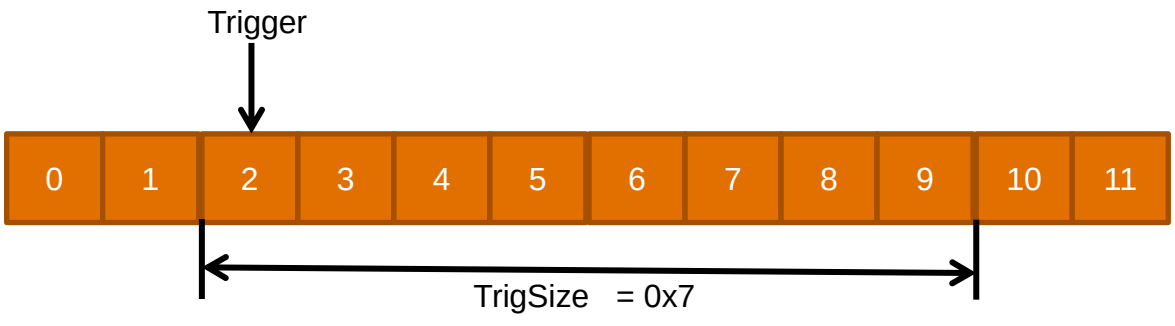
Trigger/Timing Diagram

- Programmable delay FIFOs
  - Up to 12 us delay per delay FIFO module
  - In units of 1/320MHz
- Event Formatter combines the CHESS data and timing data into a streaming data

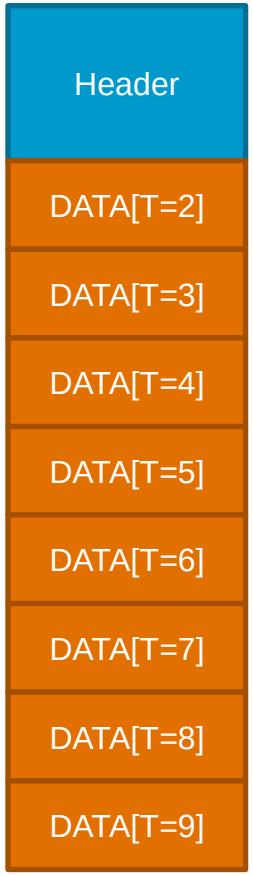


Event Formatter: Readout Sequence

- Waits for trigger
- When triggered
  - Puts the 64-bit timing message into the header
  - Programmable number of CHESS data samples per event frame



Frame Format



Header Word Format

HDR[0]

- BIT[1:0] = Virtual Channel ID
  - Statically set to 0x0
- BIT[7:2] = Destination ID = lane + Z
  - Software programmable
- BIT[31:8] = Transaction ID
  - Increments every packet
- BIT[47:32] = Acquire Counter
  - Increments every timing trigger
- BIT[55:48] = OP Code
  - Software programmable
- BIT[59:56] = Element ID
  - Statically set to 0x0
- BIT[63:60] = Destination ID = Z only
  - Software programmable

- HDR[1]
  - BIT[31:0] = Frame Number
    - Increments every packet
  - BIT[63:32] = Ticks
    - Lower 32-bits of timing message
- HDR[2]
  - BIT[31:0] = Fiducials
    - Upper 32-bits of timing message
  - BIT[47:32] = sbtemp[0]
    - Statically set to 0x0
  - BIT[63:48] = sbtemp[1]
    - Statically set to 0x0
- HDR[3]
  - BIT[15:0] = sbtemp[2]
    - Statically set to 0x0
  - BIT[31:16] = sbtemp[3]
    - Statically set to 0x0
  - BIT[63:32] = Frame Type
    - Software programmable

- Header Format Based on existing LCLS PGP header format

Data Word Format

BIT[06:00] = ASIC[0], ROW[6:0]
BIT[11:07] = ASIC[0], COL[4:0]
BIT[12:12] = ASIC[0], Multi-Hit Flag
BIT[13:13] = ASIC[0], Data Valid Flag
BIT[15:14] = 0x0
BIT[22:16] = ASIC[1], ROW[6:0]
BIT[27:23] = ASIC[1], COL[4:0]
BIT[28:28] = ASIC[1], Multi-Hit Flag
BIT[29:29] = ASIC[1], Data Valid Flag
BIT[31:30] = 0x0
BIT[38:32] = ASIC[2], ROW[6:0]
BIT[43:39] = ASIC[2], COL[4:0]
BIT[44:44] = ASIC[2], Multi-Hit Flag
BIT[45:45] = ASIC[2], Data Valid Flag
BIT[63:46] = 0x0