LHC Detector Upgrades

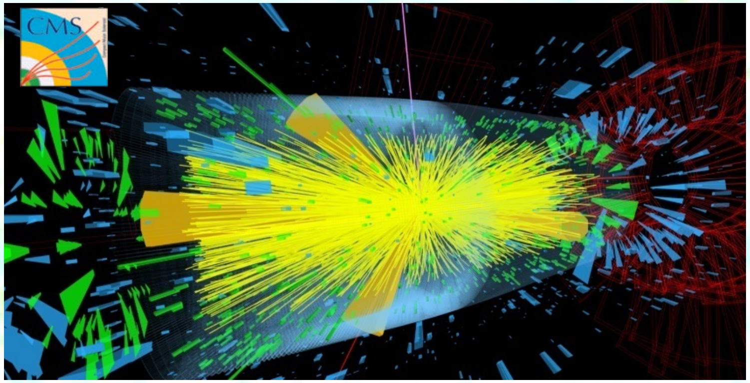
High Luminosity LHC

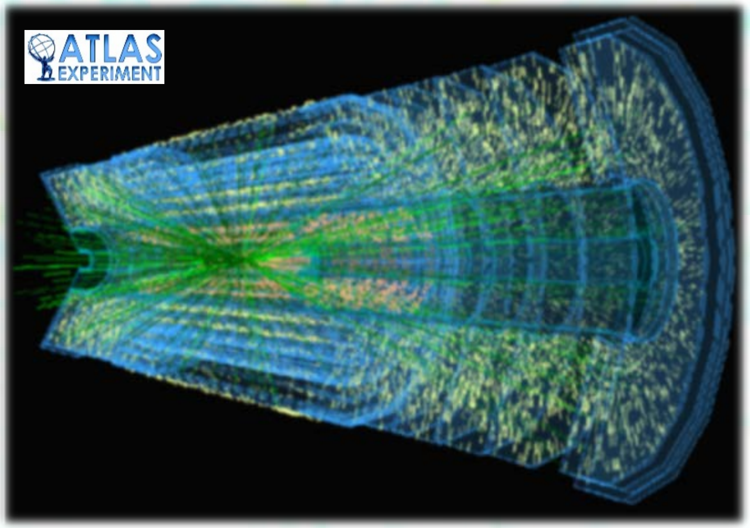
UNIVERSITY OF BIRMINGHAM

10th Annual Meeting of the Helmholtz Alliance "Physics at the Terascale"

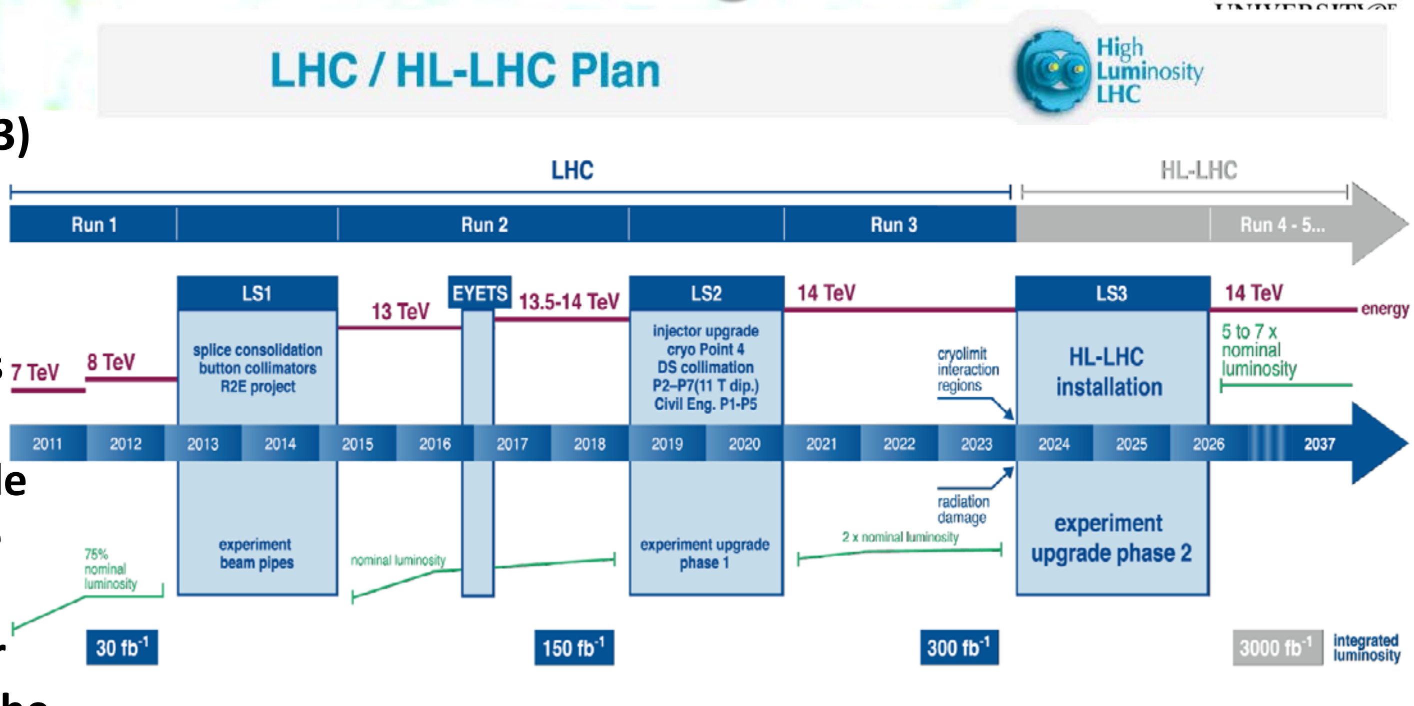
Phil Allport

- **Overview of HL-LHC Programme**
- **Tracking Technologies**
  - **Silicon Detectors**
    - **ATLAS, CMS, LHCb, ALICE**
  - **Gaseous Detectors**
    - **Muon Spectrometers, ALICE TPC**
  - **Scintillating Fibre**
    - **LHCb**
- **Calorimeter Upgrades**
  - **Electromagnetic**
  - **Hadron**
- **Fast Timing Detectors and Particle Identification**
- **Read-out and Triggering**
- **Conclusions**





Overview of HL-LHC Programme



CERN Council (May 2013)
"The discovery of the Higgs boson is the start of a major programme of work to measure this particle's properties with the highest possible precision for testing the validity of the Standard Model and to search for further new physics at the energy frontier. The LHC is in a unique position to pursue this programme."

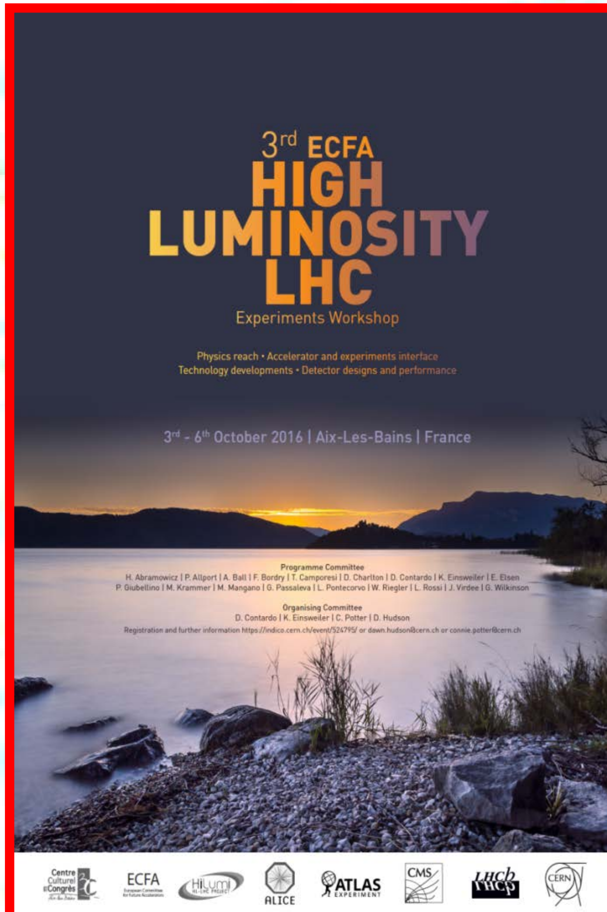
"Europe's top priority should be the exploitation of the full potential of the LHC, including the <u>high-luminosity upgrade of the machine and detectors</u> with a view to collecting ten times more data than in the initial design, by around 2030"

HEPAP in the US (May 2014) decided: "*The <u>HL-LHC</u> is strongly supported and is the first high-priority large-category project in our recommended program*"

CERN Council (June 2016) Formal approval of the High Luminosity LHC project, HL-LHC

Overview of HL-LHC Programme

https://indico.cern.ch/category/4863/



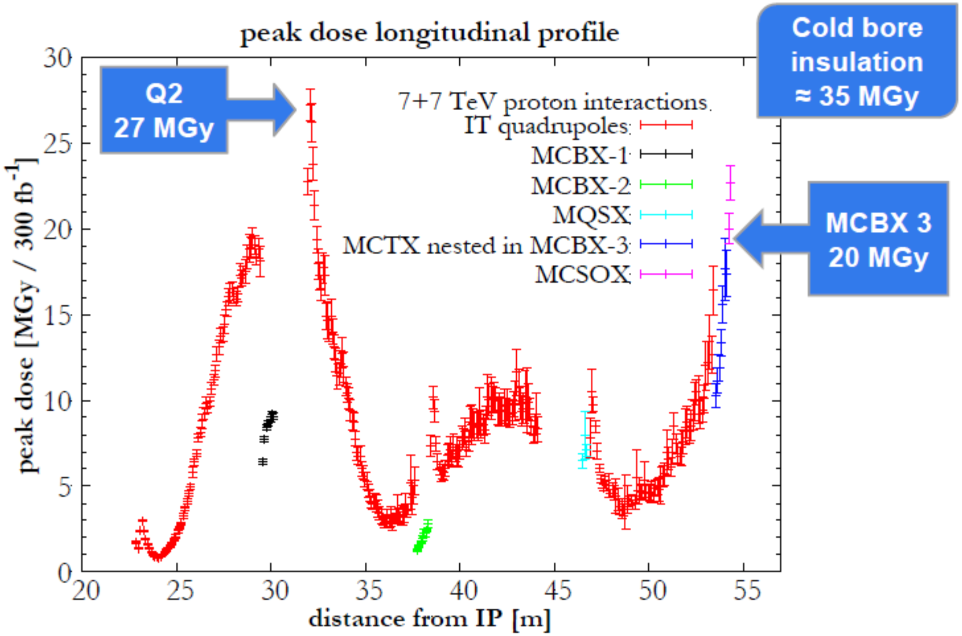
https://indico.cern.ch/event/524795/

Overview of HL-LHC Programme

High Luminosity LHC

UNIVERSITY OF BIRMINGHAM

Radiation damage to triplet magnets at 300 fb-1



LHC accelerator overviw
Frédérick Bordry
3rd ECFA High-luminosity LHC experiments workshop
3rd October 2016 – Aix-les-Bains
12

1983	:	First studies for the LHC project
1988	:	First magnet model (feasibility)
1994	:	Approval of the LHC by the CERN Council
1996-1999	:	Series production industrialisation
1998	:	Declaration of Public Utility & Start of civil engineering
1998-2000	:	Placement of the main production contracts
2004	:	Start of the LHC installation
2005-2007	:	Magnets Installation in the tunnel
2006-2008	:	Hardware commissioning
2008-2009	:	Beam commissioning and repair

2010-2035: Physics exploitation
- 2010 – 2012 : Run 1 ;7 and 8 TeV
- *2015 – 2018 : Run 2 ; 13 TeV*
- 2021 – 2023 : Run 3
- **2024 – 2025 : HL-LHC installation**

HiLumi HL-LHC PROJECT

Around 300 fb^{-1} the present Inner Triplet magnets reach the end of their useful life (due to radiation damage) and must be replaced.

Goal of HL-LHC project:
- 250 – 300 fb^{-1} per year
- **3000 fb^{-1} in about 10 years**

Overview of HL-LHC Programme

UNIVERSITY OF BIRMINGHAM

Goal of High Luminosity LHC (HL-LHC):

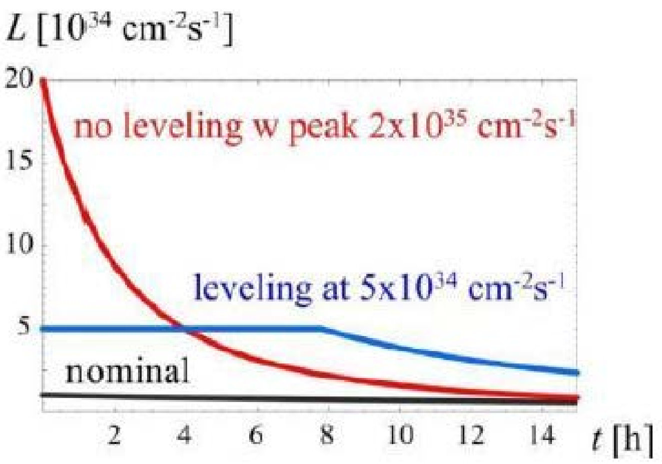
The main objective of HiLumi LHC Design Study is to determine a hardware configuration and a set of beam parameters that will allow the LHC to reach the following targets:

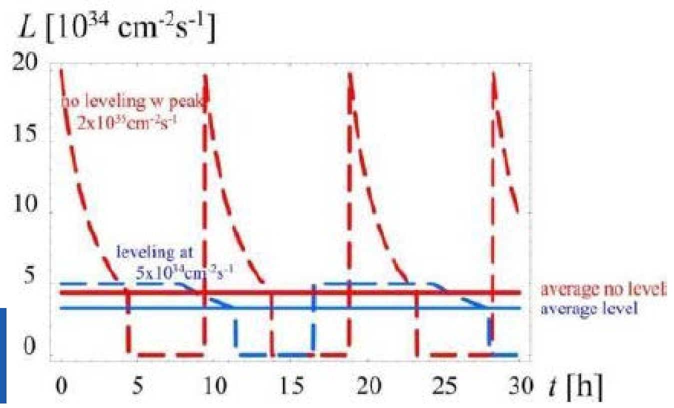
Prepare machine for operation **beyond 2025 and up to 2035-37**

Devise beam parameters and operation scenarios for:

- #enabling a total integrated luminosity of **3000 fb^{-1}**
- #implying an integrated luminosity of **250-300 fb^{-1} per year**,
- #design for μ ~ **140 (~ 200)** (➔ peak luminosity of **5 (7) 10^{34} cm^{-2} s^{-1}**) pile-up density (<1.3 events/mm)
- #design equipment for 'ultimate' performance of **7.5 10^{34} cm^{-2} s^{-1}** and **4000 fb^{-1}**

=> Ten times the luminosity reach of first 10 years of LHC operation



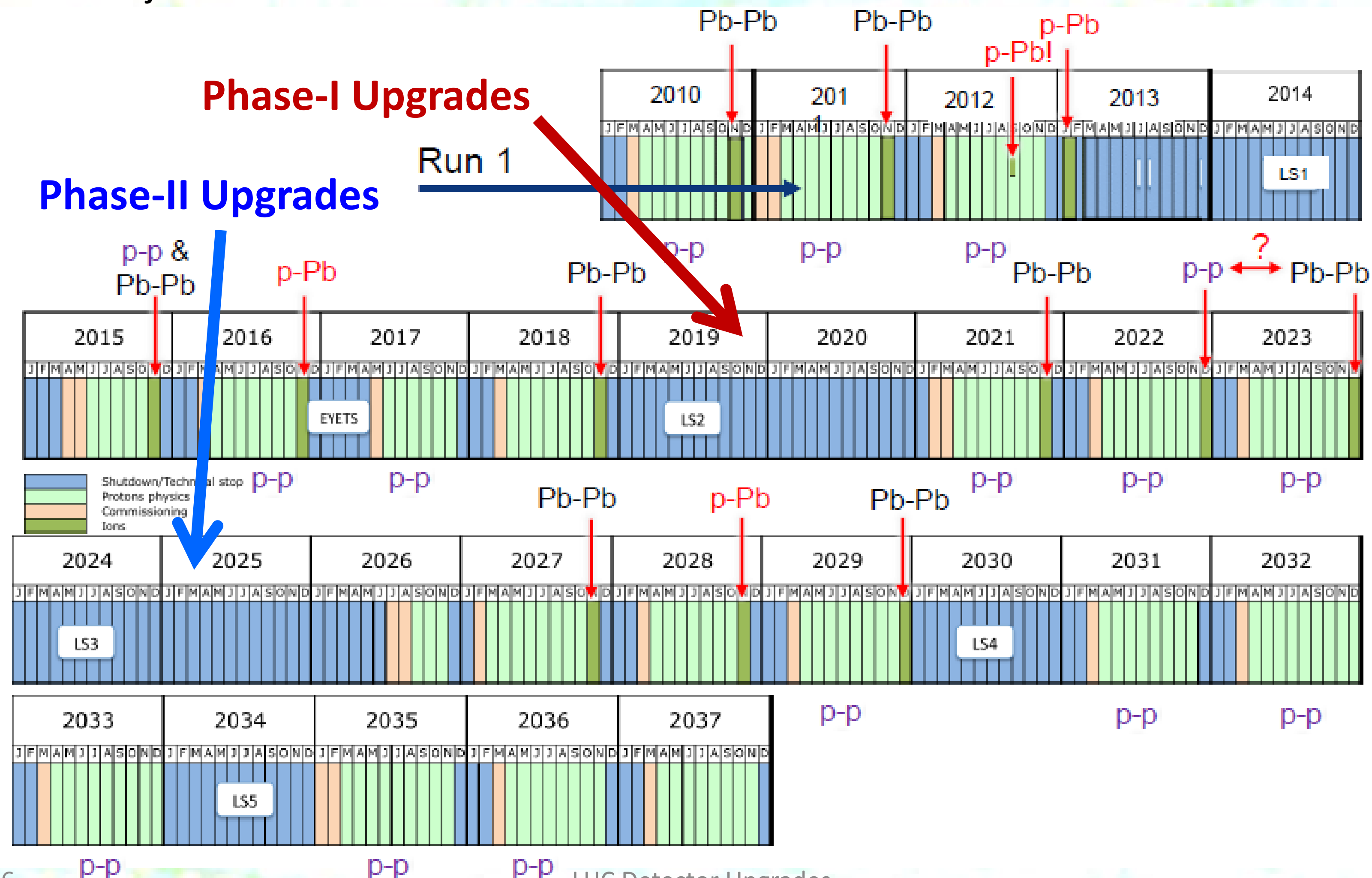


LHC accelerator overviw
Frédérick Bordry
3rd ECFA High-luminosity LHC experiments workshop
3rd October 2016 – Aix-les-Bains
14

LHC Schedule and Nomenclature

EYETS 2016/17 (19 weeks) (no Linac4 connection during Run2)

LS2	starting in 2018 (July)	18 months + 3months BC (Beam Commissioning)
LS3	LHC: starting in 2023 =>	30 months + 3 BC
	injectors: in 2024 =>	13 months + 3 BC

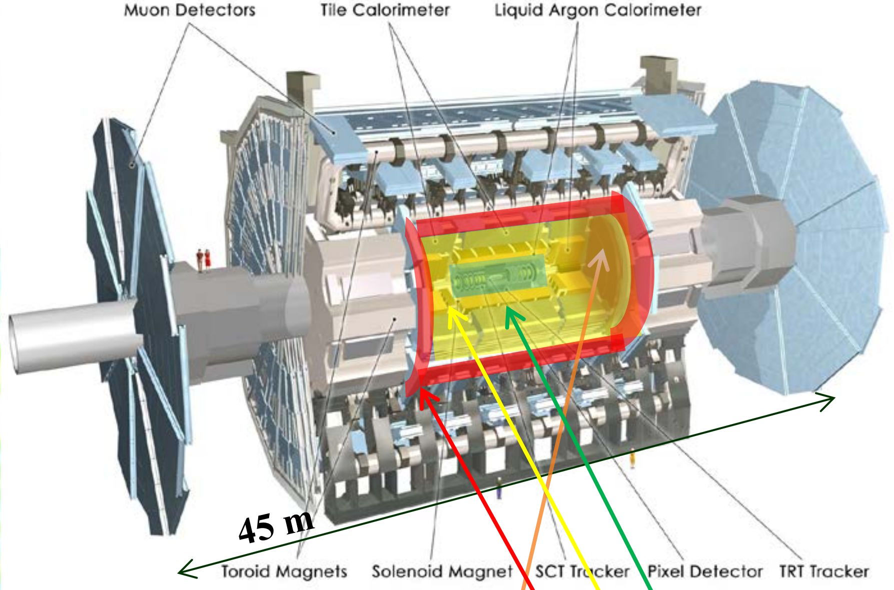


ATLAS: Phase-II Upgrades

High Luminosity LHC

UNIVERSITY OF BIRMINGHAM

https://cds.cern.ch/record/2055248/files/LHCC-G-166.pdf

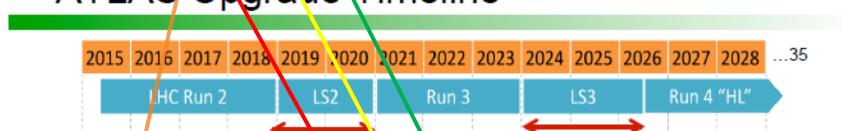


Trigger and Data Acquisition	Scoping Scenarios Reference (275 MCHF)	Middle (235 MCHF)	Low (200 MCHF)
Level-0 Trigger System			
Central Trigger	✓	✓	✓
Calorimeter Trigger (e/γ)	$\lvert\eta\rvert < 4.0$	$\lvert\eta\rvert < 3.2$	$\lvert\eta\rvert < 2.5$
Muon Barrel Trigger	MDT everywhere RPC-BI Tile-μ	MDT (BM & BO only) Partial η coverage RPC-BI Tile-μ	MDT (BM & BO only) No RPC-BI Tile-μ
Muon End-cap Trigger	MDT everywhere	MDT (EE&EM only)	MDT (EE&EM only)
Level-1 Trigger System			
Output Rate [kHz]	400	200	200
Central Trigger	✓	✓	✓
Global Trigger	✓	✓	✓
Level-1 Track Trigger (*RoI based tracking*)	$p_T > 4$ GeV $\lvert\eta\rvert \leq 4.0$	$p_T > 4$ GeV $\lvert\eta\rvert \leq 3.2$	$p_T > 8$ GeV $\lvert\eta\rvert \leq 2.7$
High-Level Trigger			
FTK++ (*Full tracking*)	$p_T > 1$ GeV 100 kHz	$p_T > 1$ GeV 50 kHz	$p_T > 2$ GeV 50 kHz
Event Filter	10 kHz output	5 kHz	5 kHz
DAQ			
Detector Readout	✓ [400 kHz L1 rate]	✓ [200 kHz L1 rate]	✓ [200 kHz L1 rate]
DataFlow	✓ [400 kHz L1 rate]	✓ [200 kHz L1 rate]	✓ [200 kHz L1 rate]

Detector System	Scoping Scenarios Reference (275 MCHF)	Middle (235 MCHF)	Low (200 MCHF)
Inner Tracker			
Pixel Detector	$\lvert\eta\rvert \leq 4.0$	$\lvert\eta\rvert \leq 3.2$	$\lvert\eta\rvert \leq 2.7$
Barrel Strip Detector	✓	✓ [No stub layer]	✓ [No stereo in layers #2,#4] [Remove layer #3] [No stub layer]
Endcap Strip Detector	✓	✓ [Remove 1 disk/side]	✓ [Remove 1 disk/side]
Calorimeters			
LAr Calorimeter Electronics	✓	✓	✓
Tile Calorimeter Electronics	✓	✓	✓
Forward Calorimeter	✓	✗	✗
High Granularity Precision Timing Detector	✓	✗	✗

Muon Spectrometer	Scoping Scenarios Reference (275 MCHF)	Middle (235 MCHF)	Low (200 MCHF)
Barrel Detectors and Electronics			
RPC Trigger Electronics	✓	✓	✓
MDT Front-End and readout electronics (BI+BM+BO)	✓	✓ [BM+BO only]	✓ [BM+BO only]
RPC Inner layer in the whole layer	✓	✓ [in half layer only]	✗
Barrel Inner sMDT Detectors in the whole layer	✓	✓ [in half layer only]	✗
MDT L0 Trigger Electronics (BI +BM+BO)	✓	✓ [BI +BM only]	✓ [BI +BM only]
End-cap and Forward Muon Detectors and Electronics			
TGC Trigger Electronics	✓	✓	✓
MDT L0 Trigger and Front-End read-out electronics (EE+EM+EO)	✓	✓ [EE +EM only]	✓ [EE +EM only]
sTGC Detectors in Big Wheel Inner Ring	✓	✓	✓
Very-forward Muon tagger	✓	✗	✗

ATLAS Upgrade Timeline



Phase-1 Upgrade	Phase-2 Upgrade
L = 2e34 (μ~60) int L = 200 fb^{-1}	L = 7.5e34 (μ~200) int L = 3000 fb^{-1}
• New Muon Small Wheel (NSW) • Fast Track Trigger (FTK) • TDAQ Phase-1 • LAr Calorimeter Electronics • ATLAS Forward Protons (AFP)	• All new Tracking Inner Detector (ITk-Strip/Pixel) • Calorimeter Electronics Upgrade • New Forward Calorimeter ? • Muon System Upgrade • TDAQ Phase-2

CMS: Phase-II Upgrades

http://cds.cern.ch/record/2055167/files/LHCC-G-165.pdf?version=4

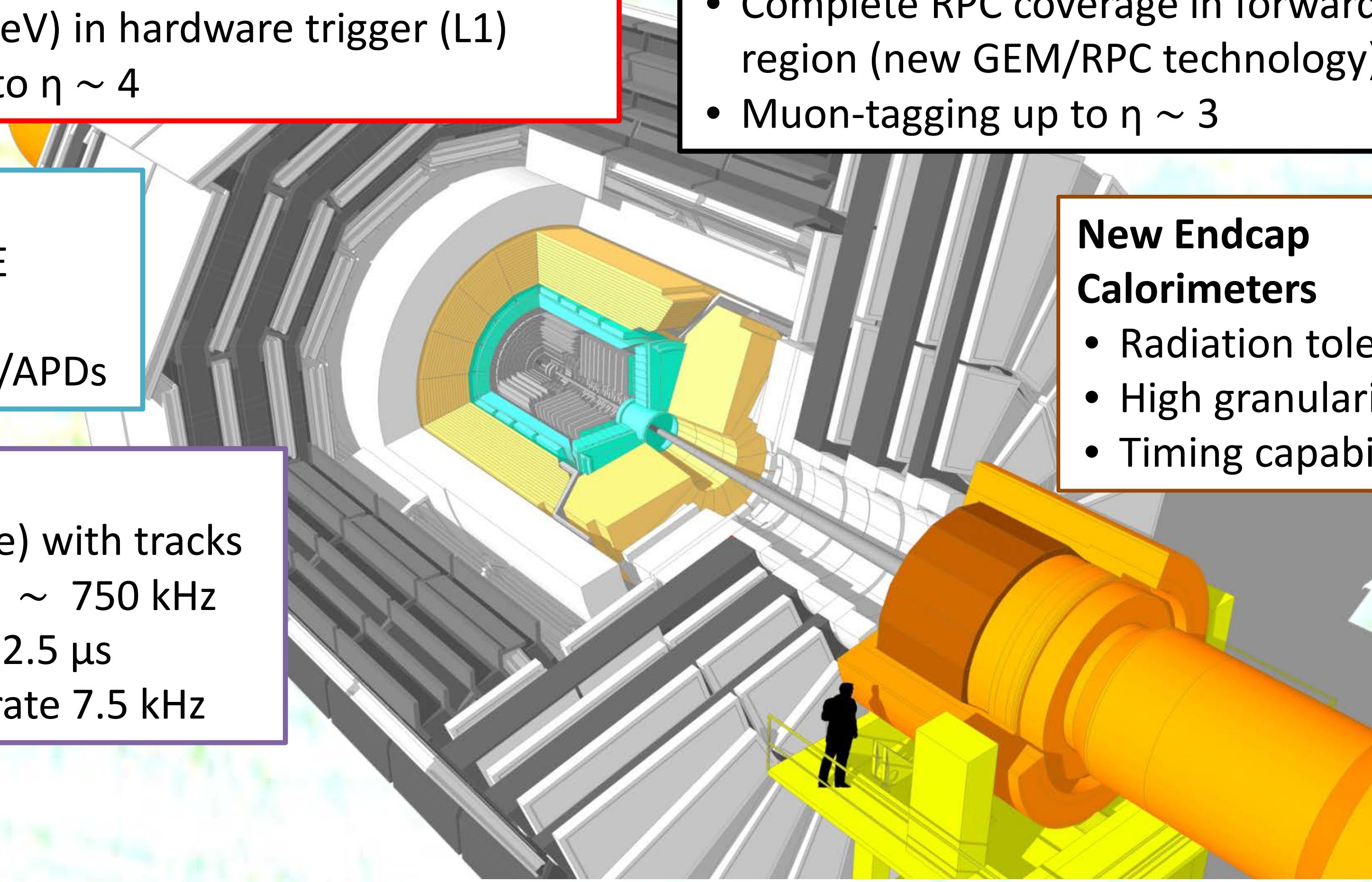
New Tracker
- Radiation tolerant - high granularity - less material
- Tracks (P_T>2GeV) in hardware trigger (L1)
- Coverage up to η ~ 4

Muons
- Replace DT and CSC FE/BE electronics
- Complete RPC coverage in forward region (new GEM/RPC technology)
- Muon-tagging up to η ~ 3

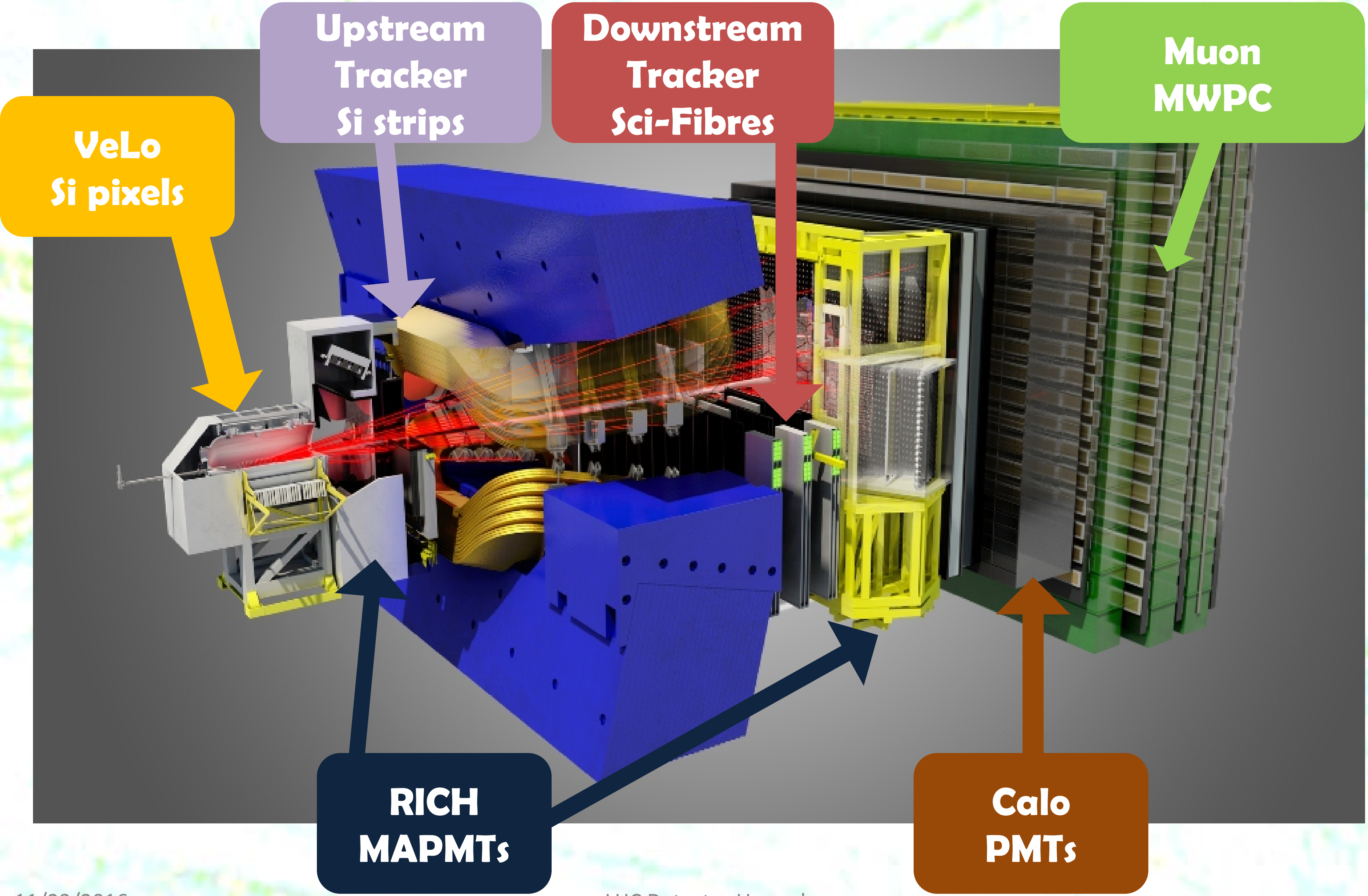
Barrel ECAL
- Replace FE/BE electronics
- Cool detector/APDs

New Endcap Calorimeters
- Radiation tolerant
- High granularity
- Timing capability

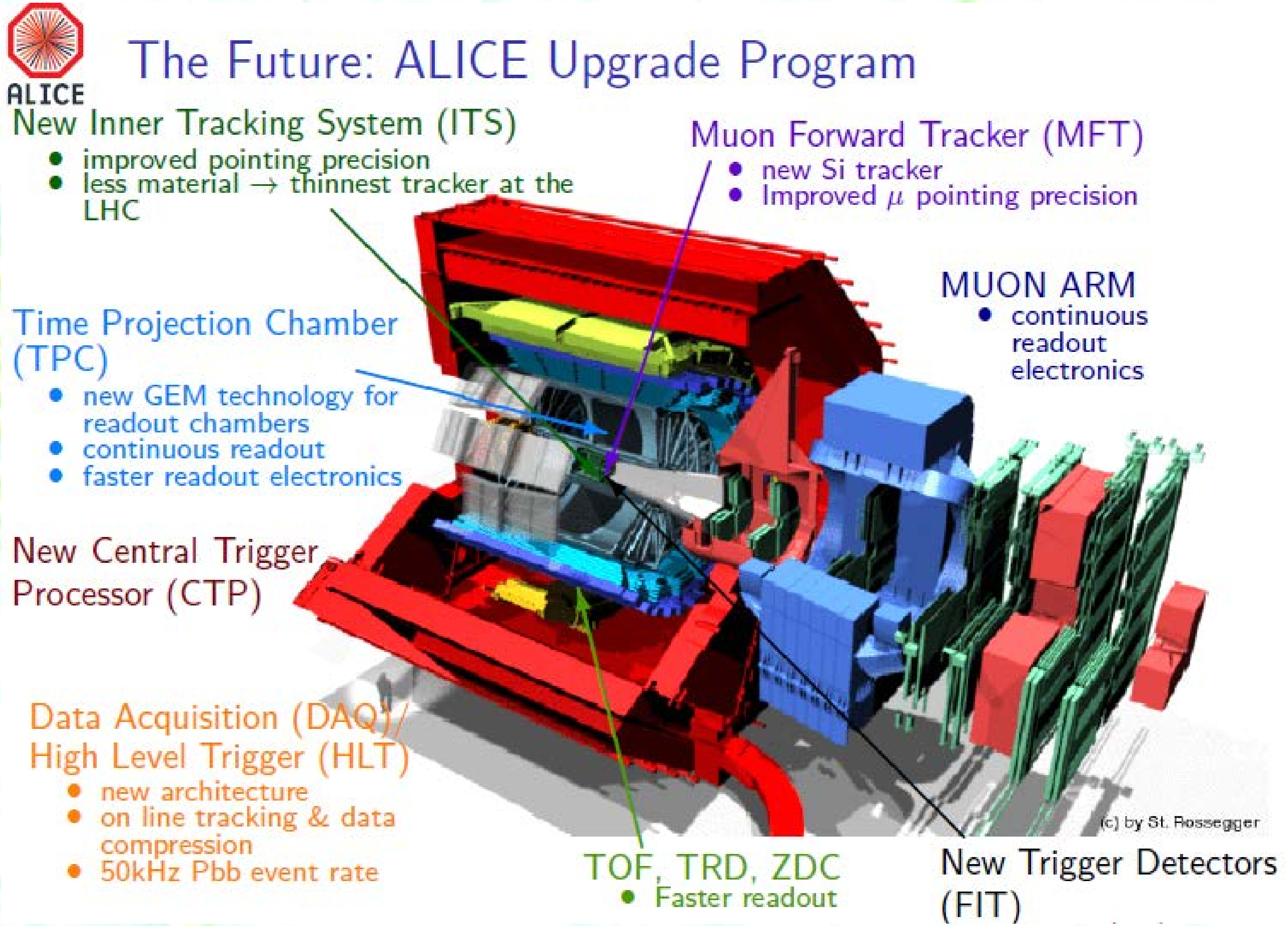
Trigger/DAQ
- L1 (hardware) with tracks and rate up ~ 750 kHz
- L1 Latency 12.5 μs
- HLT output rate 7.5 kHz



LHCb: Phase-I Upgrades

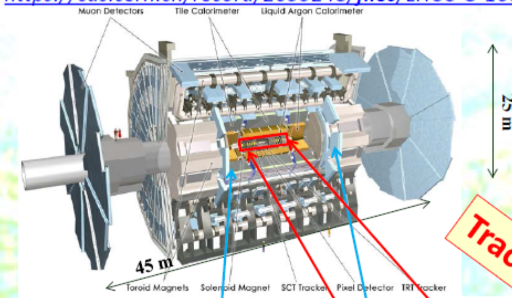


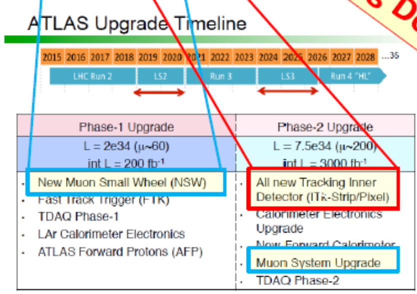
ALICE: Phase-I Upgrades



ATLAS: Phase-II Upgrades

https://cds.cern.ch/record/2055248/files/LHCC-G-166.pdf





Trigger and Data Acquisition	Scoping Scenarios: Reference (275 MCHF)	Middle (235 MCHF)	Low (200 MCHF)
Level-0 Trigger System			
Central Trigger	✓	✓	✓
Calorimeter Trigger (e/γ)	|η| < 4.0	|η| < 3.2	|η| < 2.5
Muon Barrel Trigger	MDT everywhere, RPC BI, Tile-μ	MDT (BM & BO only), Partial η coverage RPC BI, Tile-μ	MDT (BM & BO only), No RPC BI, Tile-μ
Muon End-cap Trigger	MDT everywhere	MDT (EE&EM only)	MDT (EE&EM only)
Level-1 Trigger System			
Output Rate (kHz)	400	200	200
Central Trigger	✓	✓	✓
Global Trigger	✓	✓	✓
Level-1 Track Trigger (RoI based tracking)	p_T > 4 GeV, |η| ≤ 4.0	p_T > 4 GeV, |η| ≤ 3.2	p_T > 8 GeV, |η| ≤ 2.7
High-Level Trigger			
FTK++ (Full tracking)	p_T > 1 GeV, 100 kHz	p_T > 1 GeV, 50 kHz	p_T > 2 GeV, 50 kHz
Event Filter	10 kHz output	5 kHz	5 kHz
DAQ			
Detector Readout	✓ [400 kHz L1 rate]	✓ [200 kHz L1 rate]	✓ [200 kHz L1 rate]
DataFlow	✓ [400 kHz L1 rate]	✓ [200 kHz L1 rate]	✓ [200 kHz L1 rate]

Detector System	Scoping Scenarios: Reference (275 MCHF)	Middle (235 MCHF)	Low (200 MCHF)
Inner Tracker			
Pixel Detector	|η| ≤ 4.0	|η| ≤ 3.2	|η| ≤ 2.7
Barrel Strip Detector	✓	✓ [No stub layer]	✓ [No stereo in layers #2,#4] [Remove layer #3] [No stub layer]
Endcap Strip Detector	✓	✓ [Remove 1 disk/side]	✓ [Remove 1 disk/side]
Calorimeters			
[illegible] Calorimeter Electronics	✓	✓	✓
[illegible] Electronics	✓	✓	✓
[illegible]	✓	✗	✗
[illegible]	✓	✗	✗

[illegible]	Scoping Scenarios: Reference ([illegible] MCHF)	Middle (235 MCHF)	Low (200 MCHF)
Barrel Dete[illegible]			
RPC Trigger Ele[illegible]	[illegible]	✓	✓
MDT Front-End and readout electronics (BI+BM+BO)	[illegible]	[illegible]	✓ [BM+BO only]
RPC Inner layer in the whole layer	✓	[illegible] only]	✗
Barrel Inner sMDT Detectors in the whole layer	✓	[illegible] layer only]	✗
MDT L0 Trigger Electronics (BI+BM+BO)	✓	✓ [BI+BM only]	✓ [BI+BM only]
End-cap and Forward Muon Detectors and Electronics			
TGC Trigger Electronics	✓	✓	✓
MDT L0 Trigger and Front-End read-out electronics (EE+EM+EO)	✓	✓ [EE+EM only]	✓ [EE+EM only]
sTGC Detectors in Big Wheel Inner Ring	✓	✓	✓
Very-forward Muon tagger	✓	✗	✗

Tracking Detector Upgrades

CMS: Phase-II Upgrades

http://cds.cern.ch/record/2055167/files/LHCC-G-165.pdf?version=4

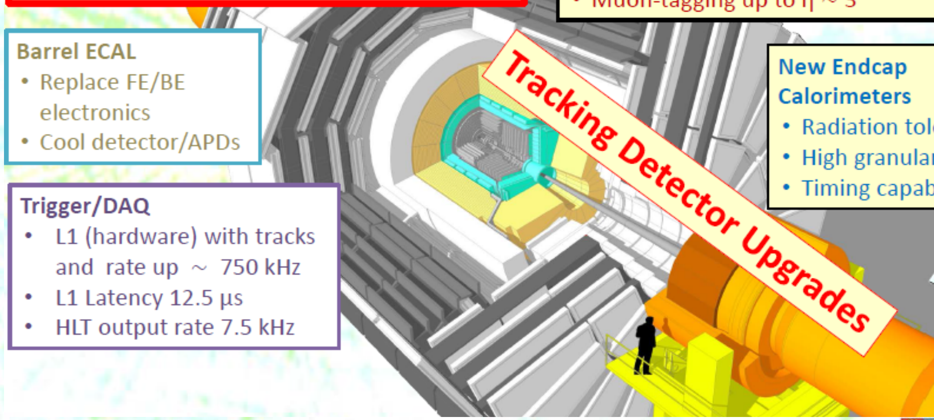
New Tracker
- Radiation tolerant - high granularity - less material
- Tracks (P_T>2GeV) in hardware trigger (L1)
- Coverage up to η ~ 4

Muons
- Replace DT and CSC FE/BE electronics
- Complete RPC coverage in forward region (new GEM/RPC technology)
- Muon-tagging up to η ~ 3

Barrel ECAL
- Replace FE/BE electronics
- Cool detector/APDs

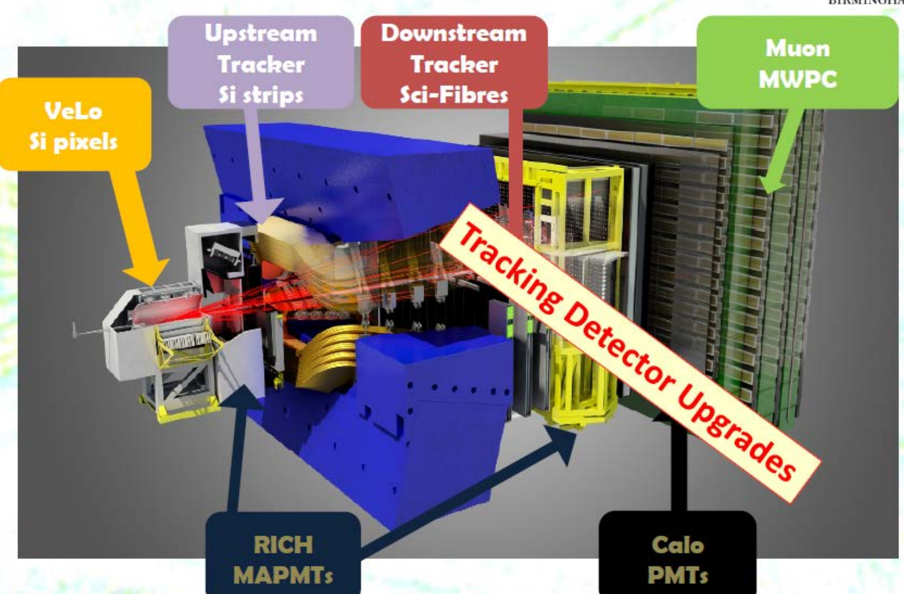
New Endcap Calorimeters
- Radiation tolerant
- High granularity
- Timing capability

Trigger/DAQ
- L1 (hardware) with tracks and rate up ~ 750 kHz
- L1 Latency 12.5 μs
- HLT output rate 7.5 kHz



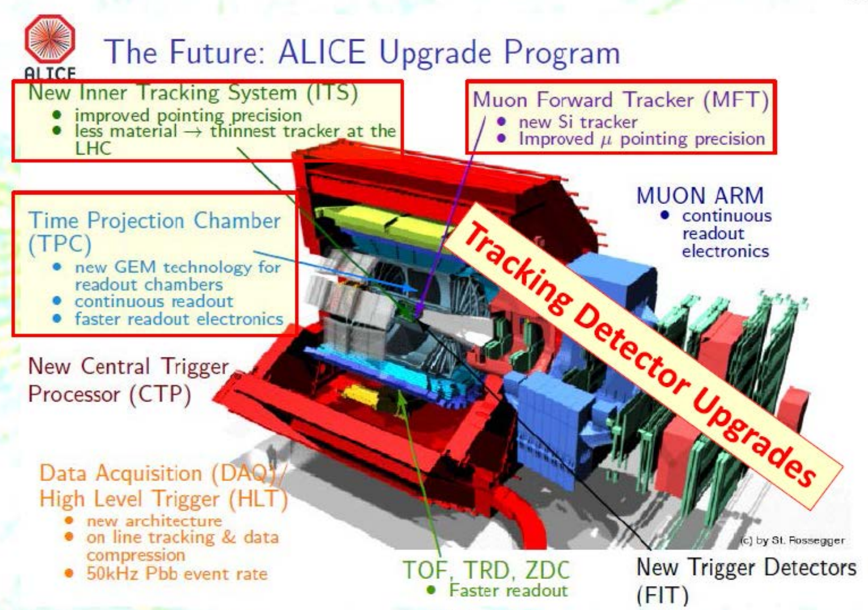
Tracking Detector Upgrades

LHCb: Phase-I Upgrades



Tracking Detector Upgrades

ALICE: Phase-I Upgrades



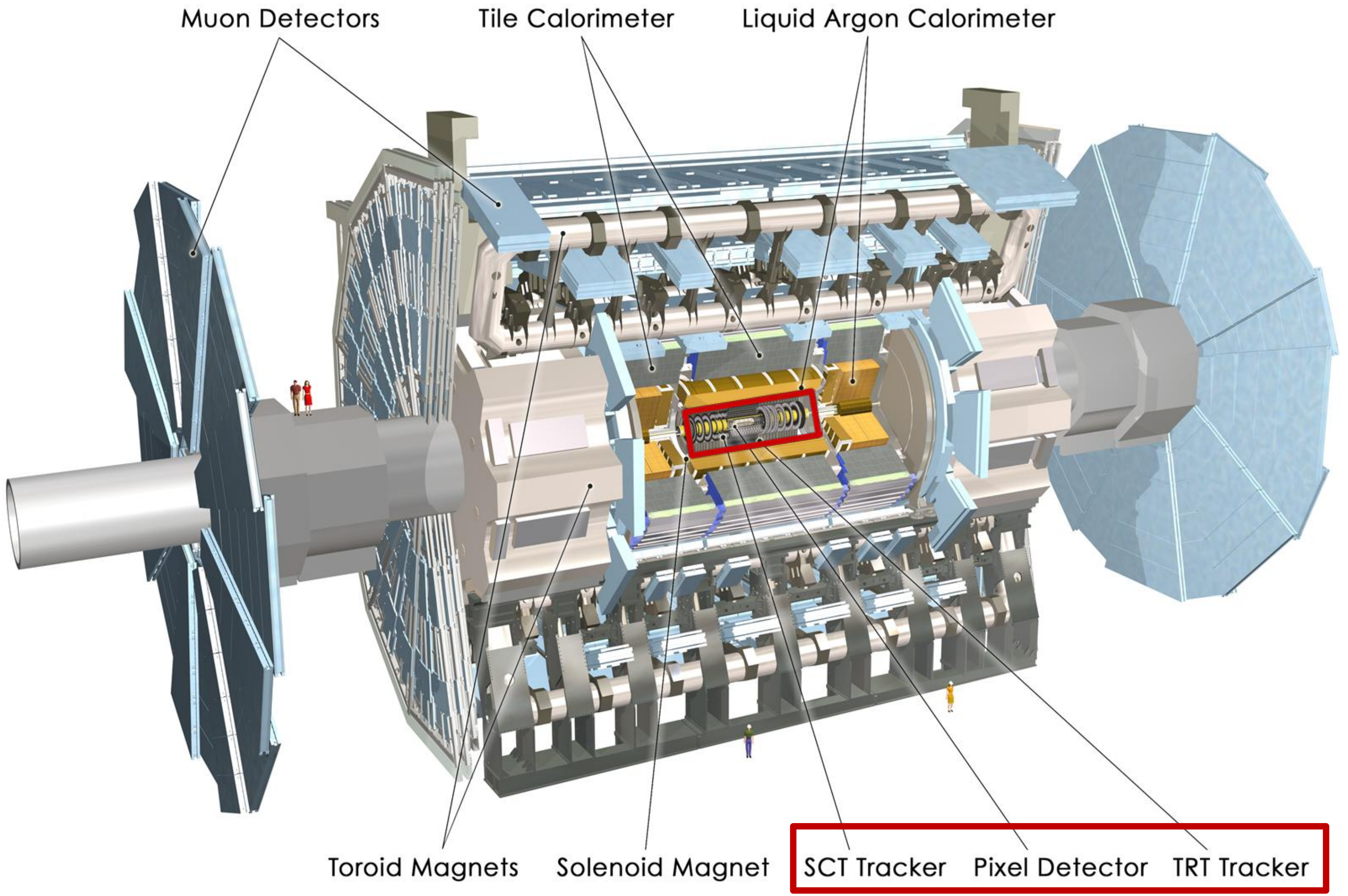
Tracking Detector Upgrades

Tracking Technologies

- For HL-LHC, fine granularity over large areas and minimal mass are targeted consistent with constraints of very high radiation environment, very high hit and data rates, cooling, plus complex event triggering capabilities
- Vertex detectors target finest granularity (RD53: 50μm×50 μm pixels), minimal scattering material (ALICE: <0.5% X_0/layer) and the highest radiation tolerance (ATLAS and CMS: $2\times10^{16} n_{eq}/cm^2$ and 1Grad, RD50)
- Large area silicon coverage for high efficiency track finding (>99% for muons), precision momentum resolution (even 30% at 1 TeV), good extrapolation outwards and into pixel layers, excellent pattern recognition even in dense jets, low material, triggering capability and be highly cost effective
- Systems require low mass cooling and compact, radiation-hard, optical plus electrical links with HV/LV multiplexing (very large numbers of channels running at low voltages drawing high currents → power loss in cables)
- Muon detectors need improved spatial resolution and enhanced rate capability → advanced micro-pattern gas detectors
- Fast detector plus electronics layers with read-out into first level of triggering
- Large area detector construction necessitates very close links with industry to develop designs and processes for mass production
- Other technologies include scintillating fibres (LHCb) and straws (NA62, Mu2e)

ATLAS Tracker Upgrade (ITk)

Current ATLAS Inner Detector ($60m^2$, 10^8 channels)

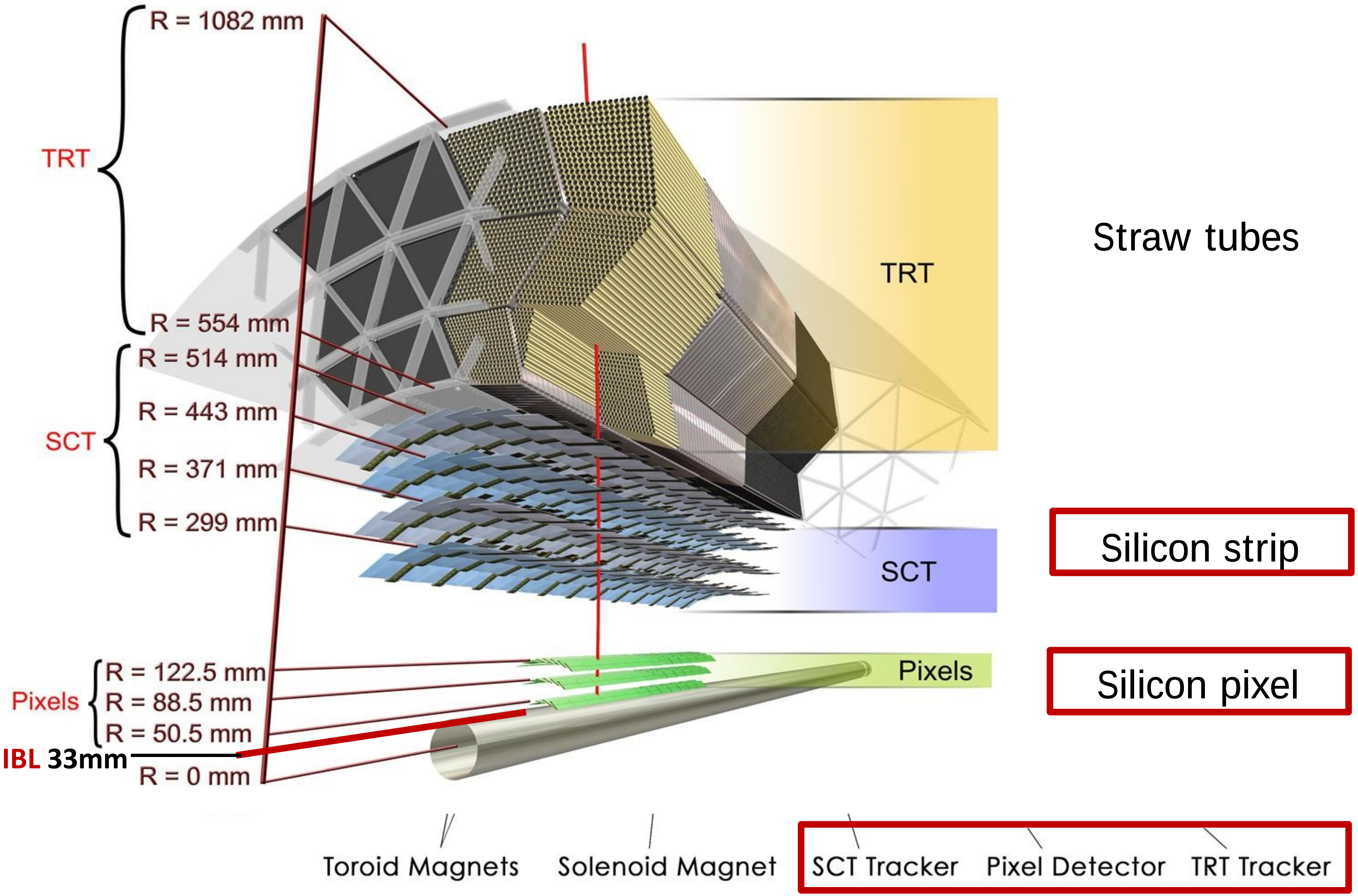


ATLAS Tracker Upgrade (ITk)

High Luminosity LHC

UNIVERSITY OF BIRMINGHAM

Current ATLAS Inner Detector (60m^2, 10^8 channels)



Straw tubes

Silicon strip

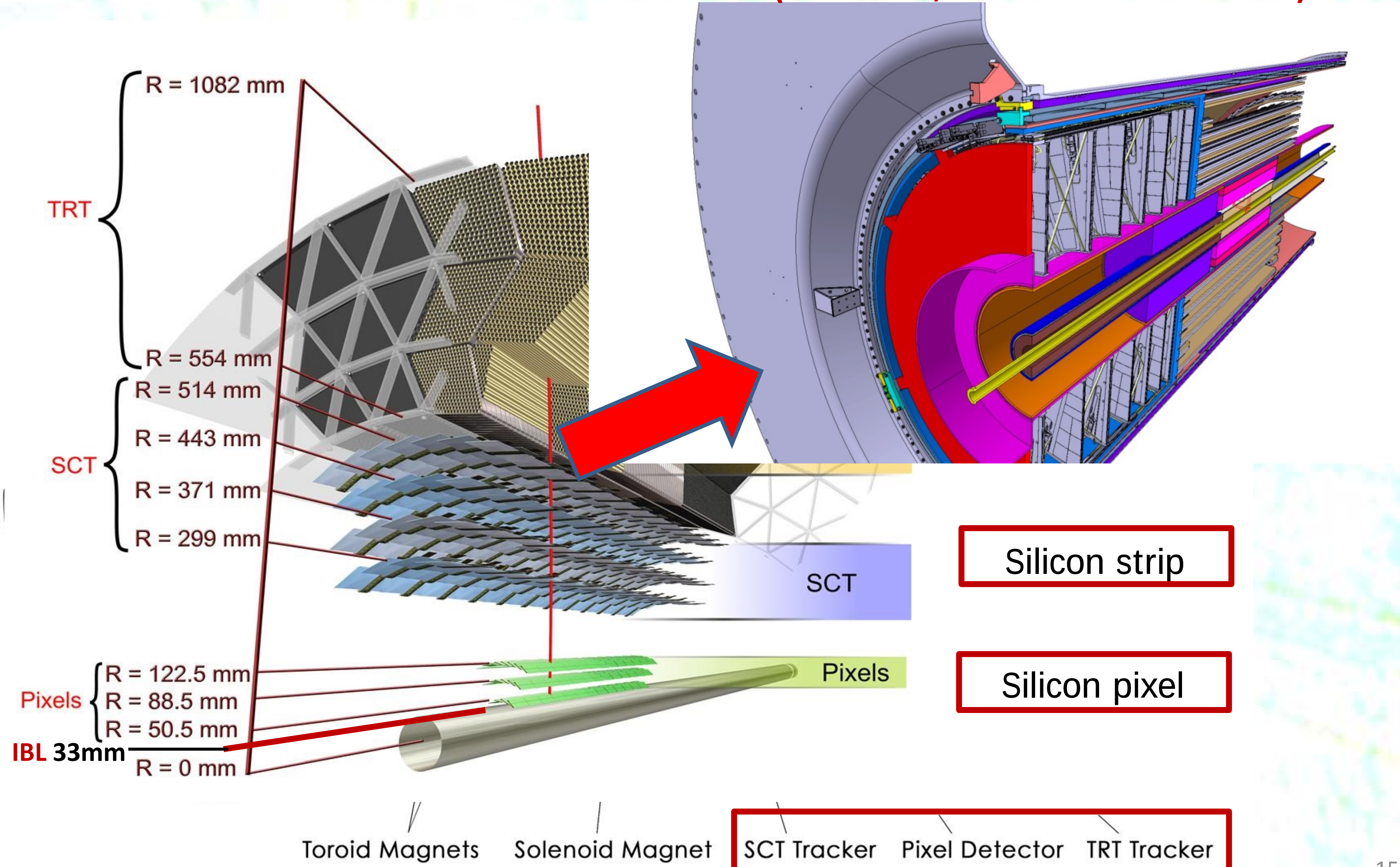
Silicon pixel

High Luminosity LHC

ATLAS Tracker Upgrade (ITk)

UNIVERSITY OF BIRMINGHAM

New All Silicon Inner Detector (200m^2, ~10^{10} channels)

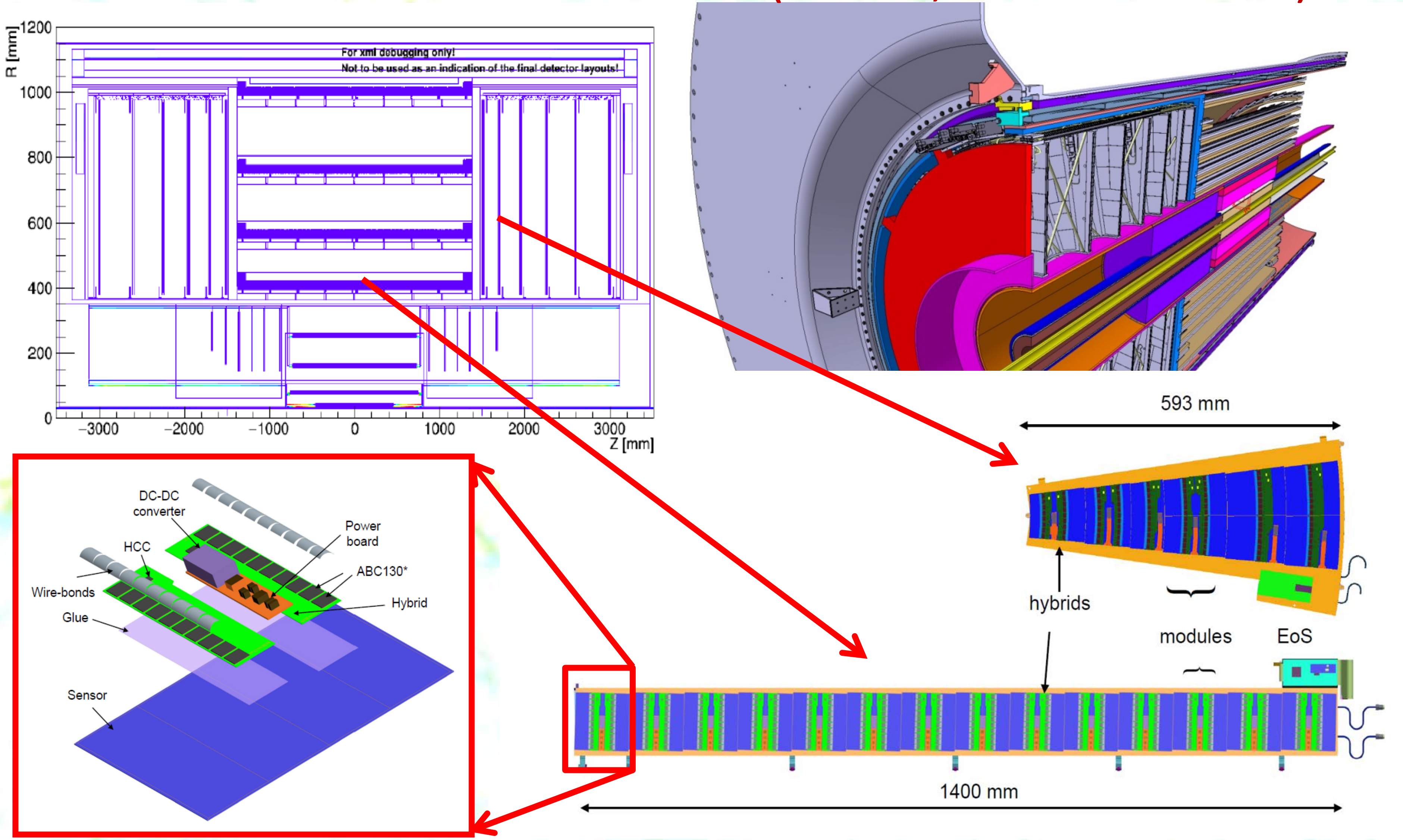


ATLAS Tracker Upgrade (ITk)

High Luminosity LHC

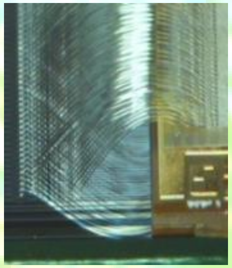
UNIVERSITY OF BIRMINGHAM

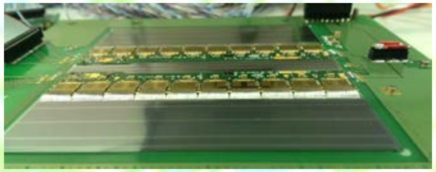
New All Silicon Inner Detector (200m^2, ~10^{10} channels)



ATLAS Tracker Upgrade (ITk)

Single-sided modules sandwiched around low mass structures

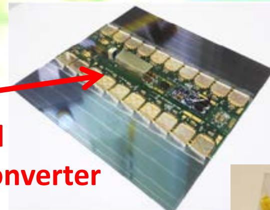




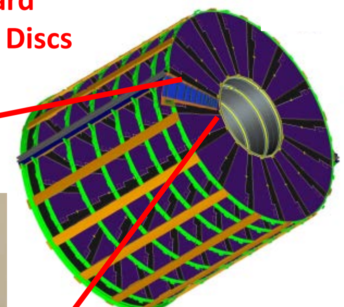
256 Channel ASICs (4 row wire bonding) in 130nm CMOS with L0/L1 functionality

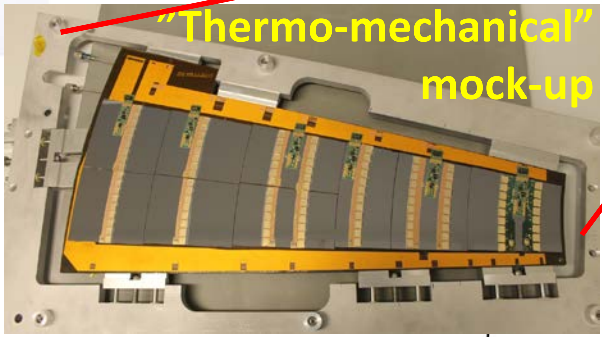
Powering (DC/DC strip Serial pixel), HV multiplexing, CO_2 embedded cooling, low mass modular supports & services

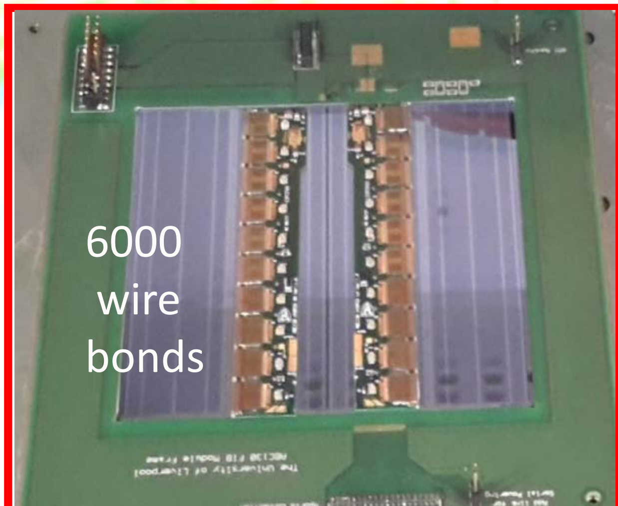
Module with on-board DC-DC converter

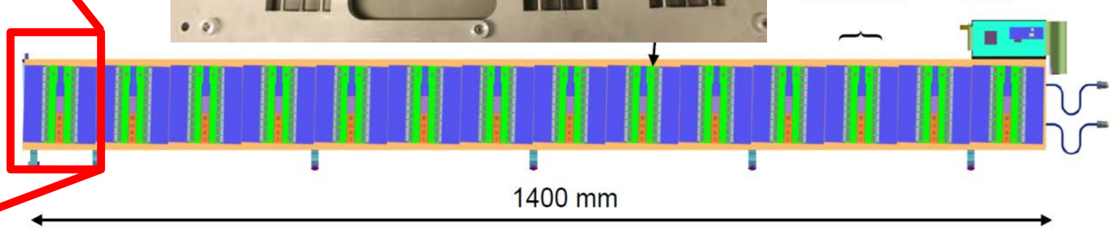


ATLAS Forward Wedges and Discs

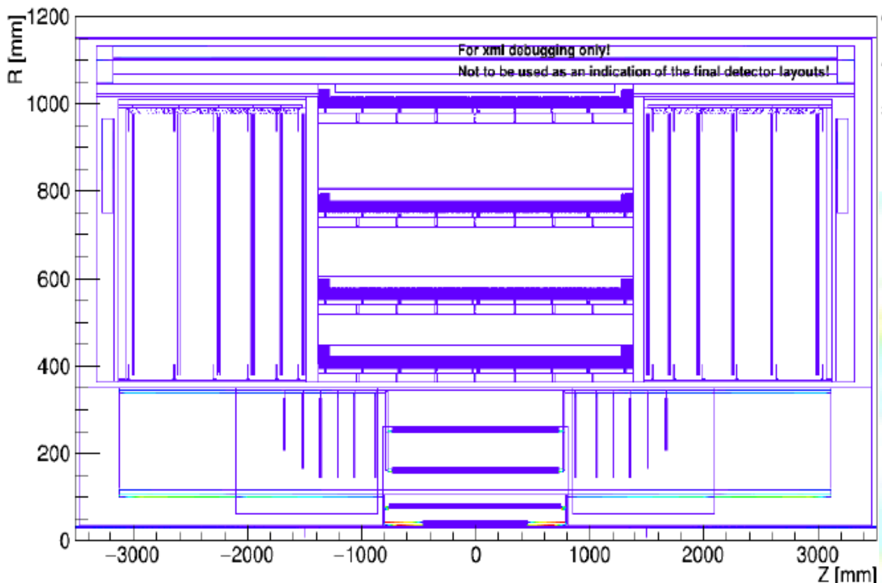


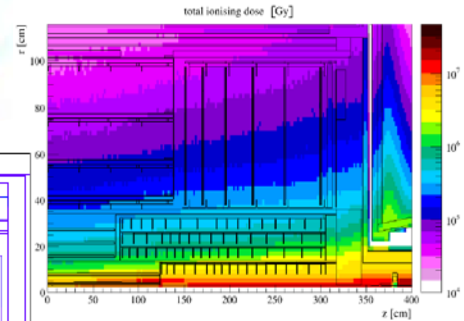






ATLAS Tracker Upgrade (ITk)

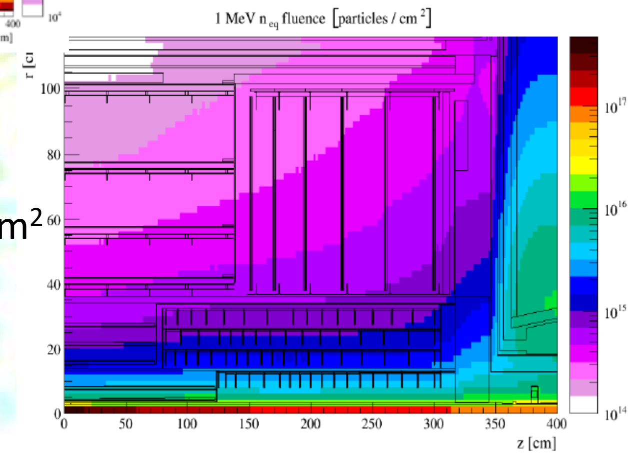


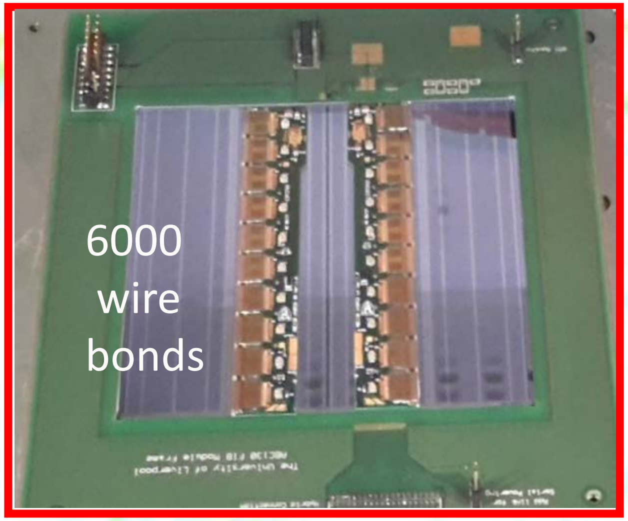


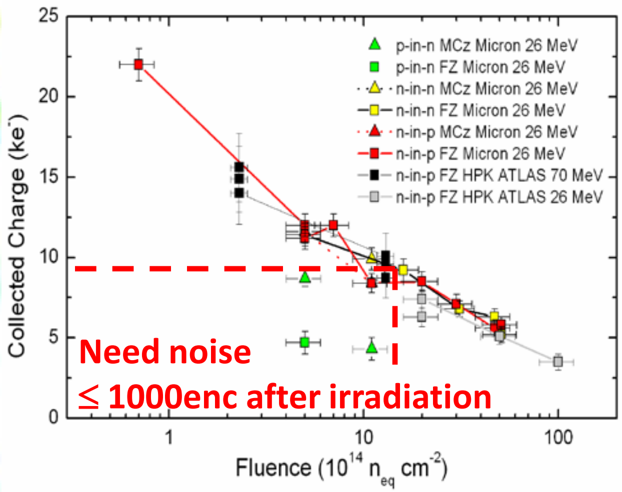
Unprecedented levels of radiation at HL-LHC

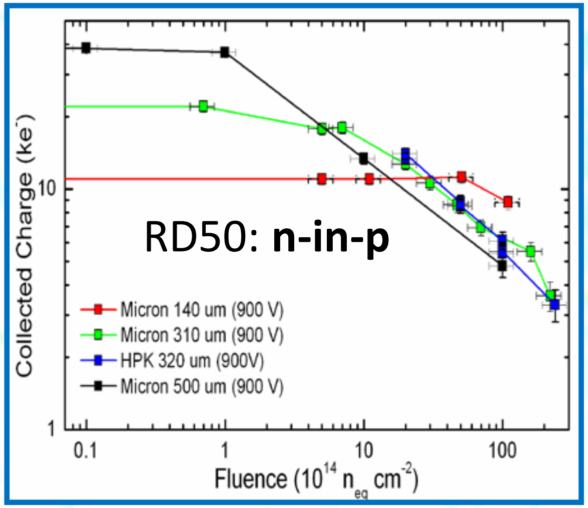
Strip detectors must survive damage to lattice equivalent to that from $1.2\times10^{15}/cm^2$ 1 MeV neutrons and 0.5 MGy

(Pixels > ×10 this)

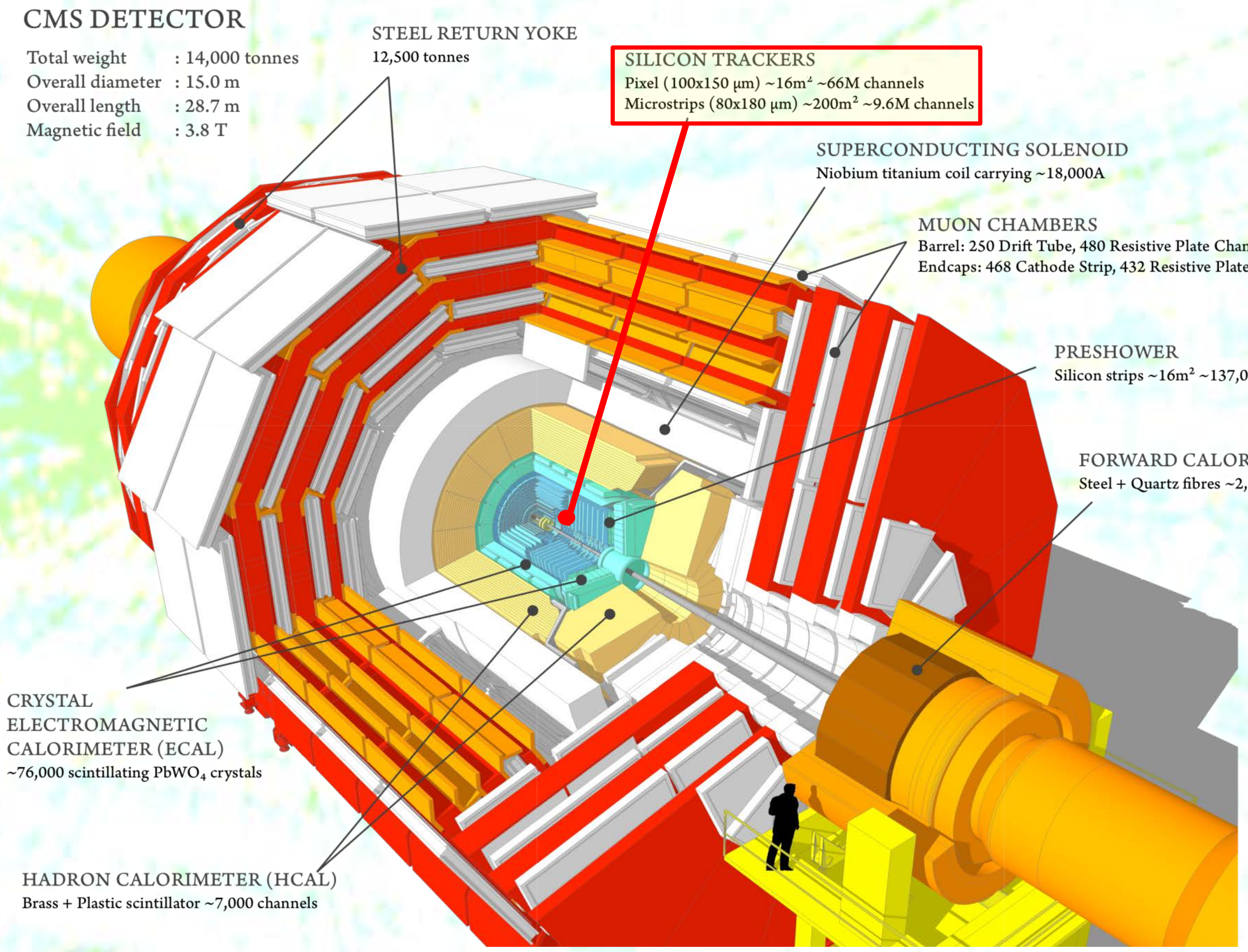








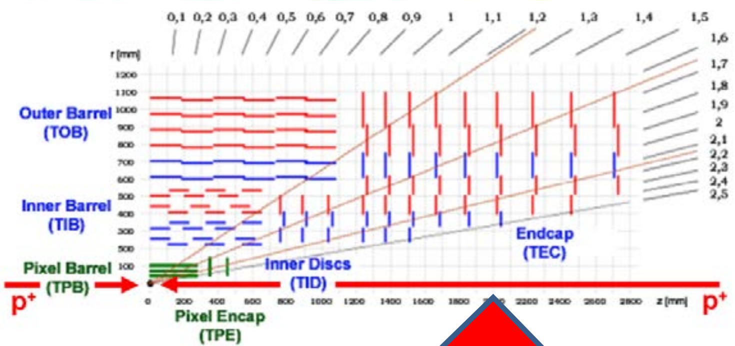
CMS Tracker Upgrade



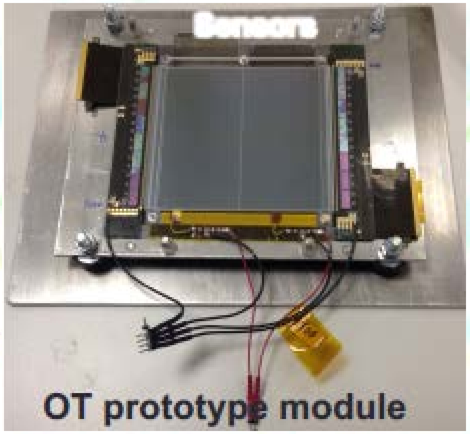
CMS Tracker Upgrade

Outer trackers need radiation hardness of current n-in-n pixel sensors at fraction of the cost

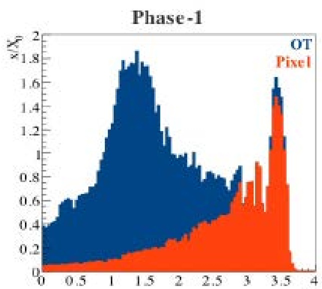
→ **ATLAS/CMS: n-in-p strip technology**



Many large area sensors produced for both ATLAS and CMS

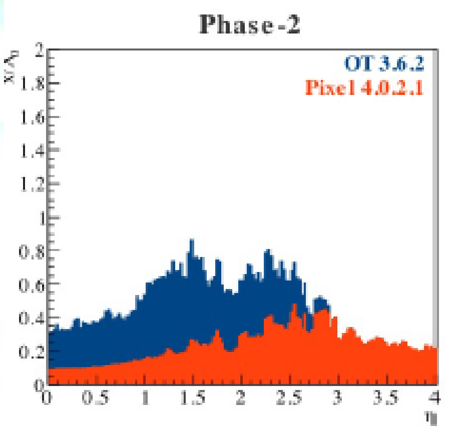


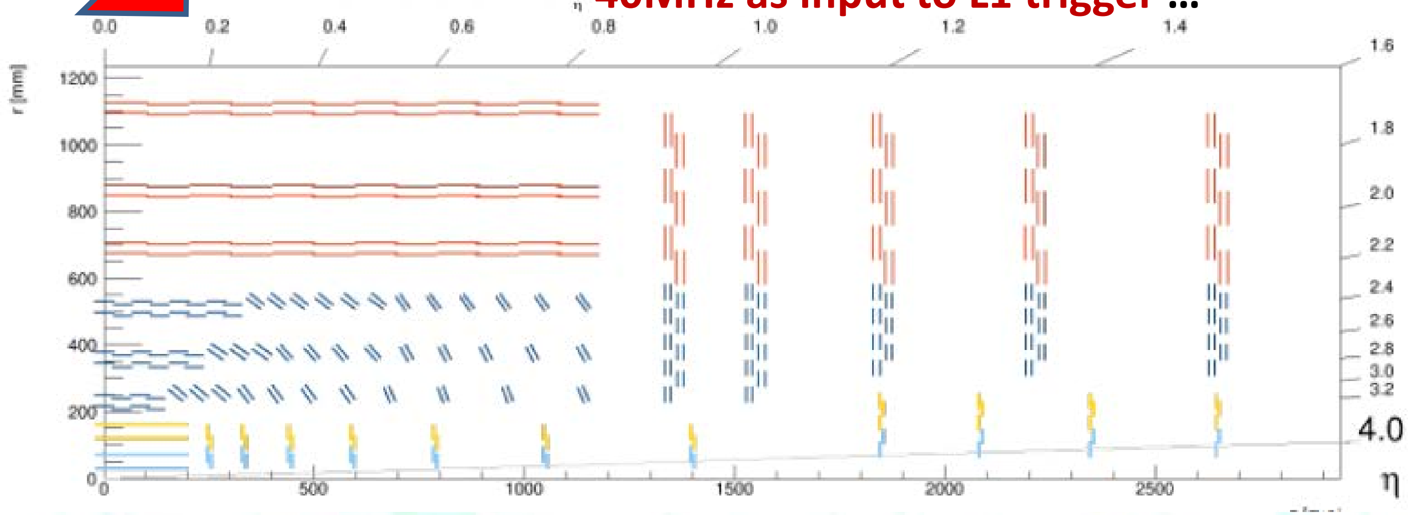
Interest in larger (8”) wafers particularly for forward regions (and HGCAL)



In CMS design driven by requirement to identify all tracks with P_T>2GeV at 40MHz as input to L1 trigger …

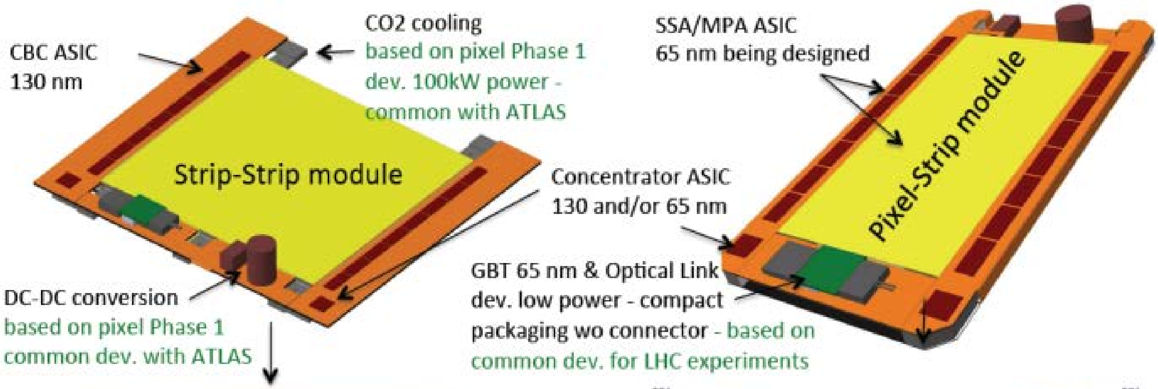
Greatly reduced material in tracking volume

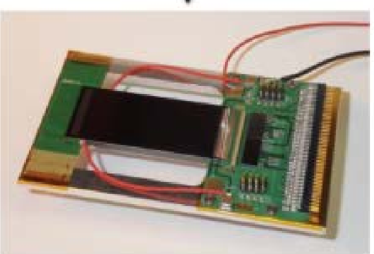


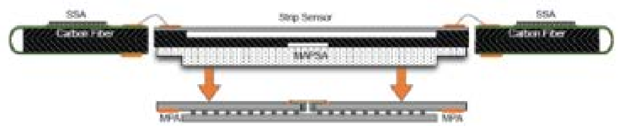


CMS Tracker Upgrade

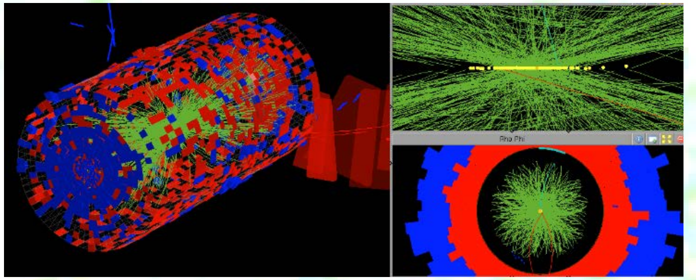
Paired layers with short strips (outer radii) and long pixels plus short strips (inner radii)

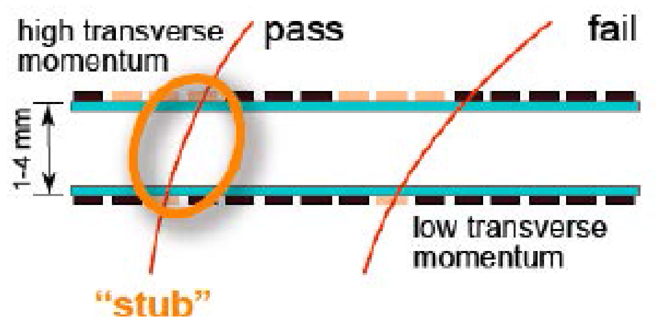


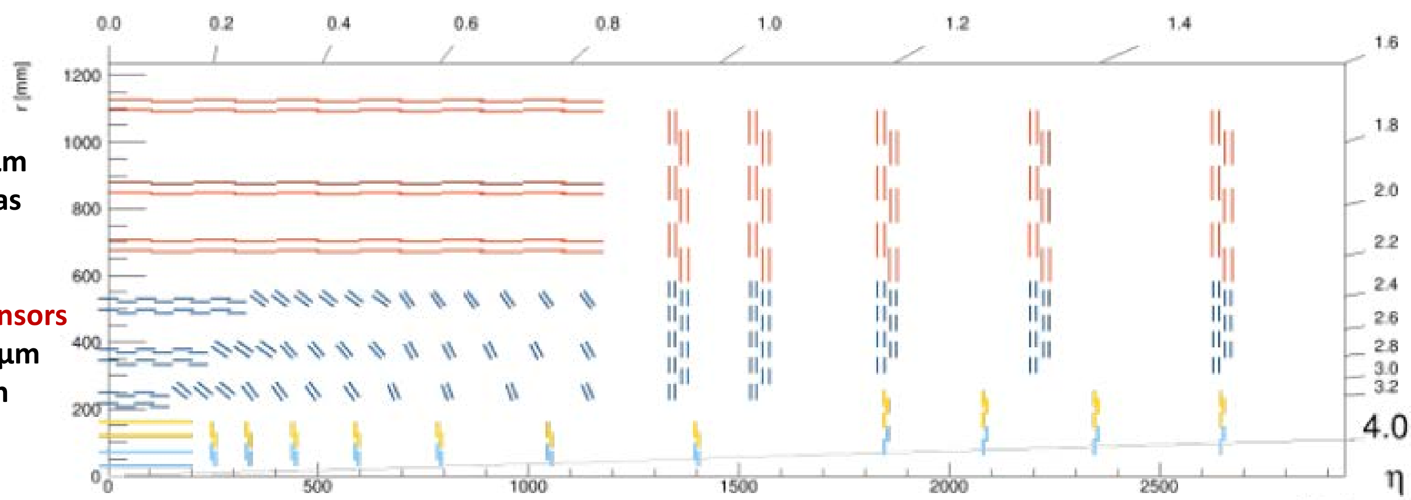




Flex hybrid - Flip-Chip assembly - possibly TSV for inter-chip connection







5cm x 10cm silicon strip sensors

- strips: length 2.5cm, pitch 100µm
- AC coupled with poly-silicon bias resistors

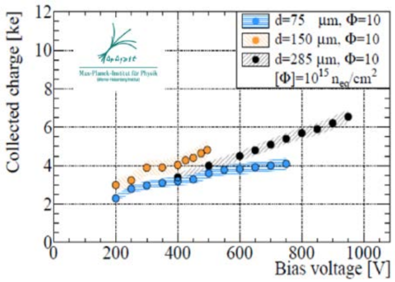
5cm x 10cm silicon macro-pixel sensors

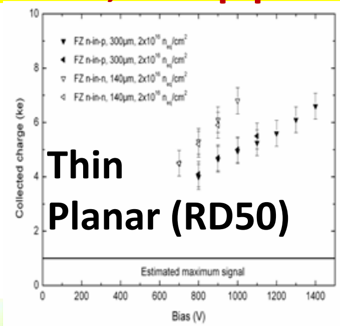
- strips: length 1.5mm, pitch 100µm
- DC coupled with punch-through biasing

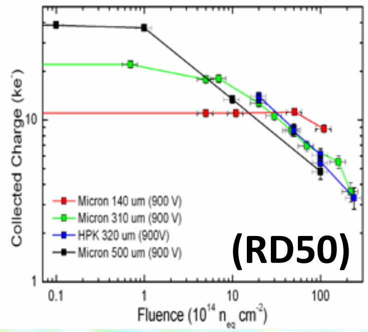
Hadron Collider Hybrid Pixels

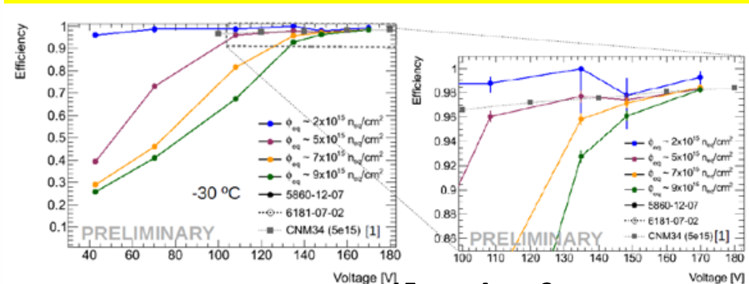
(ECFA 13/284 https://cds.cern.ch/record/1631032)

HL-LHC (3000fb^{-1}) implies doses up to $2\times10^{16}n_{eq}/cm^2$ and 1Grad (also up to 200 collisions per beam crossing). However n-in-n, n-in-p planar, 3D and diamond sensors are useable after such doses



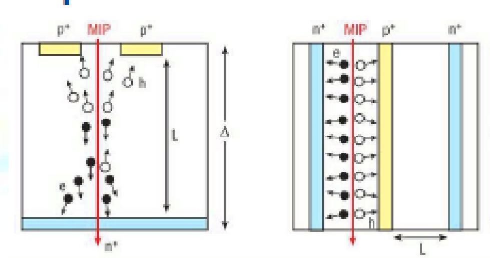






3D after $9\times10^{15}n_{eq}/cm^2$ (RD50)

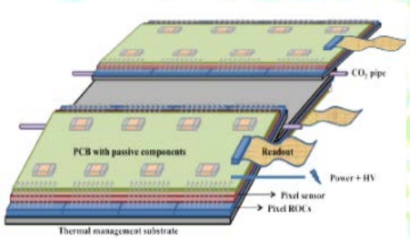
→ The mechanisms leading to larger than expected signals (also seen in 3D sensors) is mostly understood and is even now being exploited (doping profile, trenches) to enhance the signals after radiation

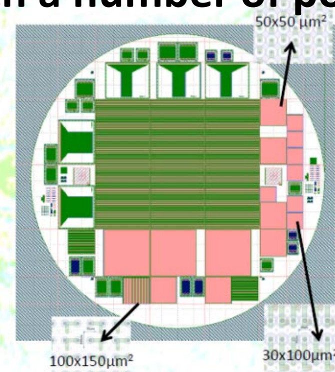


(3D sensors installed in ATLAS IBL)

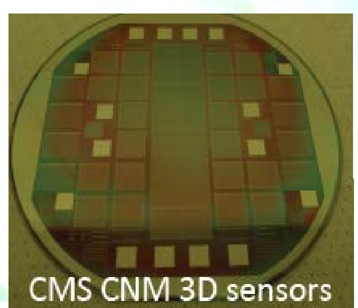
Use of 65nm (RD53) CMOS ASIC technology allows pixel sizes of 50µm×50µm or 25µm×100µm (LHCb VeLoPIX 130nm: 55µm×55µm)

Large format sensors needed to tile larger areas and examples have been prototyped with a number of potential suppliers



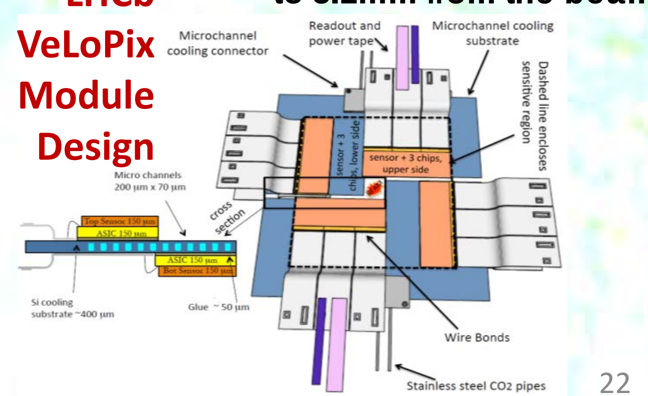


CMS Small Pitch 3D Run



LHCb VeLoPix Module Design

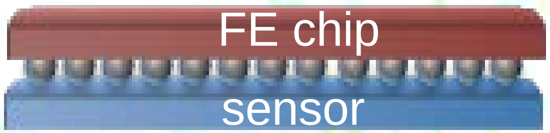
24 stations with sensors down to 5.1mm from the beam



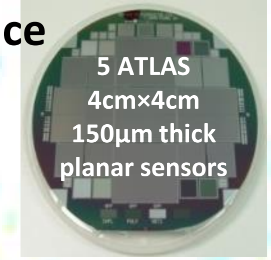
Hadron Collider Hybrid Pixels

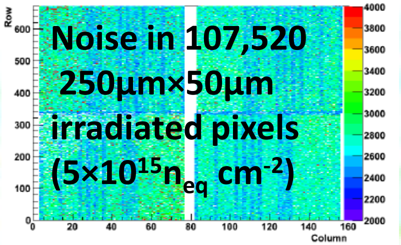
(ECFA 13/284 https://cds.cern.ch/record/1631032)

- **Irradiated single and quad n-in-p pixel modules (for higher radii) studied in test-beam with excellent performance**

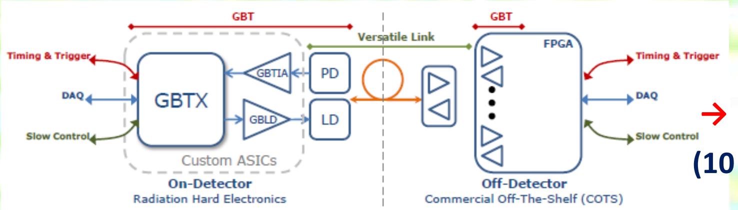


Conventional bump-bonding





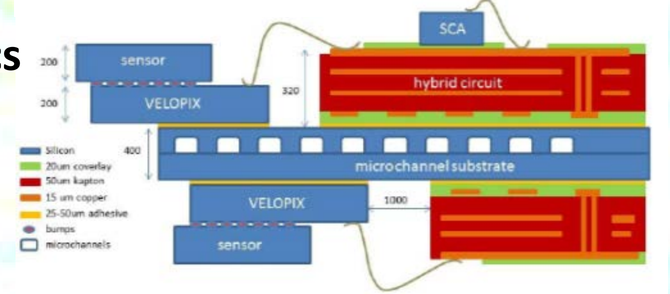
- **Micro-channel in-silicon cooling (LHCb, ALICE, NA62)**
- **Need custom rad-hard, low power, fast opto-electronics**



→ **lpGBTx, + VTTx**

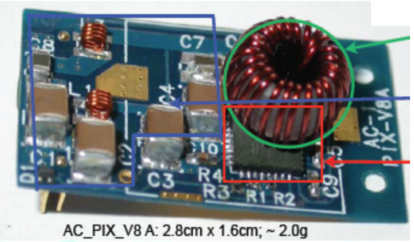
(10 Gbit/s plus versatile link)

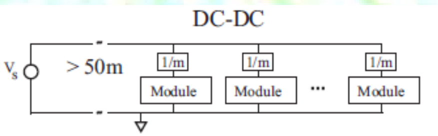
LHCb VeLoPix Module

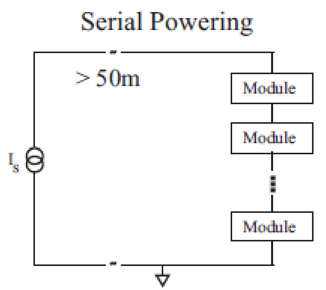


- **Low mass structures, services (electrical link to optical for innermost layers), LV (serial powering for innermost layers, DC/DC elsewhere), CO_2 cooling…**

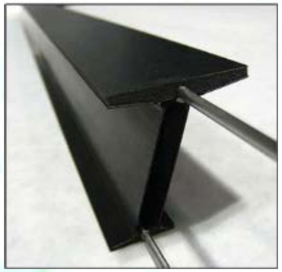
DC to DC converter to step down 10V→2.5V

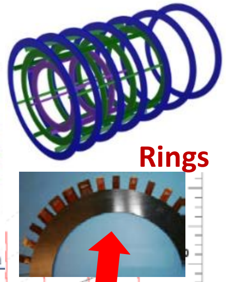


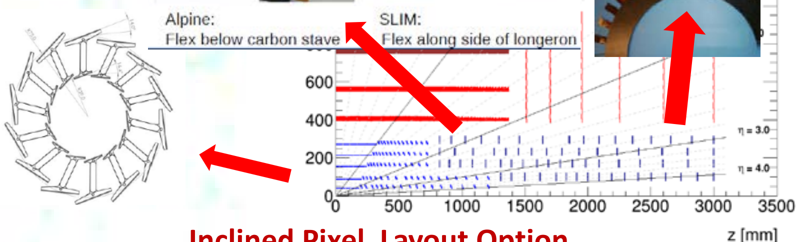




ATLAS Phase-II Prototype Barrel Pixel Supports







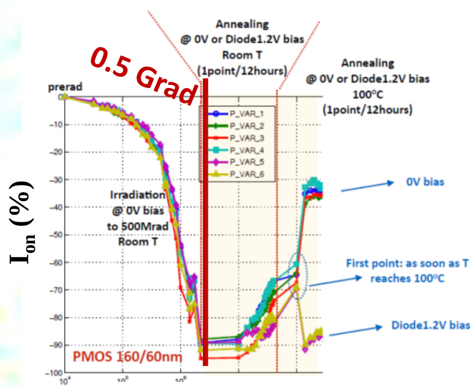
Inclined Pixel Layout Option

ATLAS and CMS Pixel Read-out

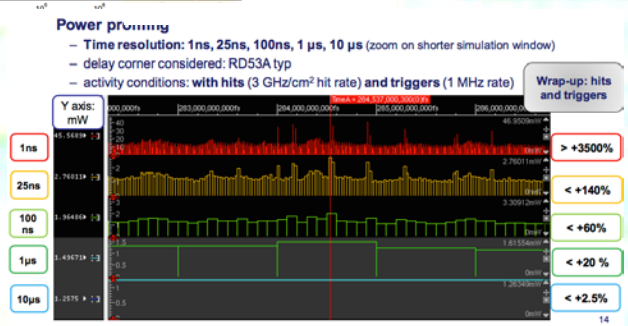
RD53: Common 65nm CMOS pixel ASIC development

(LHCC Report)

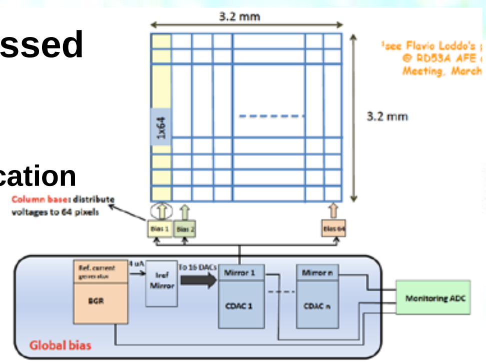
- **Many Challenges being addressed**
  - **PMOS test structure radiation effects with narrow and short channels**
  - **Architecture simulations and optimization using Monte Carlo hit data from experiments.**
  - **Global floor plan: Upscaled small demonstrator**
  - **Shared repositories: IPs, FEs, RTL code, Simulation, full design**
  - **Optimization of design flow & tools for very large complex design**
  - **Integration of FEs (4) with biasing and required adaptions**
  - **Integration of monitoring: ADC, Temp sensor, voltages, currents, etc.**
  - **Integration of serial powering**
    - **Distributed power dissipation, power profiling, decoupling, system simulations**
  - **Integration of IO pad frame**
  - **Digital: RTL coding and technology mapping**
    - **Pixel array: Optimization (power, size, radiation tolerance)**
    - **EOC: Command decoder, chip configuration, readout data formatting, data compression**
    - **Synthesis and timing optimization/verification with radiation effects**
    - **Verification framework**

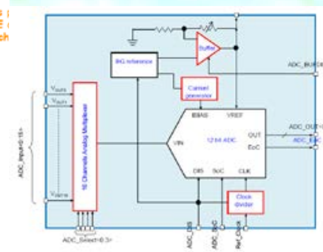


Significant V_t shift can develop with annealing depending on Temperature, Time, Bias, Device type, L, W, Received dose, but Indication that detrimental effects can be "avoided"/delayed by keeping cold



- **Several topics still to be addressed**
  - **SEU optimisation and verification**
  - **Final integration**
  - **Extensive Analog and Digital verification**
  - **DRC verification**
  - **Submission**

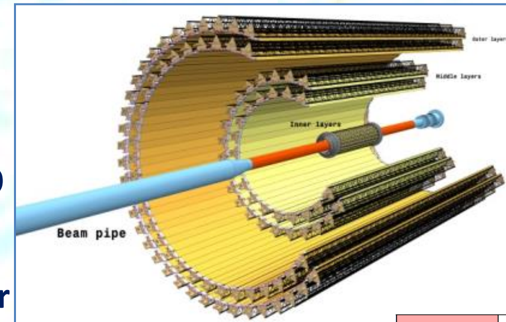




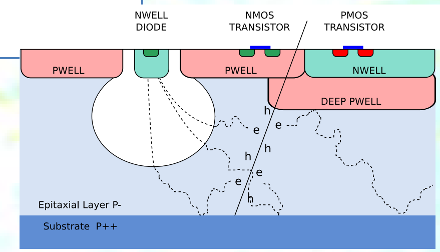
400x400 pixels power	Typ	Worst
Analog array	0.96W	1.6W
Digital array	0.77W	0.99W
EOC	0.2W	0.3W
IO	0.2W	0.3W
Shunt-LDO	0.5W (25%)	1W (30%)
Total	**~3W**	**~4W**

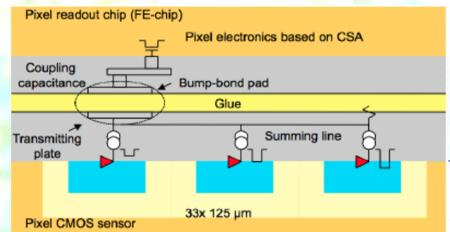
MAPS HV/HR-CMOS Detectors

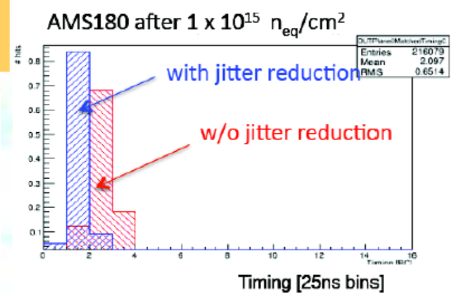
- **Commercial CMOS Image Sensors offer possible dramatic decrease in costs (Monolithic Active Pixel Sensors)**
- **MAPS can deliver very low power consumption at low R/O speeds, possibly <100mW/cm² i.e. simple water cooling**
  - **Ultra low material budget (cf ALICE ITS upgrade: <0.5% for inner layers, <1% for outer layers)**
  - **But these devices limited in speed and radiation hardness**
  - **Current and proposed MAPS for heavy ion experiments**
  - **integration time up to 4μs (noise, electron diffusion)**
  - **radiation resistance up to few 10^{13} $n_{eq}cm^{-2}$**
- **Major developments in HV/HR-CMOS → deep depletion region with charge collection by drift not diffusion → huge improvements in collection speed and radiation hardness**
- **Can either incorporate aspects of the analogue functionality into the sensor and simply glue to the FE ASIC developed for the hybrid pixel solution or go full monolithic → DMAPS**
- **Results on both approaches show very promising radiation hardness**

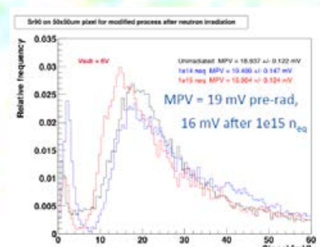


TDR for the upgrade of the ALICE inner tracking system
CERN-LHCC-2013-024

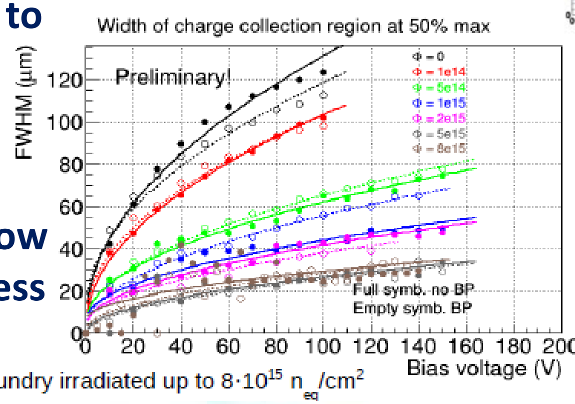




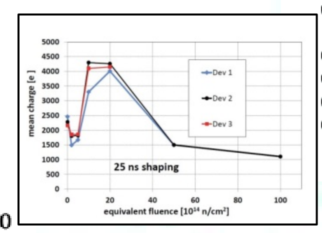




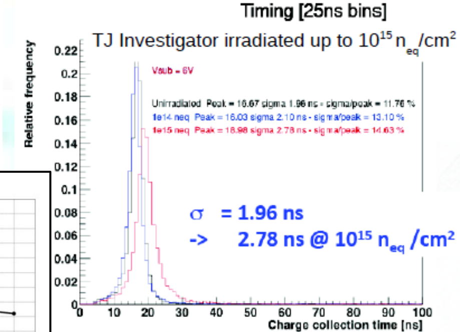
ATLAS, ALICE and RD50



LFoundry irradiated up to $8 \cdot 10^{15}$ n_{eq}/cm^2



Neutron Irradiation

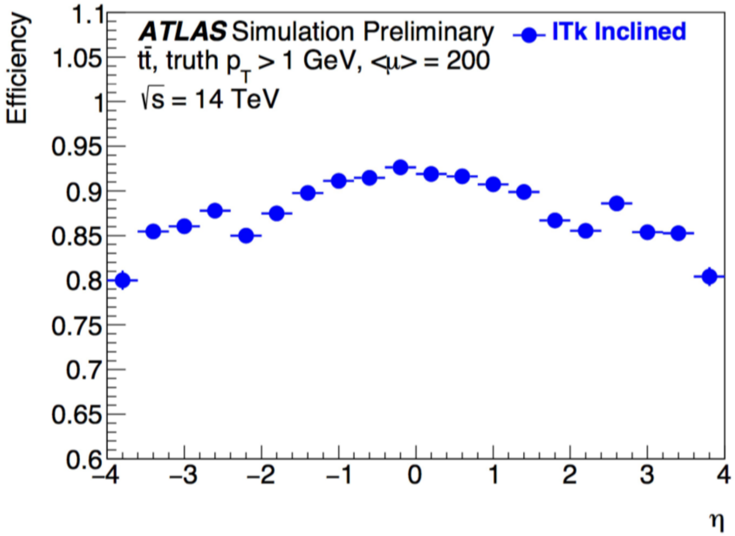


HL-LHC Tracker Performance

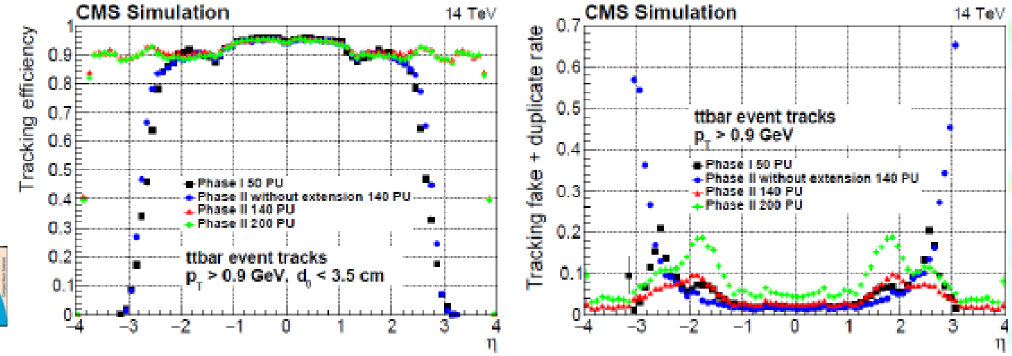
High Luminosity LHC

UNIVERSITY OF BIRMINGHAM

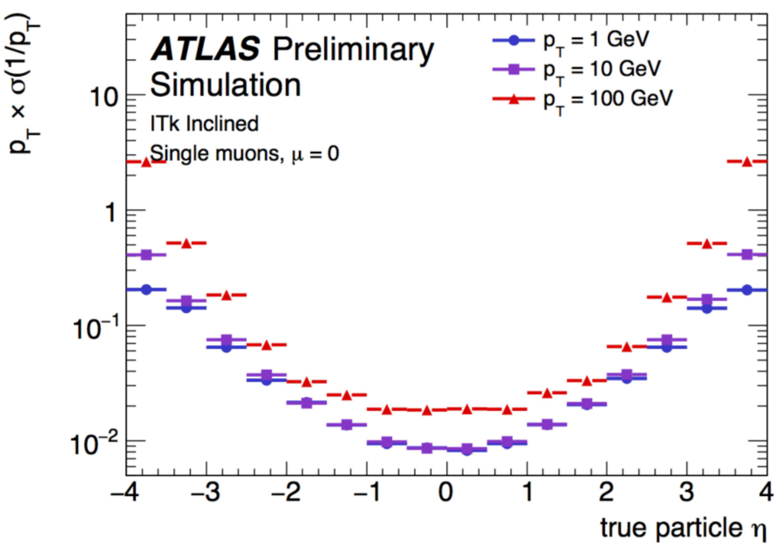
ATLAS EXPERIMENT

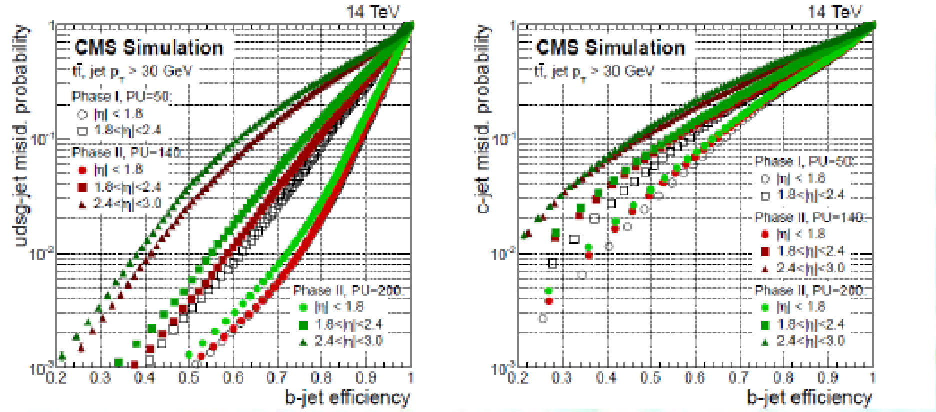


- $t\bar{t}$ events with 140 PU (●) and 200 PU (●)



- $t\bar{t}$ events with 140 PU (●■▲) and 200 PU (●■▲)

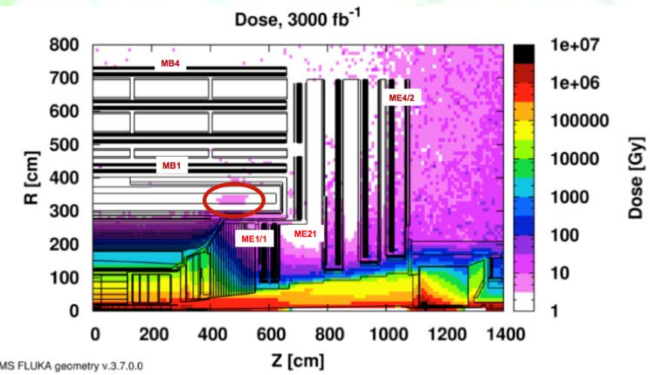




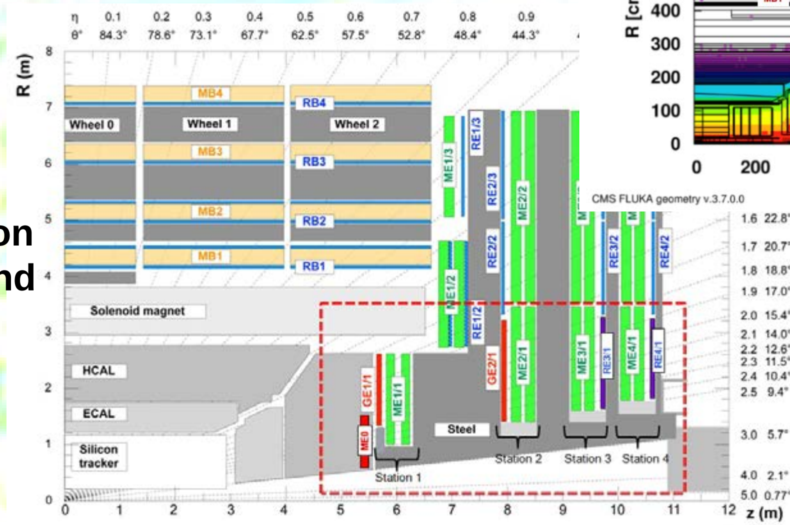
Many more performance studies and physics benchmark sensitivity results presented at the ECFA HL-LHC Workshop

Gaseous Tracking Detectors

- Electronics upgrades maintain performance of existing detectors
  - DT/CSC: cope with increased bandwidth and high L1 rate
- New forward muon detectors to improve trigger capabilities to match the new environment and increase offline coverage
  - GEM GE1/1 & 2/1 enable muon direction measurements
  - RPC RE3/1 & 4/1 improve redundancy in far stations
  - ME0 muon tracking and direction measurements for trigger, extend coverage η=2.4 ➔2.9



HL-LHC background 5x rates and 6x total doses with respect to LHC



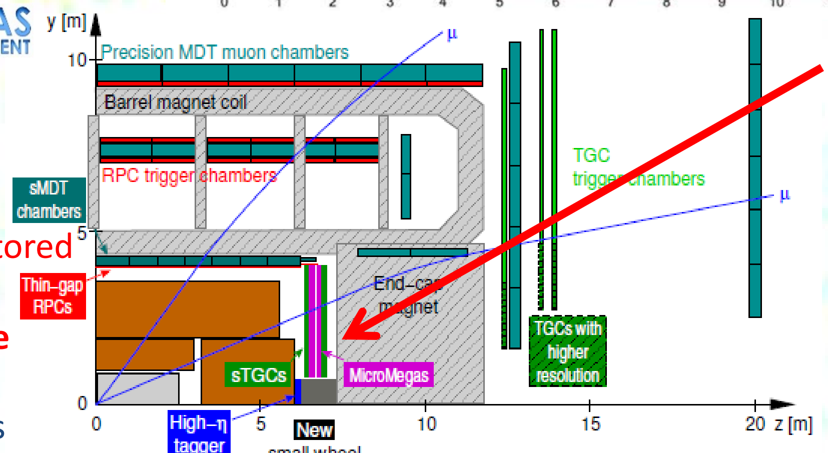
ATLAS: improve barrel muon trigger

by installing 276 additional RPC chambers in the inner barrel layer

- to close acceptance gaps and redundancy, in particular
- to compensate for potential efficiency loss of existing RPCs

by replacement of the 96 monitored drift tube (MDT) chambers by **small-diameter sMDT drift tube chambers**

to make space for the new RPCs and increase tracking rate capability



ATLAS: improve endcap muon tracking and trigger

New Small Wheels in the EI layer with high-resolution small-strip sTGC trigger chambers and Micromegas tracking detectors with increased rate capability in LS2 (2019-20)

Extension of the EI sTGC trigger chamber layer to larger radii in LS3 (2024-26) under consideration

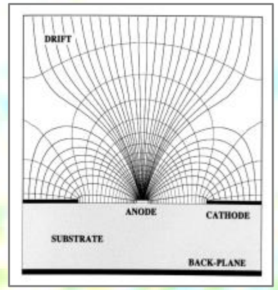
Gaseous Tracking Detectors

High Luminosity LHC

UNIVERSITY OF BIRMINGHAM

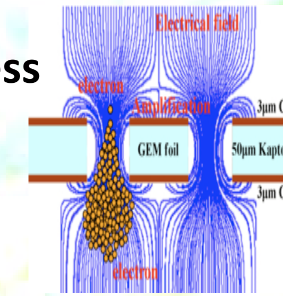
Main R&D activities for ATLAS and CMS are for new muon chambers in the forward directions.

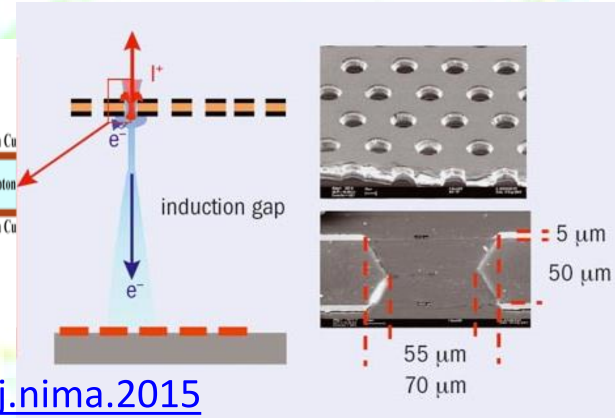
- Increase rate capabilities and radiation hardness
- Improved resolution (online trigger and offline analyses)
- Improved timing precision (background rejection)



Technologies

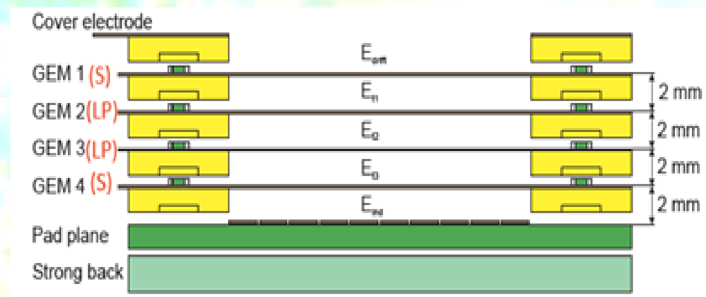
- Gas Electron Multiplier (CMS forward chambers, ALICE TPC and current LHCb)
- MicroMegas and Thin Gap Chambers (TGCs) (ATLAS forward chambers)
- Resistive Plate Chambers (RPCs) - low resistivity glass for rate capability - multi-gap precision timing (ATLAS/CMS)

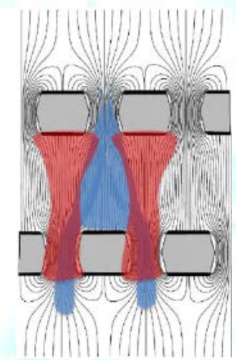




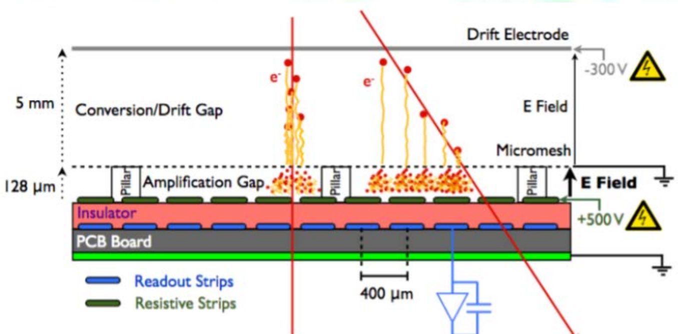
Fabio Sauli
doi:10.1016/j.nima.2015

GEM stack for ALICE TPC R/O.





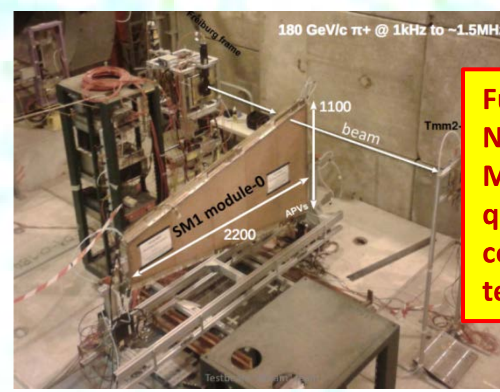
4 layer stack to target Ion backflow < 1% given continuous readout at 50kHz



MicroMegas Principle

CERN RD51 common micro-pattern gas detector R&D

Need to develop commercial large-scale production capabilities



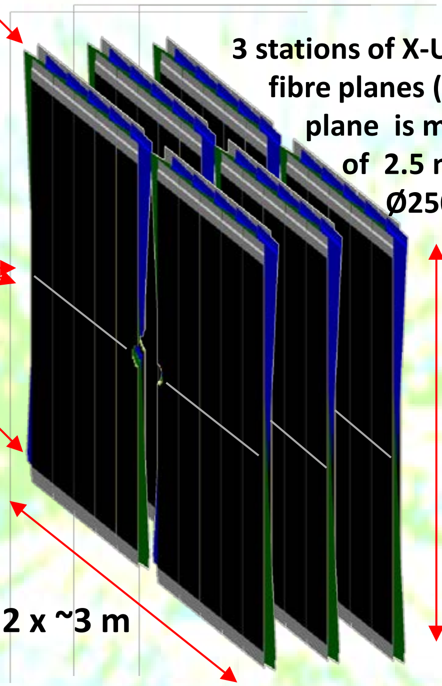
Full scale ATLAS New Small Wheel MicroMegas quadruplet completed and tested at CERN

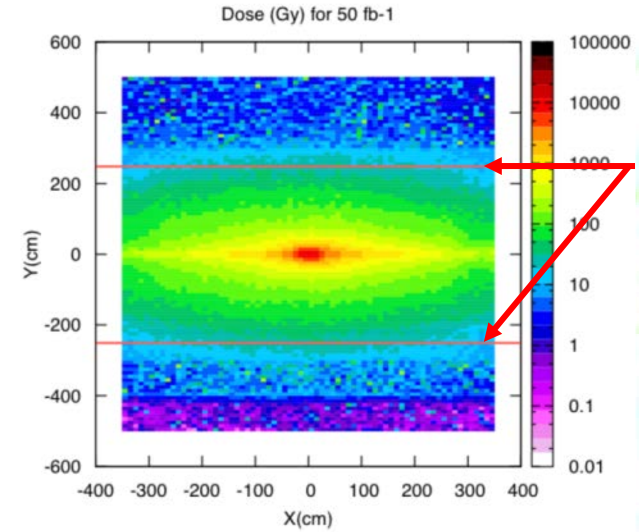
Scintillating Fibre Tracking

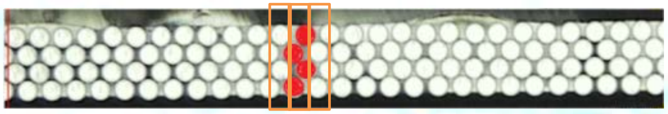
High Luminosity LHC

UNIVERSITY OF BIRMINGHAM

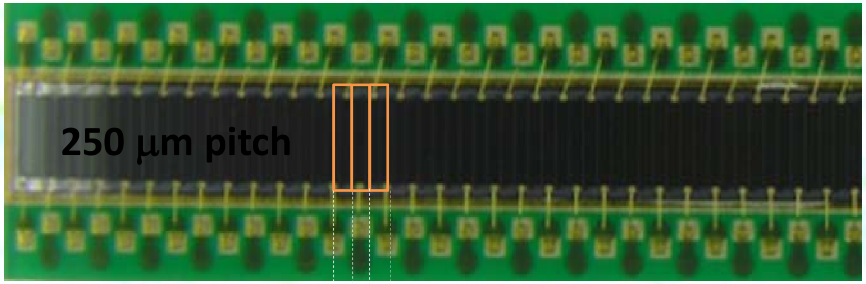
Large scale SciFi tracker for LHCb







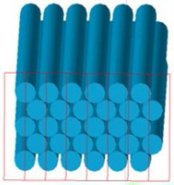
4 layer proto mat



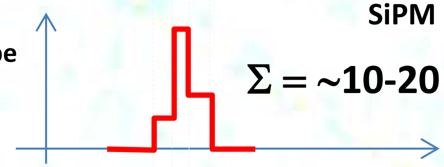
SiPM array (HPK)

Challenges

- Large size – high precision
- O(10,000 km) of fibres
- Operation of SiPM at -40°C



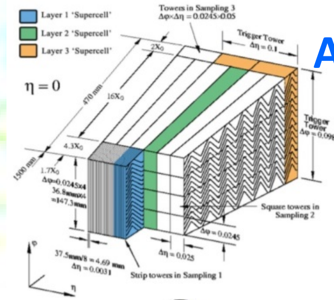
3 million (SCSF-78MJ TDR baseline) scintillating fibres with up to 30kGy non-uniform exposure (CERN/LHCC 2014-001)

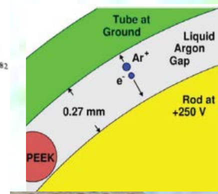


Calorimeter R&D

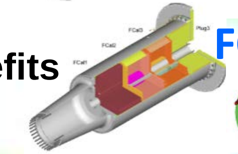
- **Major upgrades of HL-LHC calorimeter electronics to stream all data off detector at 40MHz to give ultimate trigger flexibility (GBT links)**
- **LAr excellent for radiation-hardness but granularity of read-out not optimised for HL-LHC conditions**
  - **ATLAS increased depth and segmentation (×10) inputs at Level-1 Phase-I upgrade (better benefit from intrinsic spatial resolution)**
  - **Studied new sFCal with smaller LAr gaps and tube diameters, but detailed benefit/risk assessment argued against this (despite benefits of finer pitch and concerns about loss of highest η efficiencies)**

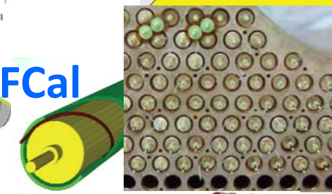
ATLAS LAr





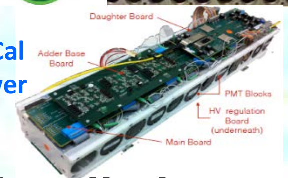
FCal





- **ATLAS Tile Calorimeter: replace HV, FE and BE electronics**

ATLAS TileCal Super-drawer

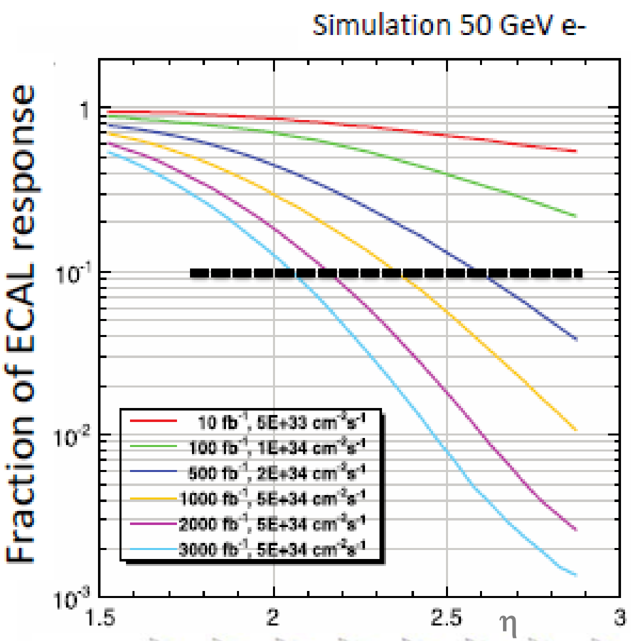


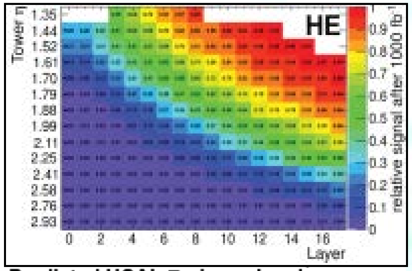
- **For other scintillator based systems, can have issues with light yield and transparency (also for wavelength shifting fibres) after irradiation**

→ **Crucial development is advanced commercial photo-detector technologies with high sensitivity, radiation tolerance, high granularity and low cost**

- **Major challenge for particle flow in calorimeters (very high granularity requirements over large areas) is cost optimisation plus need for extreme radiation hardness of all components in forward directions**

CMS: Forward Calorimeter

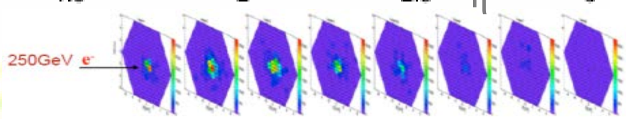


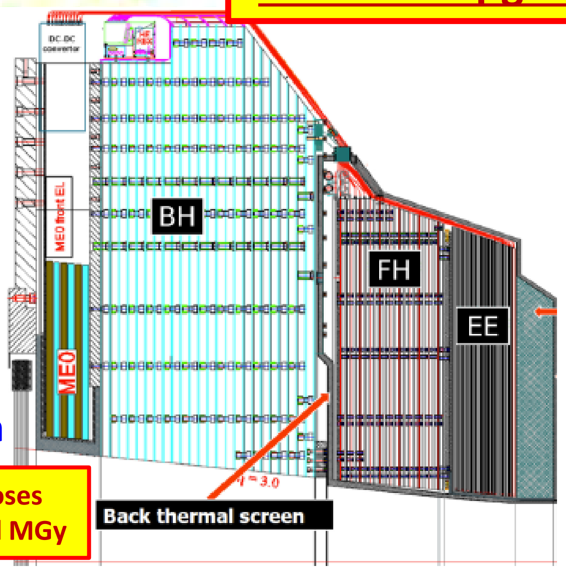


Predicted HCAL Endcap signal response after 1000fb^{-1} versus active layer and η

CMS need to replace ECAL and HCAL end-cap calorimeters due to radiation damage

CMS PFA Upgrade High Granularity Calorimeter





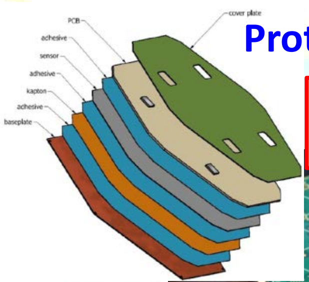
Construction:

- *Hexagonal Si-sensors built into modules.*
- *Modules with a W/Cu backing plate and PCB readout board.*
- *Modules mounted on copper cooling plates to make wedge-shaped cassettes.*
- *Cassettes inserted into absorber structures at integration site (CERN)*

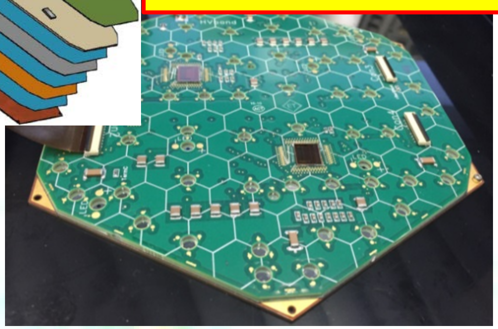
Key parameters:

- *593 m^2 of silicon*
- *6M ch, 0.5 or 1 cm^2 cell-size*
- *21,660 modules (8" or 2x6" sensors)*
- *92,000 front-end ASICS.*
- *Power at end of life 115 kW.*

Prototypes in test-beam



Silicon pads to withstand doses up to 10^{16}n/cm^2 and several MGy

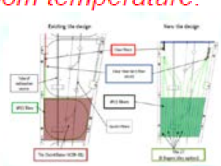


System Divided into three separate parts:

EE – Silicon with tungsten absorber – 28 sampling layers – 25 X_0 (~1.3 λ)
FH – Silicon with brass (now stainless steel) absorber – 12 sampling layers – 3.5 λ
BH – Scintillator with brass absorber – 11 layers – 5.5 λ

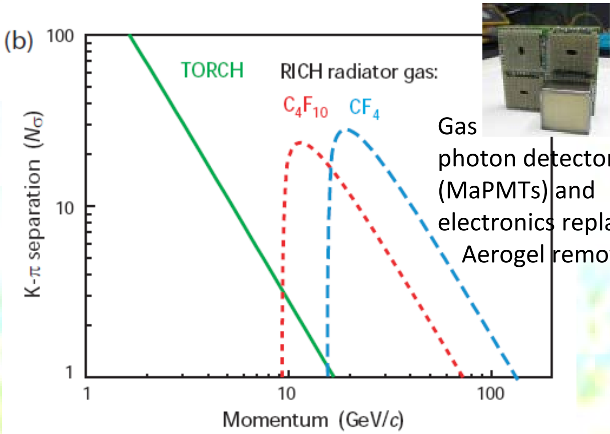
EE and FH are maintained at – 30^{0}C. BH is at room temperature.

e/γ resolution ~20%/$\sqrt{E}$ + ≤ 1%



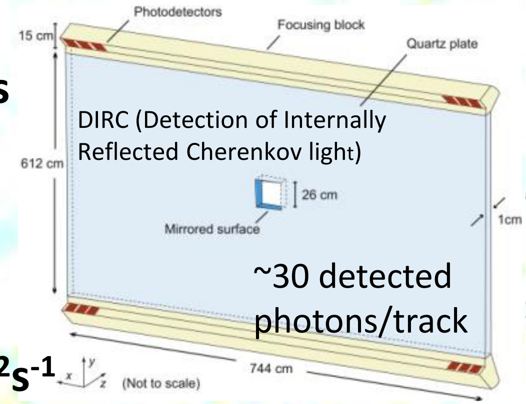
Scintillator-based HCAL with 30% of volume replaced by finger tiles to reduce optical path and attenuation

Particle ID and Timing

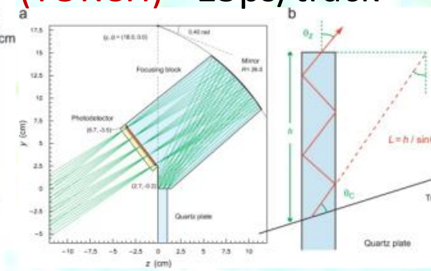


Gas photon detectors (MaPMTs) and electronics replaced. Aerogel removed.

LHCb RICH system needs upgrades for triggerless operation at higher rates: $\mathcal{L}=2\times10^{33}\mathrm{cm^{-2}s^{-1}}$

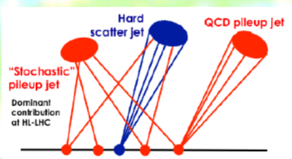


LHCb Time Of internally Reflected CHerenkov (TORCH) ~15ps/track

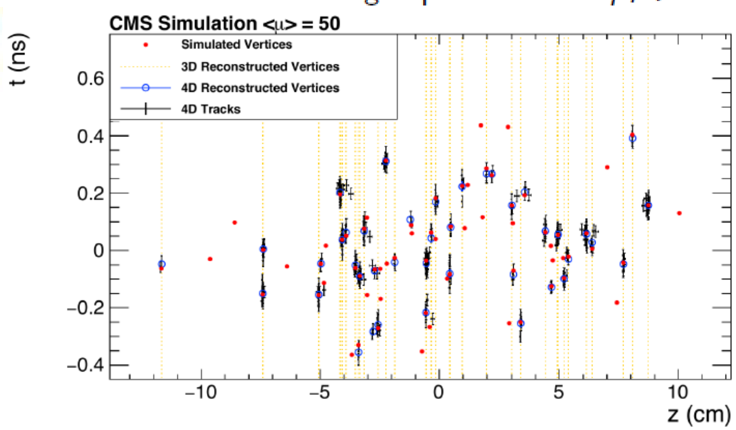


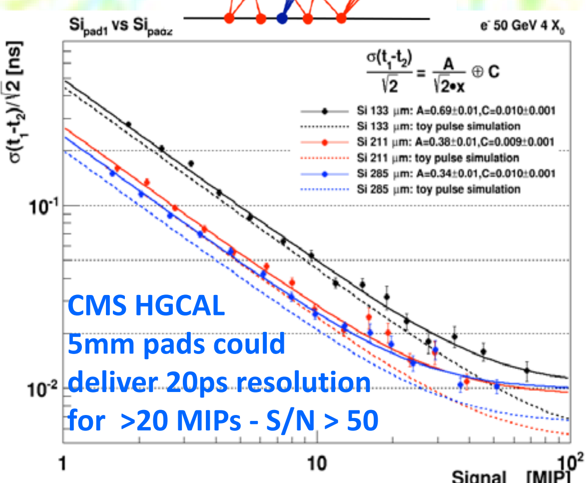
For 200 PU, depending on crossing scheme, HL-LHC can deliver down to an event/mm and up to 1.45ns bunch crossing duration

→ Use 20-30ps timing to better associate high p_T objects to vertices



20 ps resolution assumed for charged particles with $p_T > 1$ GeV

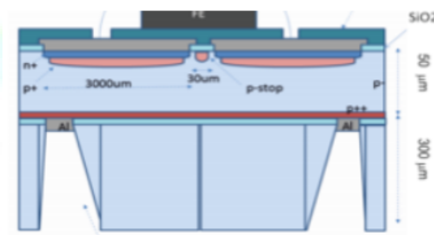




CMS HGCAL 5mm pads could deliver 20ps resolution for >20 MIPs - S/N > 50

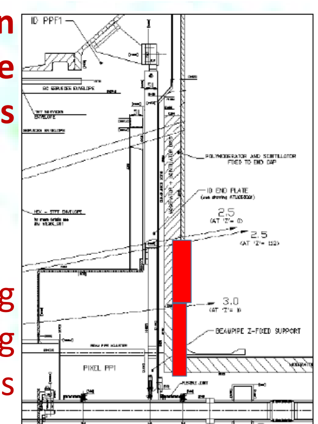
Requirements:

- time resolution =30-50 ps/mip
- Radiation tolerance to 10^{15}-10^{16}n/cm^2



RD50

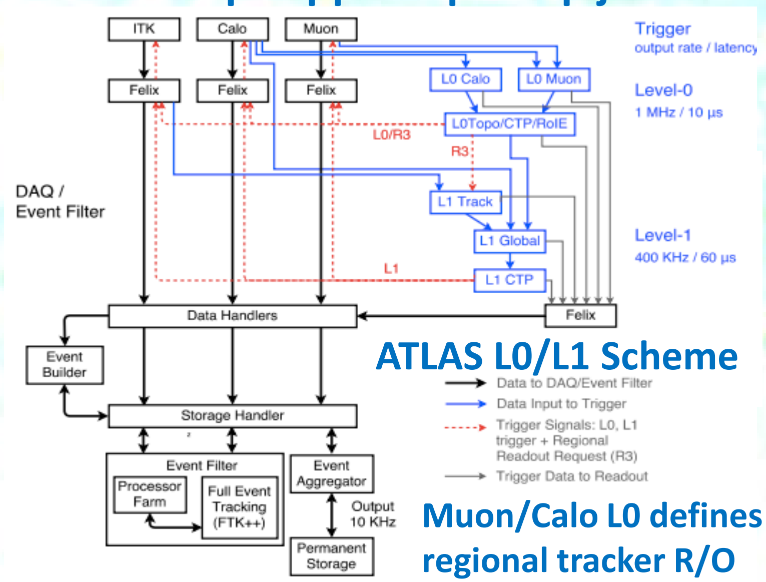
Low Gain Avalanche Detectors



ATLAS propose dedicated **H**igh **G**ranularity SiW **T**iming **D**etector in front of end-cap at z=3500mm, covering 2.4<η<4.2 (650mm>r>110mm) 50μm thick few mm² pads

HL-LHC R/O and TDAQ

- Use of 65nm feature size ASICs for ~10Gb/s electrical+optical links based on custom devices on-detector (low mass, compact and radiation-hard)
- Also need ever more powerful and more complex FPGAs for data handling
- Where possible send digitized data off-detector for every bunch crossing (ie at 40MHz) leading to total bandwidths ~10^5 Gb/s
- LHCb full triggerless (40MHz) operation, all data shipped to data acquisition
- HL-LHC operation 6-8 × 10^9 interactions per second in 25ns bunch crossings
- ATLAS & CMS hardware (L1) trigger → maintain low trigger thresholds
  - Track information for high momentum resolution - isolation - vertexing
    → can reduce rates of lepton triggers by a factor ~ 10 and help suppress pile-up jets
  - ATLAS: either L0/L1 (could allow L0 above a MHz if needed) or L0 only at 1MHz
  - CMS: ~750kHz L1 with tracking information
  - Increased L1 latency 10 - 30 µs
  - Improved algorithms
  - R&D on improved pattern recognition Associative Memories ASICs and advanced FPGAs to achieve fast track fitting for L1

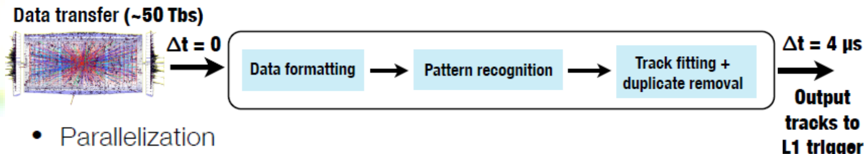


ATLAS L0/L1 Scheme

Muon/Calo L0 defines regional tracker R/O

HL-LHC R/O and TDAQ

- Use of 65nm feature size ASICs for ~10Gb/s electrical+optical links based on custom devices on-detector (low mass, compact and radiation-hard)
- Also need ever more powerful and more complex FPGAs for data handling
- Where possible send digitized data off-detector for every bunch crossing (ie at 40MHz) leading to total bandwidths ~10^5 Gb/s
- LHCb full triggerless (40MHz) operation, all data shipped to data acquisition
- HL-LHC operation 6-8 × 10^9 interactions per second in 25ns bunch crossings
- ATLAS & CMS hardware (L1) trigger → maintain low trigger thresholds
  - Track information for high momentum resolution - isolation - vertexing
    → can reduce rates of lepton triggers by a factor ~ 10 and help suppress pile-up jets
  - ATLAS: either L0/L1 (could allow L0 above a MHz if needed) or L0 only at 1MHz
  - CMS: ~750kHz L1 with tracking information
  - Increased L1 latency 10 - 30 µs
  - Improved algorithms
  - R&D on improved pattern recognition Associative Memories ASICs and advanced FPGAs to achieve fast track fitting for L1



- Parallelization
  - Divide tracker in segments in ϕ / z
  - Time-multiplexed systems -- process several BX simultaneously
- Different approaches to attack combinatorics & occupancies
  - Tracklet road search algorithm with full hit precision
  - Hough transform with large time-multiplexing

  Fully FPGA based
  - ✓ Off-the-shelf hardware
  - ✓ Programmable --> flexible systems
  - ✓ Must fit within FPGA resources & latency

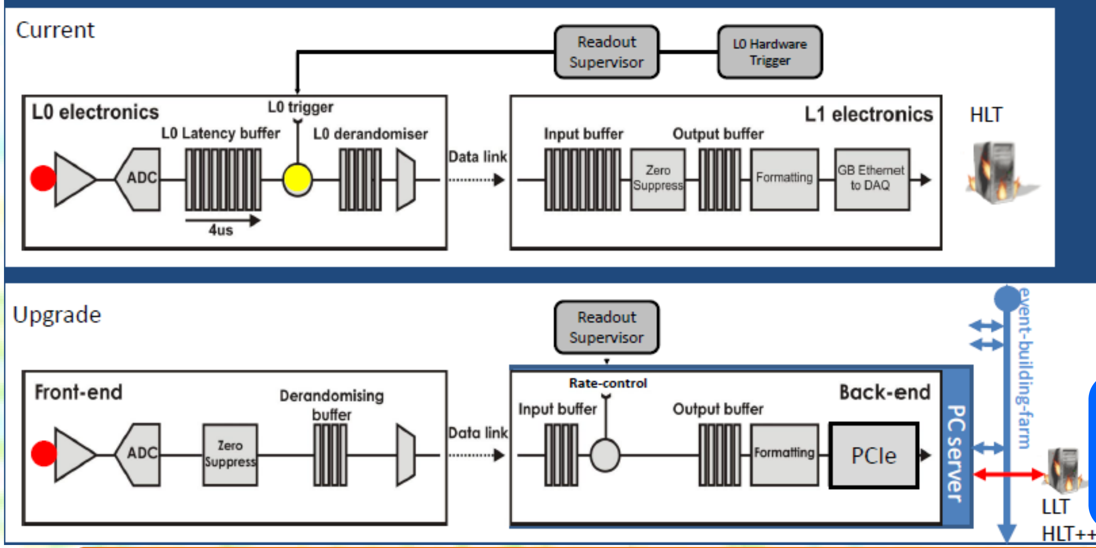
  - Associative memory (AM) pattern recognition (+ FPGA)

  AM assisted
  - ✓ Previous used (CDF & ATLAS FTK) but lower rates + longer latency
  - ✓ Requires custom ASICs

HL-LHC R/O and TDAQ

- **LHCb full triggerless (40MHz) operation, all data shipped to data acquisition**

No ‘front-end’ trigger, Event rate to DAQ nominally 40 MHz

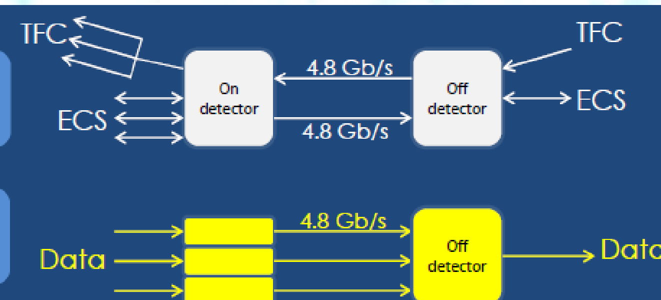


Data compression on Front-end driven by link cost:
Need ~ 15,000 links (4.8 Gbit/s)

Try to be flexible & scalable: 4 of 6 sub-detectors will use FPGAs in front-ends

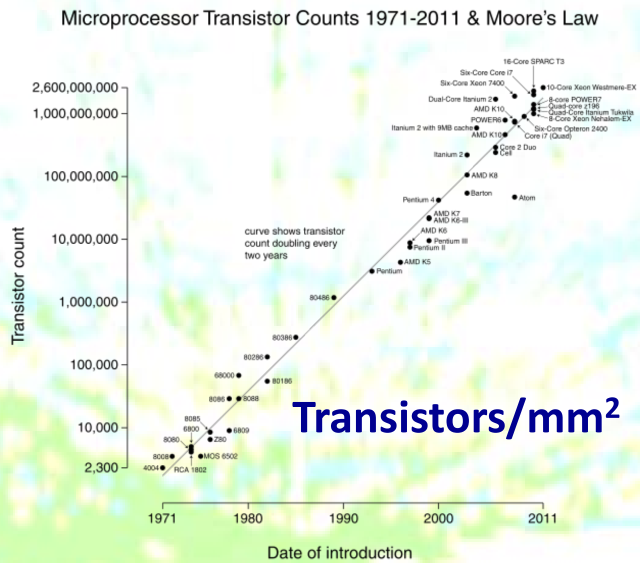
Combine slow & fast controls (ECS & TFC) in duplex links

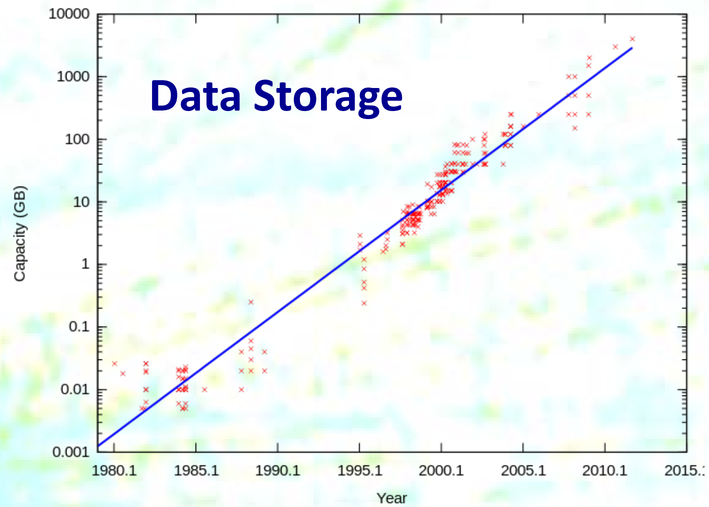
Simplex data links

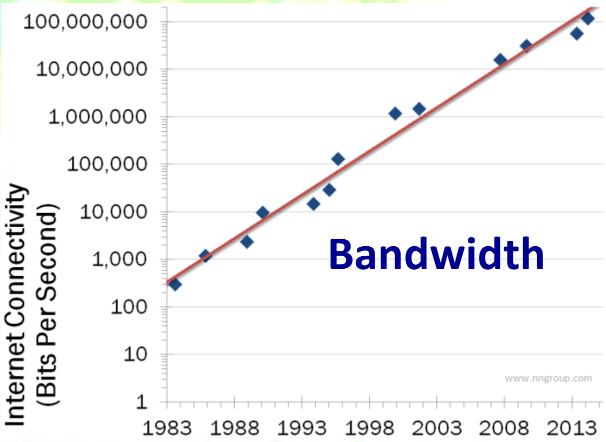


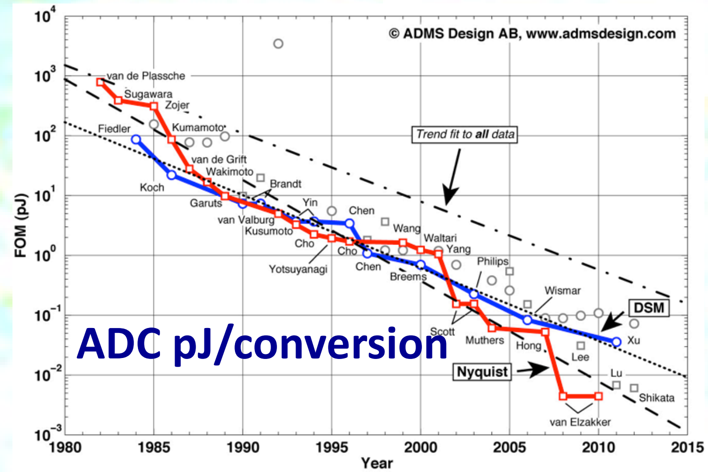
Baseline choice for backend electronics is PCIe format

Microelectronics Evolution



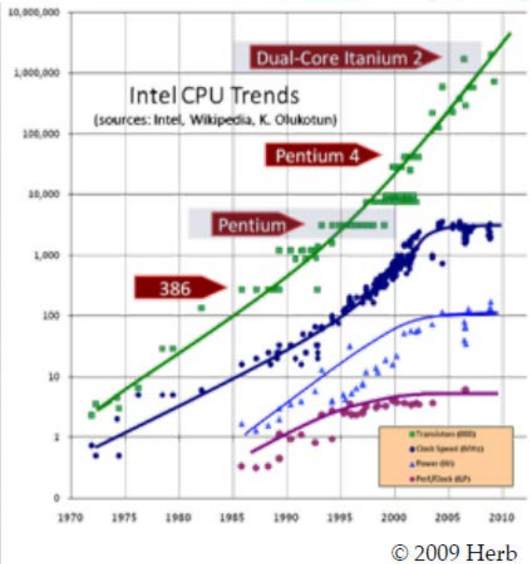




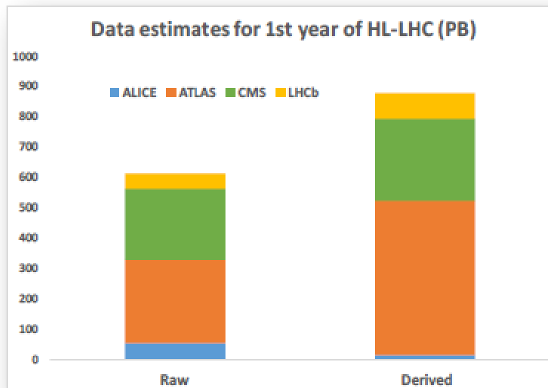


All these figures showed doubling times of < 2 years up to now. Some scalings will stop, but different improvements conceivable. Can still hope for major detector improvements and enhanced TDAQ plus computing capabilities. However, storage and CPU costs not expected to scale as fast as needed.

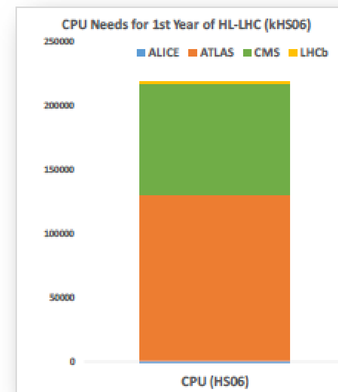
The Computing Challenge



The available transistors are used for **adding new CPU cores** while keeping the clock frequency basically constant, thus limiting the power consumption



Storage
Raw 2016: 50 PB → 2027: 600 PB
Derived (1 copy): 2016: 80 PB → 2027: 900 PB



CPU
x60 from 2016

Have to **introduce parallelism** into applications to fully exploit the continuing exponential CPU throughput gains

Some LHC software more than 20 years old
- Need to exploit modern hardware (many-core, GPU, etc.) to boost performance
- Need to modernize implementations

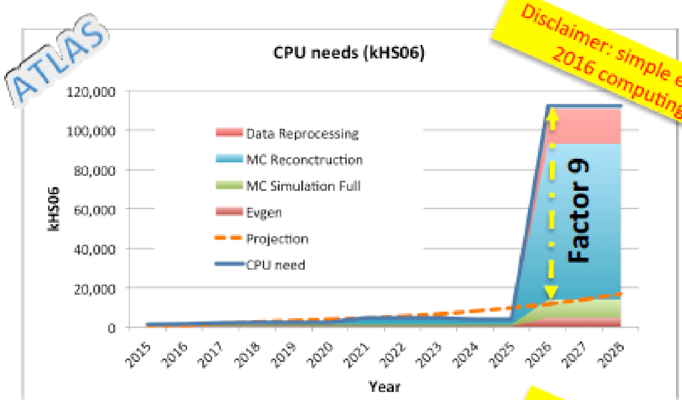
Technology at ~20%/year will bring **x6-10** in 10-11 years

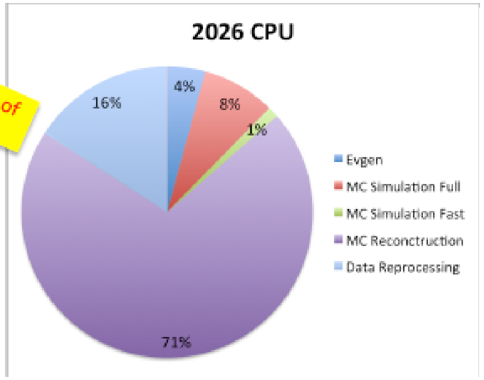
=> x10 above what is realistic to expect from technology with constant cost

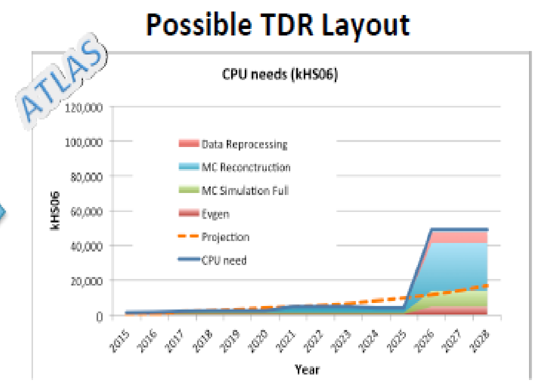
All these figures showed doubling times of < 2 years up to now. Some scalings will stop, but different improvements conceivable. Can still hope for major detector improvements and enhanced TDAQ plus computing capabilities. However, storage and CPU costs not expected to scale as fast as needed.

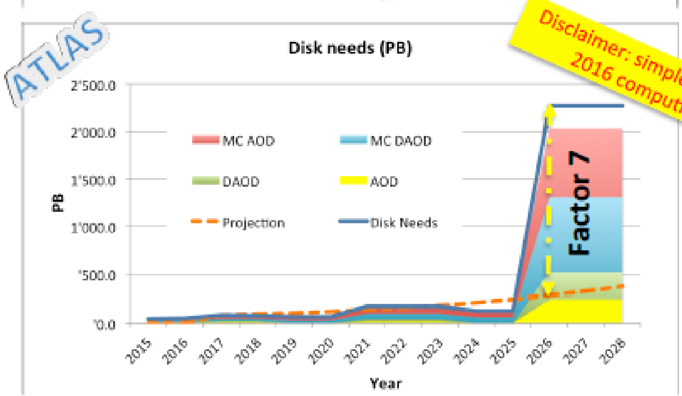
The Computing Challenge

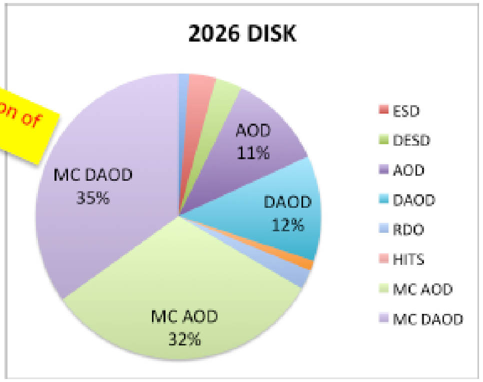
HL-LHC baseline resource needs











- Reconstruction time dominates CPU consumption at HL-LHC
- Optimised detector layout can significantly reduce this
- Needs to become a factor in detector design

All these figures showed doubling times of < 2 years up to now. Some scalings will stop, but different improvements conceivable. Can still hope for major detector improvements and enhanced TDAQ plus computing capabilities. **However, storage and CPU costs not expected to scale as fast as needed.**

Conclusions

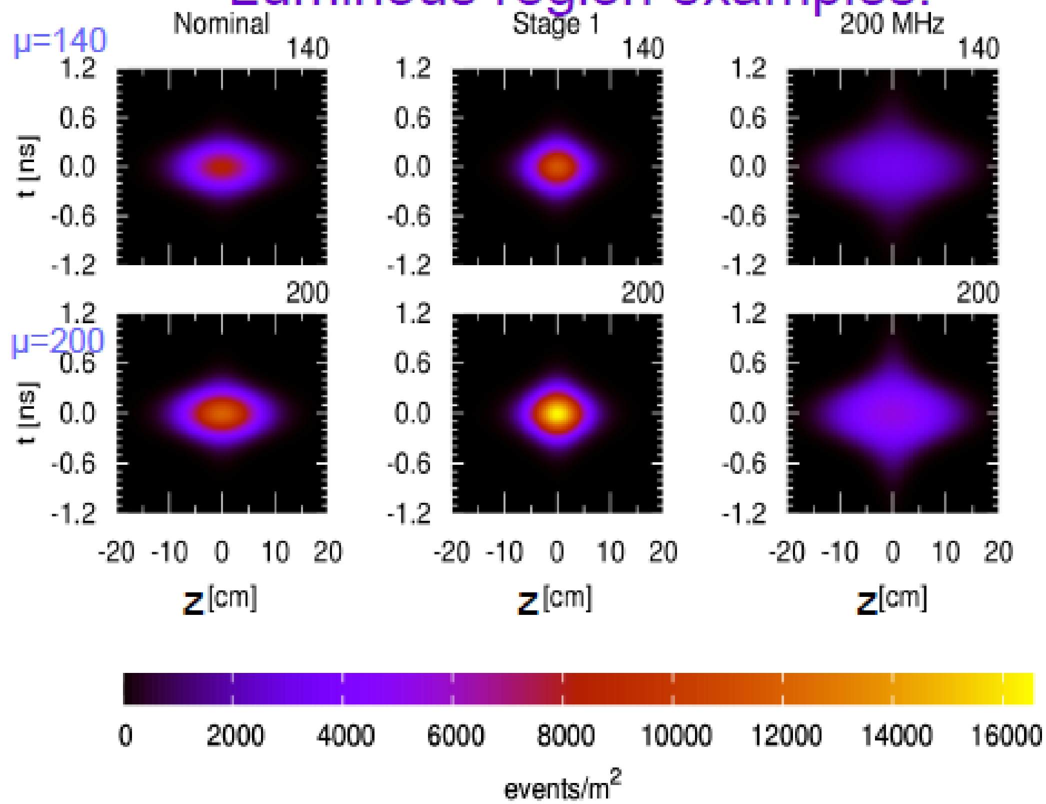
- Many new results on performance and physics reach presented at ECFA HL-LHC (https://indico.cern.ch/event/524795/timetable/) for which there has not been time to present, nor the latest accelerator developments, interface to detectors and experiment schedules
- For lack of time, progress on Phase-I upgrade preparation has largely been omitted but this represents a huge international effort
- Failed to do justice to many aspects of detector R&D, along with developments in electronics, data acquisition, monitoring, alignment, global engineering, radiation protection …
- Focus has been mainly on areas with more direct contact so many apologies also for omissions and, in particular, any errors
- Progress with detector technology is in general keeping pace with the requirements from the machine schedule but resources are an issue despite good coordination of efforts between experiments
- Sizeable and highly dedicated community engaged in detector R&D for upgrade of LHC experiments for the challenges of the HL-LHC

BACK-UP

Luminous Region

- Complex set of machine parameters define luminous region (β*, bunch length, crossing angle, etc.)
- Experiments just see spatial and temporal distribution and the evolution within fill
  - Transverse distribution not a concern as is small
  - Most detectors blind to spread in time (<1ns), but precision timing detector under evaluation
  - Primary concern is pile-up density in z (events per mm) and overall pile-up level
- Note: luminous region is not always Gaussian shaped

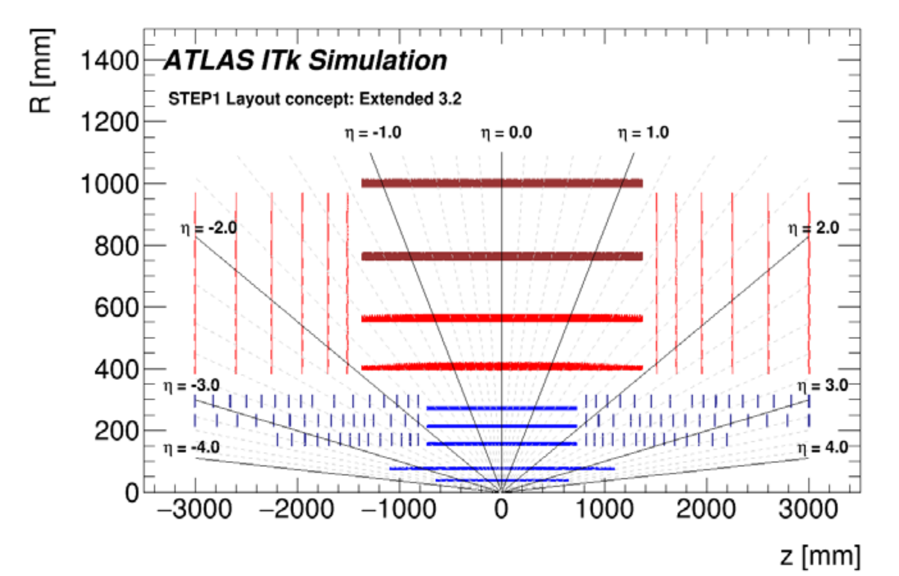
Luminous region examples:

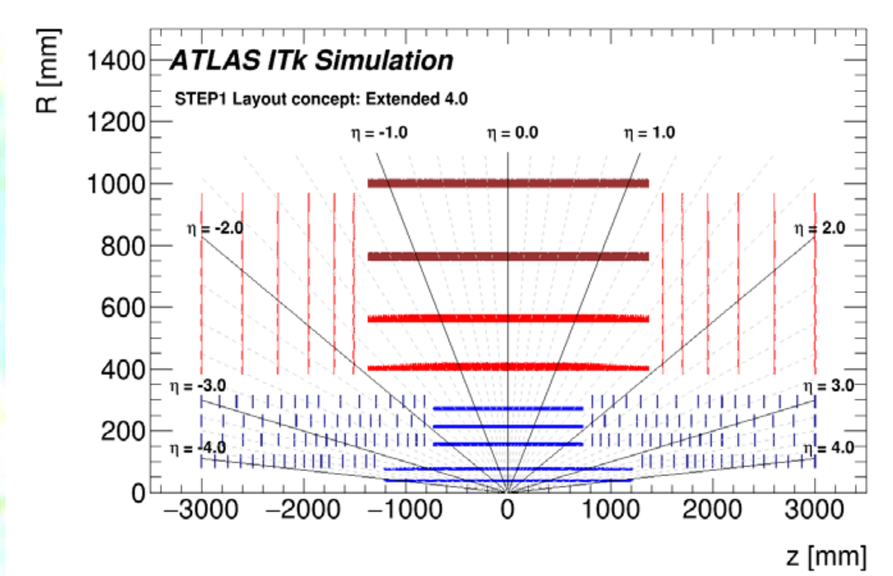


Phase-II Tracker Upgrade (ITk)

New All Silicon Inner Detector

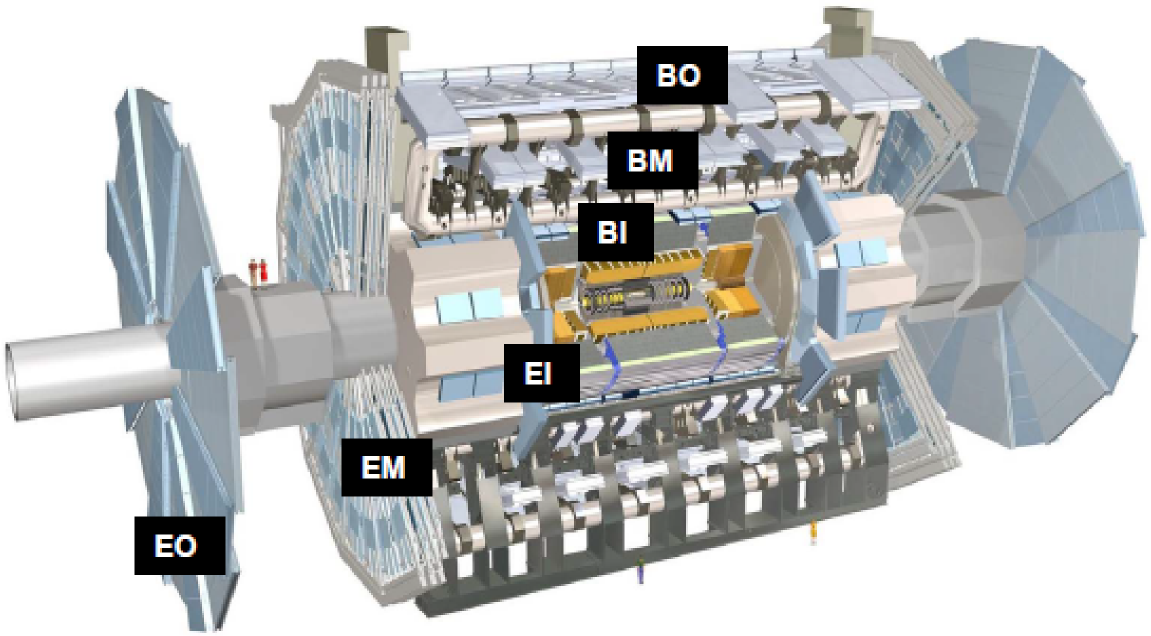
Recent baseline change from 5 paired strip layers (paired for 40mrad stereo) plus 4 pixel layers to 5 pixel and 4 strip layers (barrel) with 345mm radius boundary between the two systems.
→ Large area of pixel system particularly at high radii where radiation levels are less extreme.





Several layouts are under consideration including (not shown here) pixel layers with inclined sensors. The main differences in the ATLAS Phase-II Upgrade Scoping Document (CERN-LHCC-2015-020 ; LHCC-G-166) were in terms of the η coverage of the tracker which relates to the area of the pixel system ranging from ~13m^2 to ~16m^2.

ATLAS Muon Spectrometer



- About 1200 Monitored Drift Tube (MDT) precision tracking chambers with in total 140k drift tubes: sense wire positioning accuracy of 20 µm and chamber spatial resolution of 40 µm.

Track sagitta measurement in 3 detector layers.
Optical alignment system with 30 µm sagitta correction accuracy.

- Combined with 600 RPC (double gas gaps, barrel BM, BO) and 3600 TGC (endcaps) trigger chambers for L1 muon trigger, BCID and 2nd coord.measurement (< 10 ns time and order cm spatial resolution).

High neutron and gamma background rates:
up to 400 Hz/cm^2 in EI MDTs at LHC design luminosity.

About 7 x higher background rates expected at HL-LHC, as well as much increased muon trigger rate.

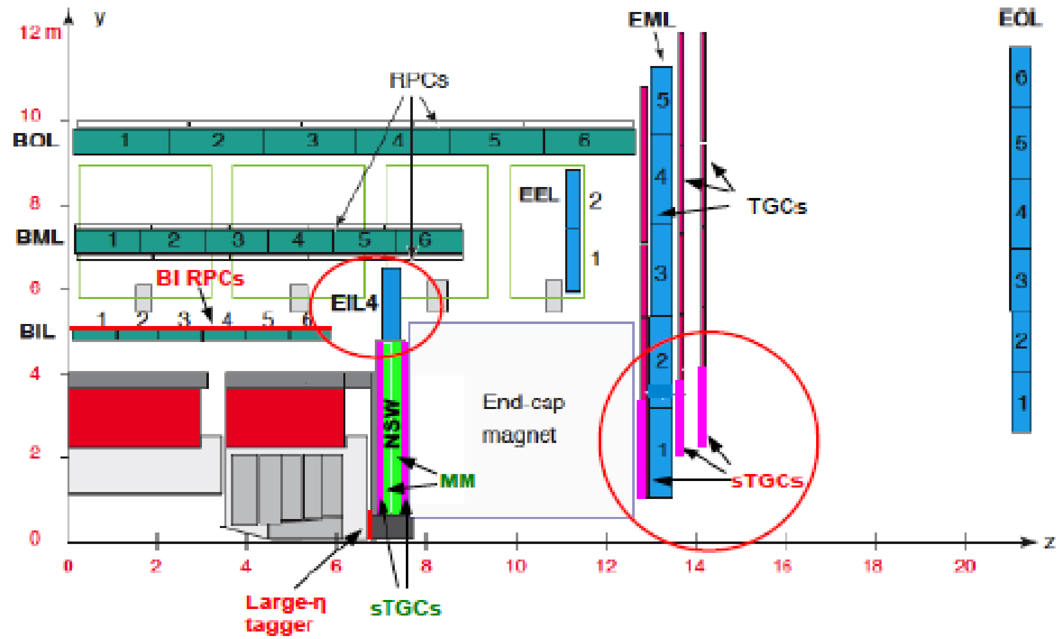
Replacement of TGC chambers

TGC rate capability is sufficient for HL-LHC

Two options under study.

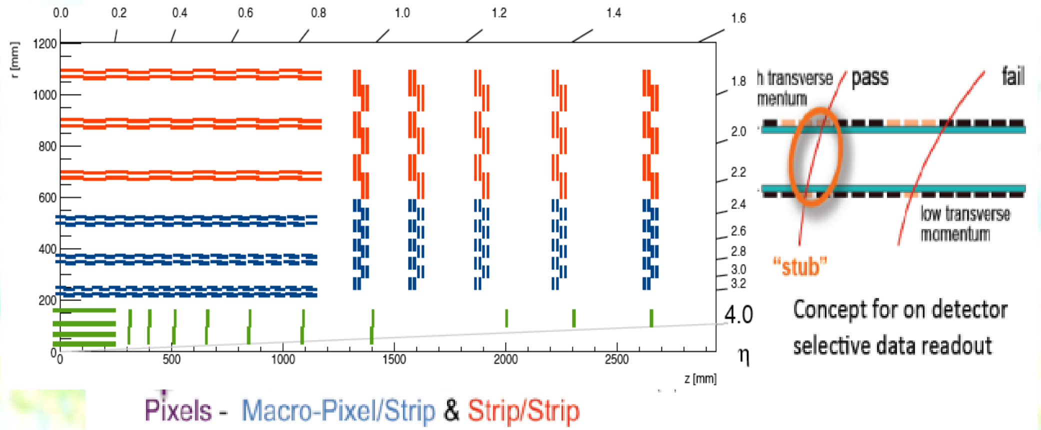
1) from LoI, Scoping Doc.:
   Replacement of inner ring of "Big Wheel" with TGCs (sTGCs) with Improved spatial resolution

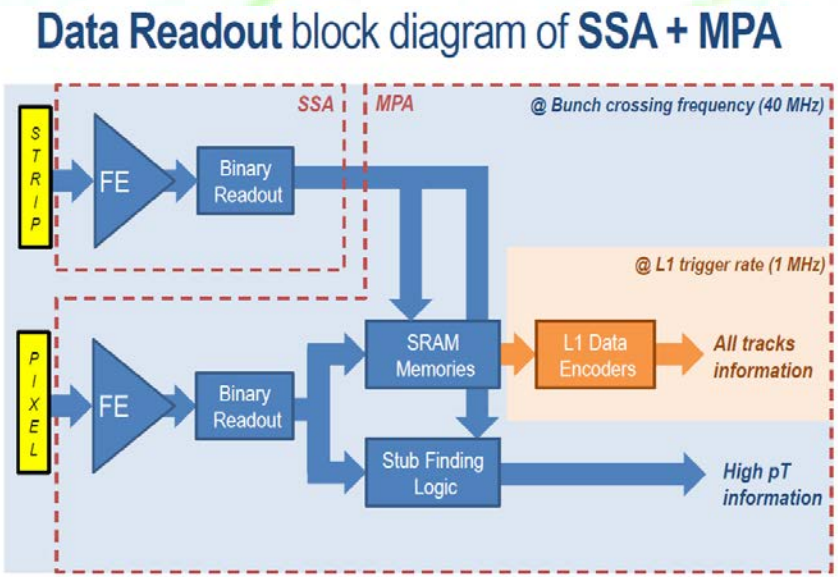
   Main goal is improve trigger selectivity in forward region. From latest studies it may not be necessary

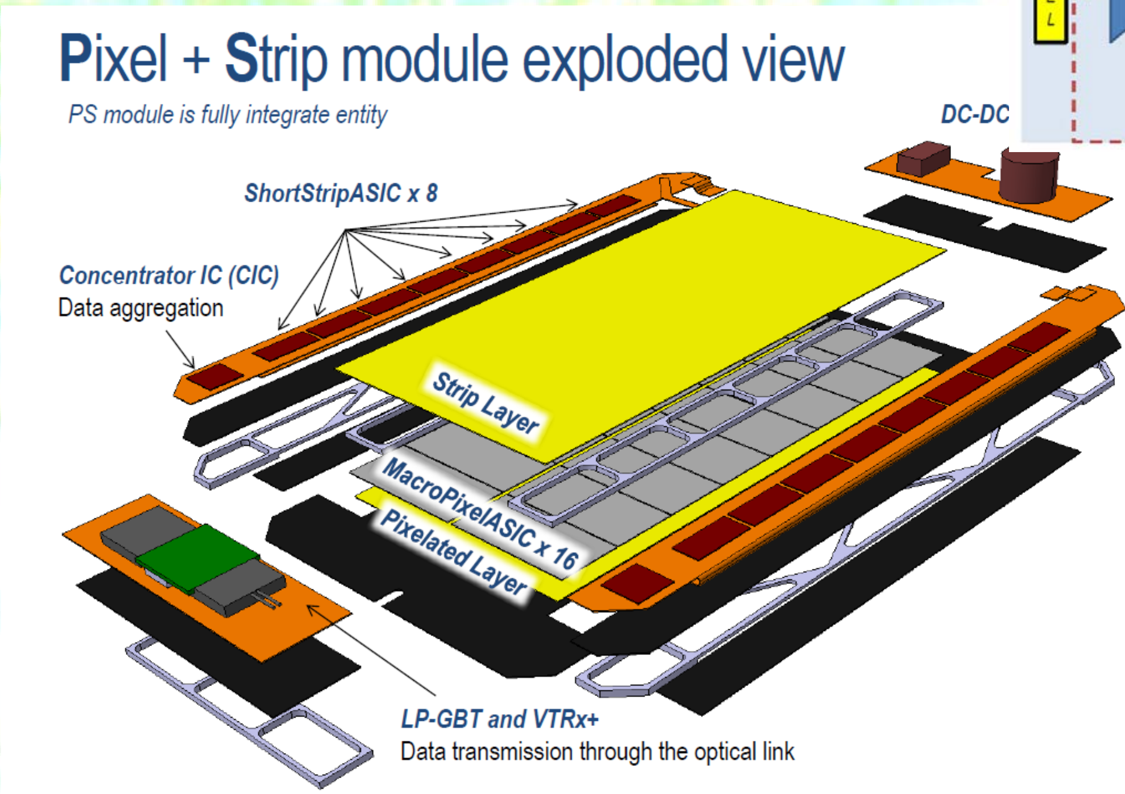


2) EIL4 chambers,
   $1<|\eta|<1.3$ only on "large" ϕ sectors.
   Currently only one TGC doublet, with coarse resolution in trigger readout:
   Trigger with weak inner-plane coincidence.
   Proposal to replace with triplet with better granularity to improve the trigger selectivity.
   Would bring to same level of fake rejection as in NSW and in "small" sectors (BIS78).

CMS: Strip-Pixel Module

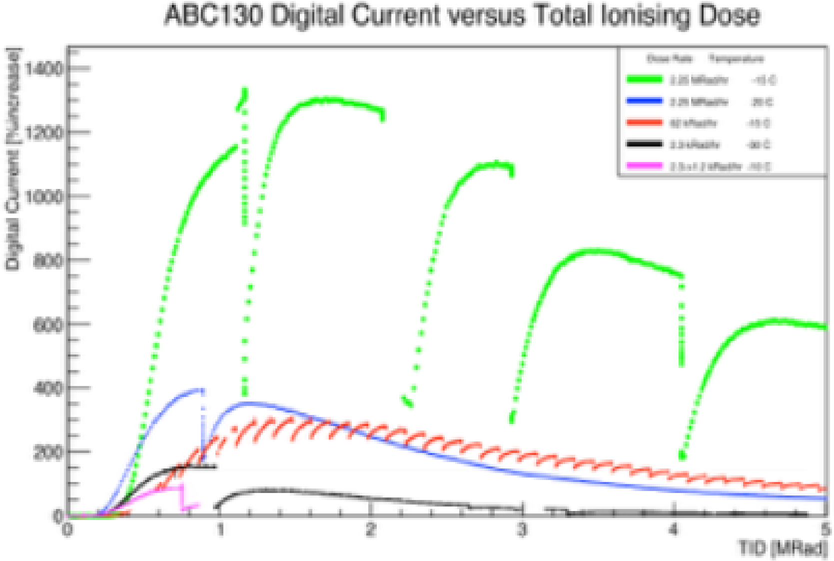






Could the functionality of these modules benefit from CMOS technology to replace the macro-pixel layers?

Radiation Studies FE-chips

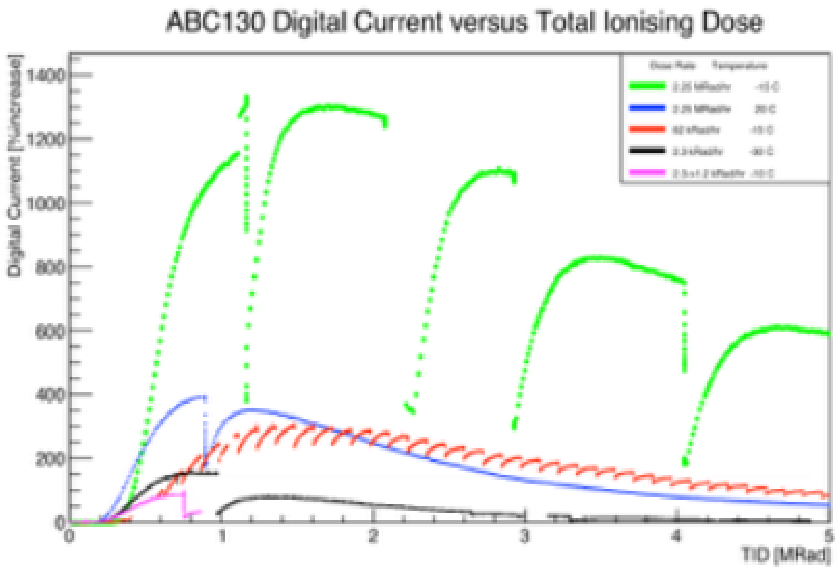


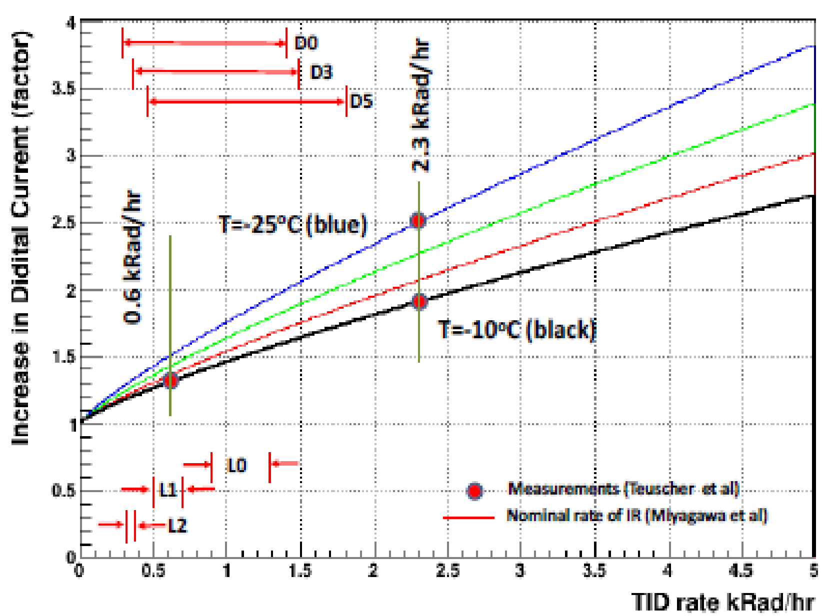
Source	T (C)	Current Increase Factor	Dose Rate (MRad/h)
Co-60 CERN	-25	2.5	0,0023
Co-60 CERN	-10	1.9	0,0023
Co-60 CERN	-10	1.3	0,0006
x-ray CERN	-15	3.9	0,062
x-ray CERN	-15	13.6	2,25
x-ray CERN	+20	5.2	2,25
Birmingham-p	-25	9.7	1,25

- Studies at various facilities with different dose types, rates and environmental conditions with FE-chip ABC130.
  - Increase in noise up to ~10 MRad
  - Small O(1%) decrease in gain recovering at high doses
  - Current peak induced by TID at 1MRad
    - Effect depending on dose rate and temperature.

- Load on cooling/power at large object level have been calculated.
- Improved design of front-end chip to reduce impact of total ionising dose.
- Mitigate impact of increased current by designing powering and cooling appropriately.

Radiation Studies FE-chips



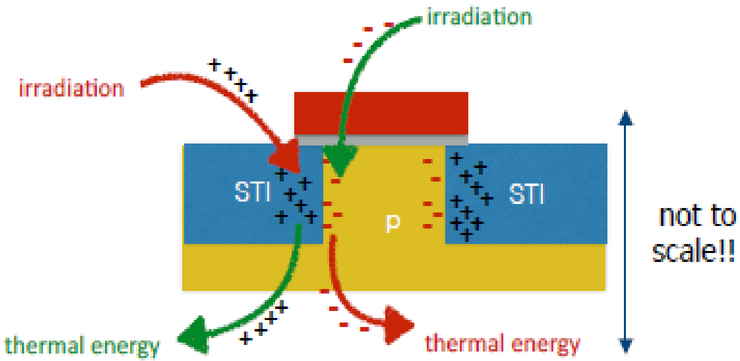


- Studies at various facilities with different dose types, rates and environmental conditions with FE-chip ABC130.
  - Increase in noise up to ~10 MRad
  - Small O(1%) decrease in gain recovering at high doses
  - Current peak induced by TID at 1MRad
    - Effect depending on dose rate and temperature.

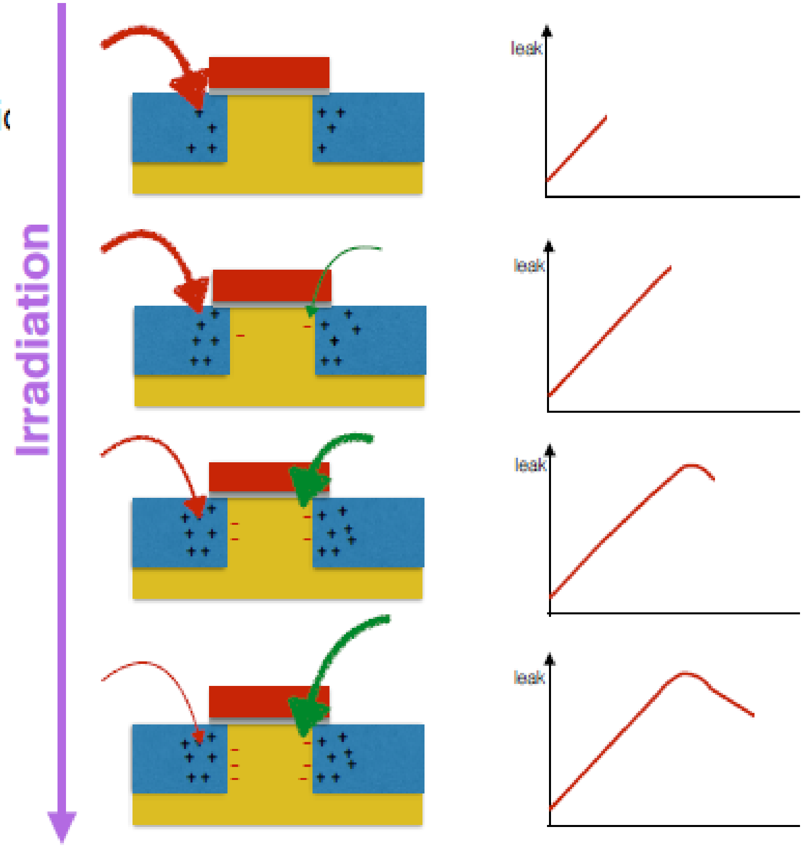
- Load on cooling/power at large object level have been calculated.
- Improved design of front-end chip to reduce impact of total ionising dose.
- Mitigate impact of increased current by designing powering and cooling appropriately.

TID Current Increase

Surface effects: Generation of charge traps due to ionizing energy loss (Total ionising dose, TID) **(main problem for electronics).**



- The leakage current is the sum of different mechanisms involving:
  - the creation/trapping of charge (by radiation)
  - its passivation/de-trapping (by thermal excitati
- These phenomena are dose rate and temperature dependent!
- Charge trapped in the STI oxide
  - +Q charge
  - Fast creation
  - Annealing already at T_{amb}
- Interface states at STI-Silicon interface
  - -Q for NMOS, +Q for PMOS
  - Slow creation
  - Annealing starts at 80-100C



STI = shallow trench interface

RD53 (65nm ASIC) Status

UNIVERSITY OF BIRMINGHAM

Radiation hardness issues in 130nm and 65nm CMOS

ACES 2016

F.Faccio

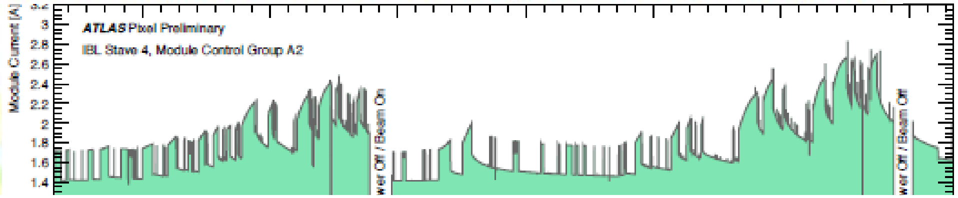
CERN - EP/ESE

The charge trapped in the lateral STI can also influence the characteristics of the main transistor - more evidently if it is narrow.

This has been called Radiation Induced Narrow Channel Effect (RINCE)

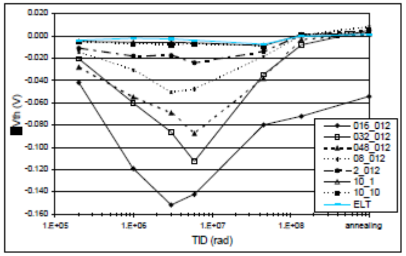
"RINCE" introduced at NSREC 2005 (F.Faccio and G.Cervelli, "Radiation induced edge effects in deep submicron CMOS transistors", IEEE Trans Nucl Science, Vol.52, N.6, Dec2005, pp.2413-2420)

… and current consumption in the ATLAS IBL in the experiment during data acquisition

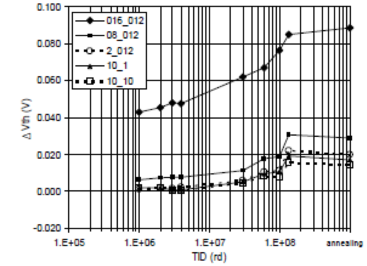


Example: apparent Vth shift in NMOS and PMOS transistors of different W, Tech. A

NMOS



PMOS



130nm

2 Technologies available for ASIC design

- **The present streamline is recommended for all new designs, it appears good for the targeted TID levels**

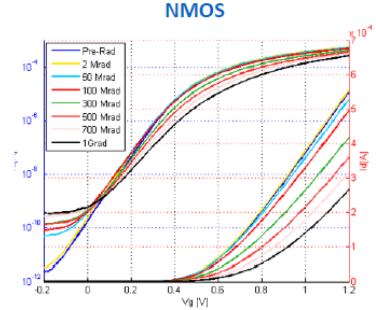
RISCE: Short channel PMOS are more damaged than NMOS

Damage occurs also in ELT transistors, hence it can not be due to the STI oxide

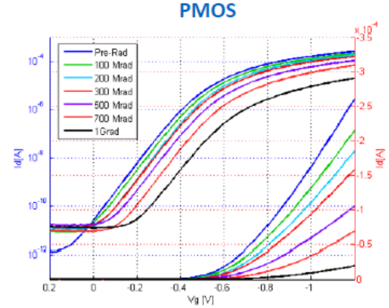
65nm

Short and narrow channel radiation-induced effects are strong (RINCE, RISCE). These are complex and make the choice of a qualification procedure and of appropriate design margins difficult, in particular for digital design

NMOS



PMOS



all processes

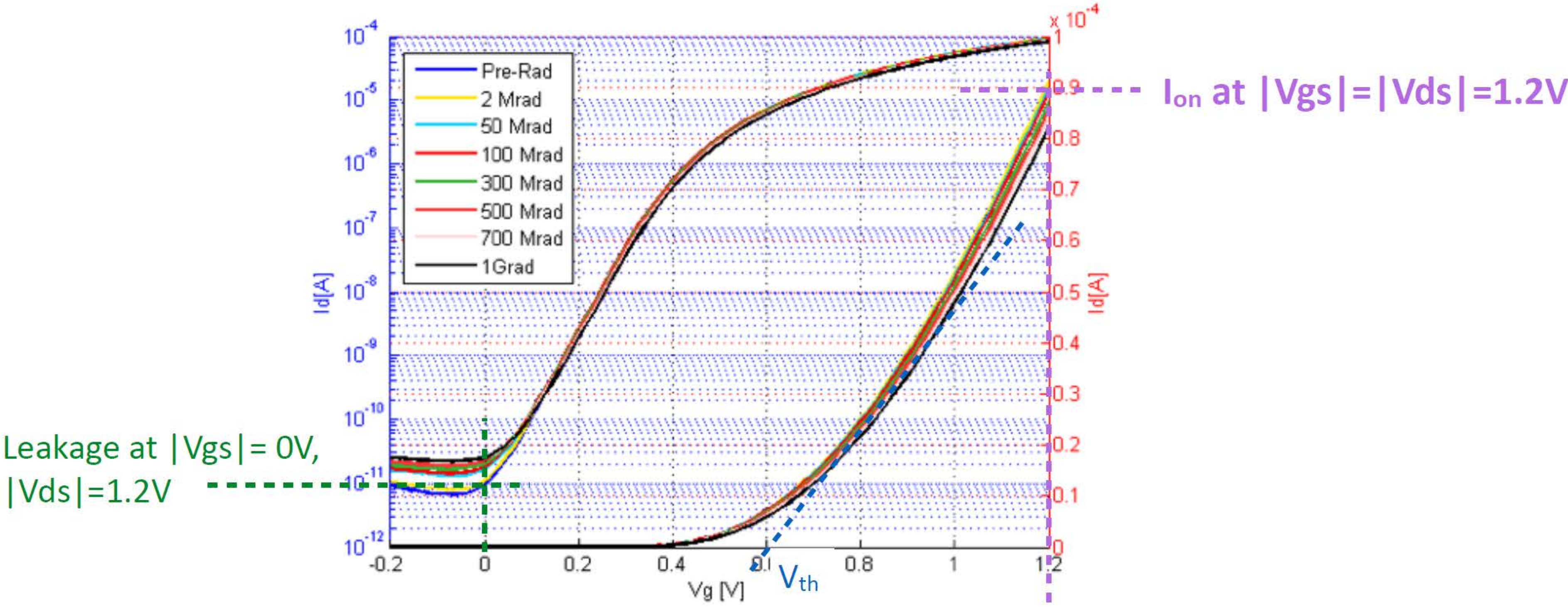
Radiation tolerance varies in different Fabs, and can change over time. We have to:

- **only qualify and use one Fab**
- **monitor regularly the natural radiation tolerance**
- **carefully qualify each ASIC during the prototyping and production phases**

In some of the results above we can see analogies with the phenomenology observed in bipolar technologies subject to ELDRS (Enhanced Low Dose Rate Sensitivity)

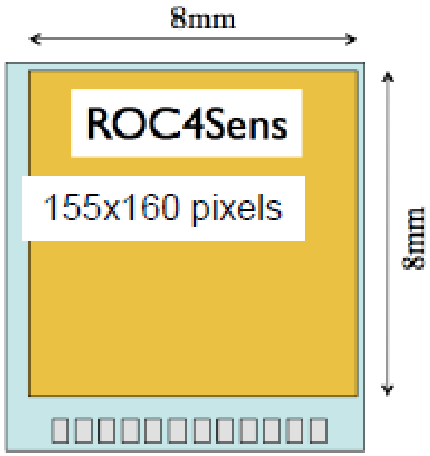
The main parameters extracted from the measurements are:

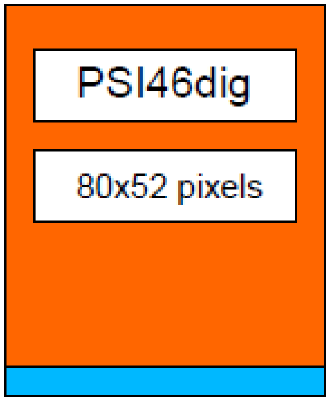
- **Drive current (I_{on})**
- **Threshold voltage (V_{th})**
- **Transconductance (G_m)**
- **Leakage current**



Test ROCs for R&D

Name	Pixel Size (μm^2)	Tech nology	Rad hard	Available ?
ROC4Sens	50x50	250 nm (IBM)	5 MGy	end-2016
FCP130	30x100	130 nm (GF)	5 MGy	end-2016
RD53A	50x50	65 nm	Up to 10 MGy	mid-2017?





"Fallback":

Name	Pixel Size (μm^2)	Tech nology	Rad hard	Available?
PSI46dig	100x150	250 nm (IBM)	1.1 MGy	In hand

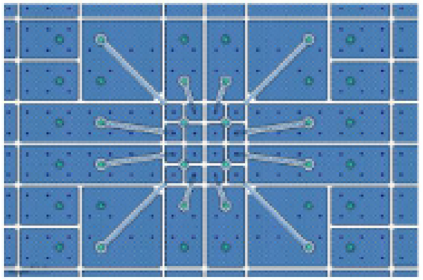
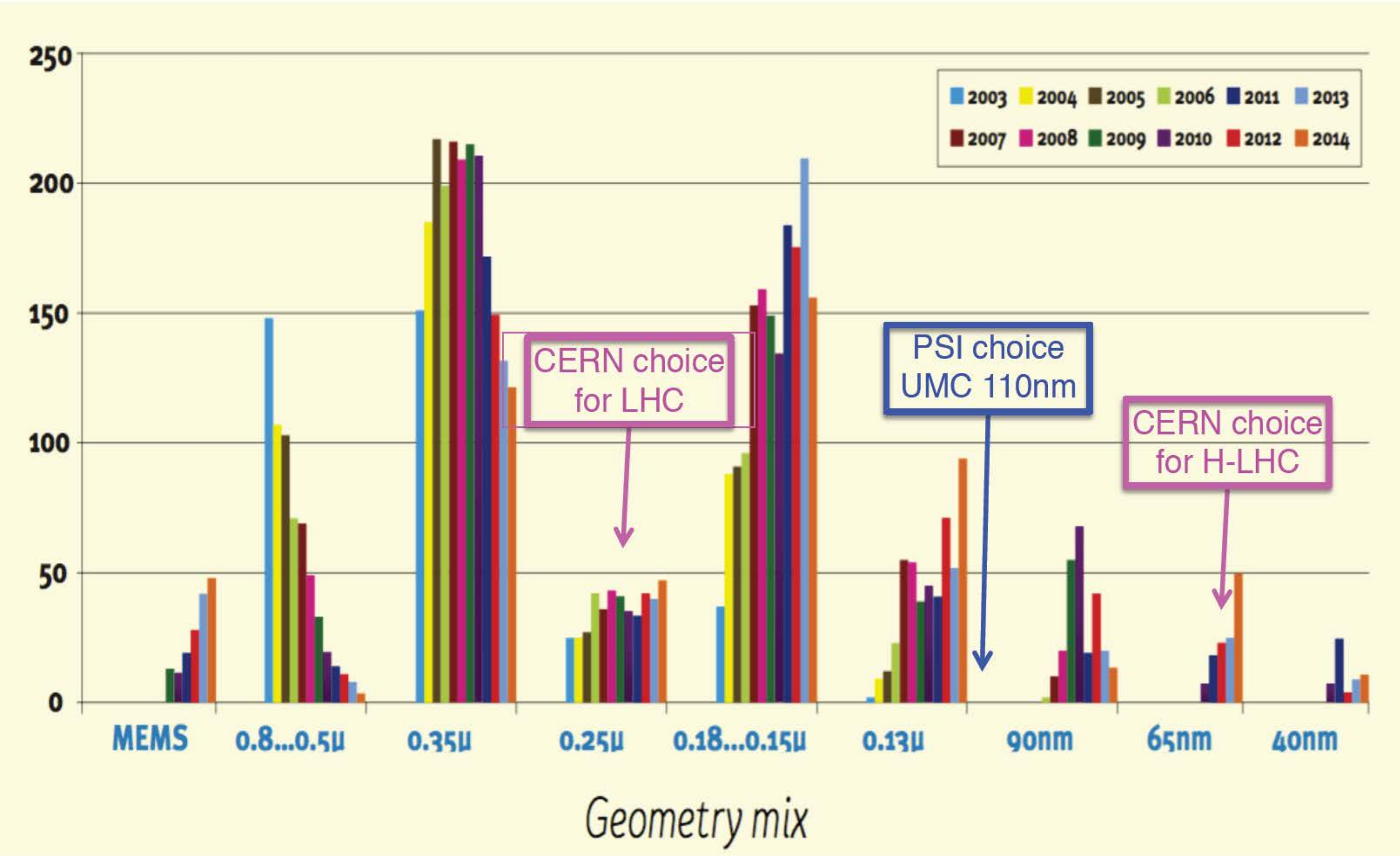


Fig. 8. Layout of 50 µm × 50 µm pixel cells surrounded by larger cells to be compatible with the PSI46dig readout chip.

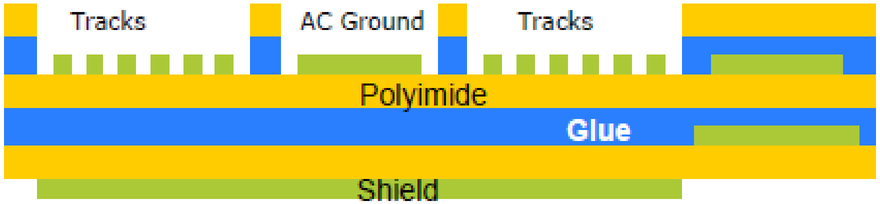
Yearly Report 2014 by Europractice

Statistics in CMOS technology use in Europe over the years.   Where is the market going?

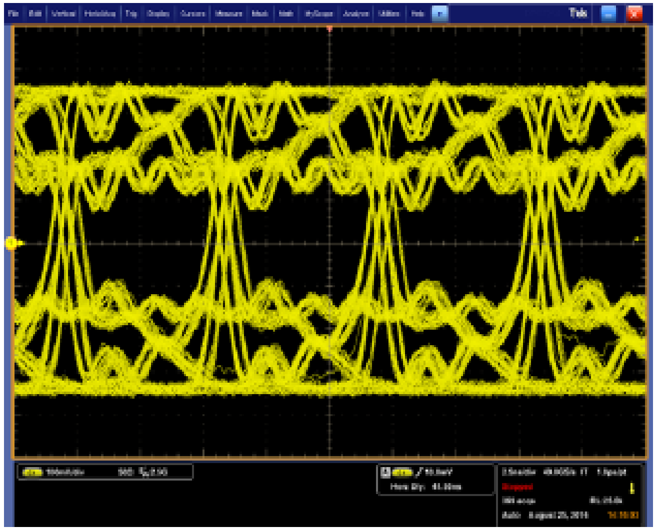


Data Transmission on Bus Tape

- Bus tapes (up to 140 cm) provide:
  - all the low and high voltage from the end of structure to the module
  - all the high speed data links



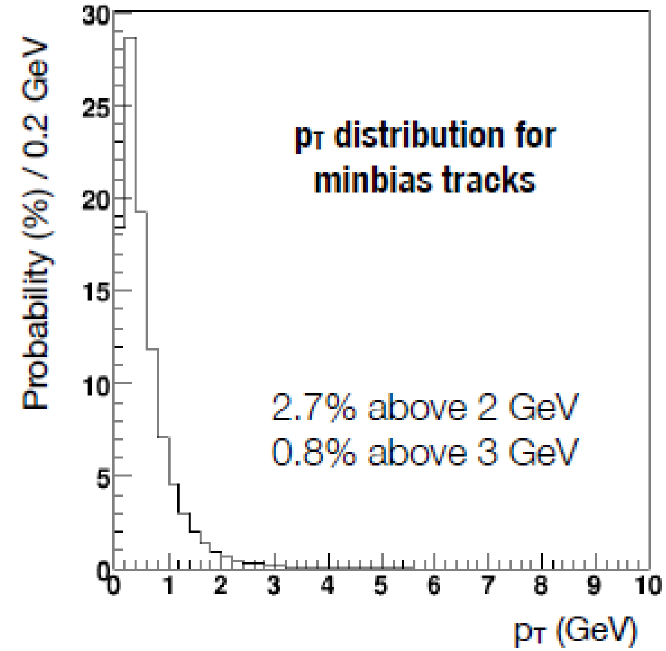
- Designed to have very high reliability and minimum material.
  - Bottom shield is necessary to avoid influence of carbon fiber facing
- 1MHz readout specification requires
  - 640 Mbps for data transmission point to point
  - 160 Mbps transmission of TTC data on multi-drop lines
- Point to point data transmission:
  - Tape bandwidth in excess of the required 640 Mbps. The transmission robustness can be further enhanced by using 8/10b encoding.
- TTC multidrop:
  - Even with reflections from 10 hybrid loads the transmission works well at 160 Mbps
  - No errors in all tests with x2 load values, or x2 speed, or both.



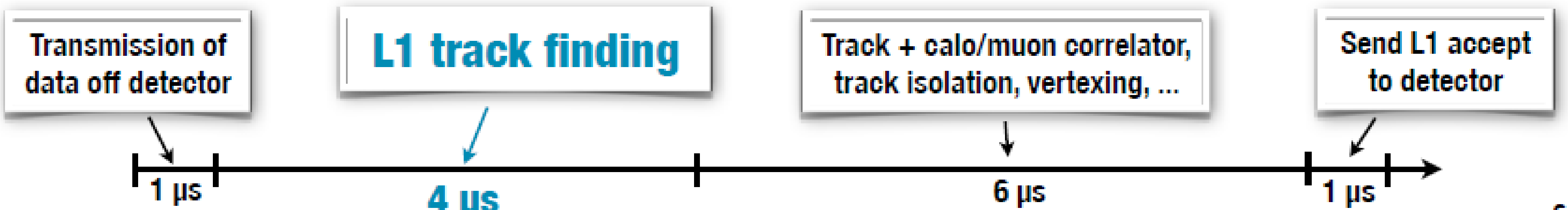
Eye diagram for PRBS-31 (equivalent to no data encoding) for 160 Mbps and double the capacitive loads

Challenges with tracking @ L1

- Expected HL-LHC conditions
  - 40 MHz BX frequency, <PU> = 200
  - ~33 charged particles from minbias @ 14 TeV
    ⇒ 6600 charged particles / BX
  - ~200 tracks with p_T > 2 GeV per event

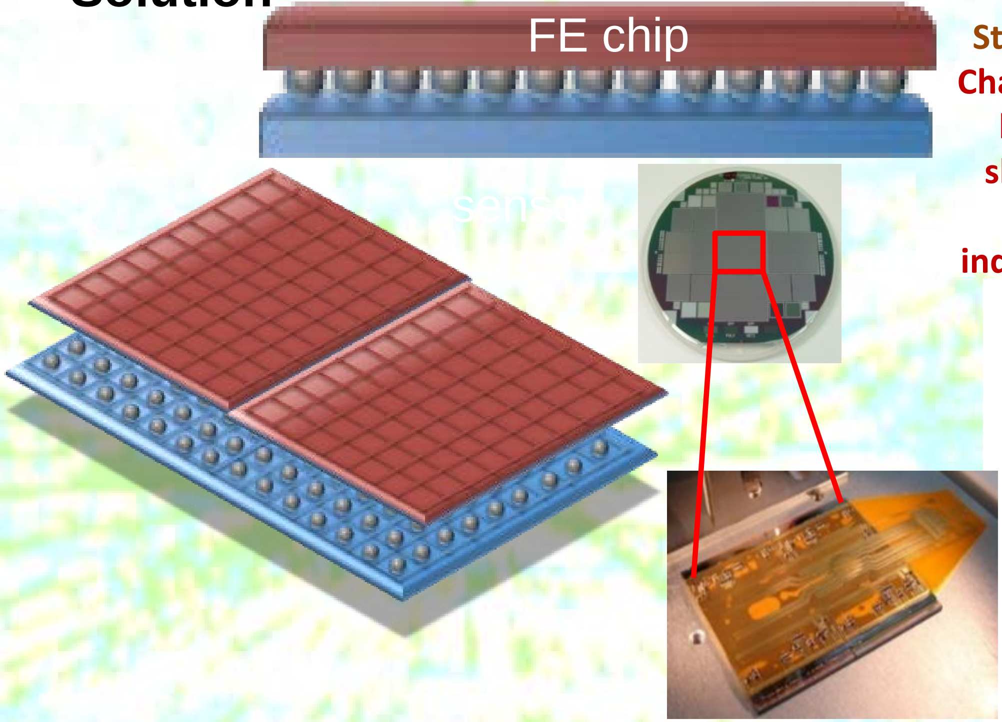


- **Combinatorics** ⇒ 15-20K input stubs / BX
- **Data volumes** ⇒ up to ~50 Tbits/s
- L1 trigger decision within 12.5 μs ⇒ **time available for track finding ~4 μs**

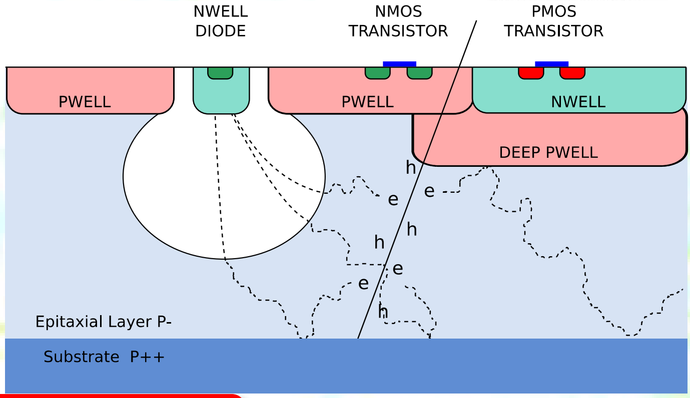


Possible CMOS Tracking for the ITk

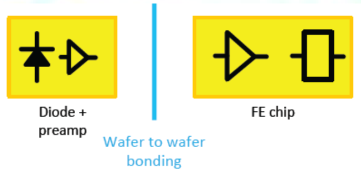
- **ATLAS Pixels: Planar Sensor Solution**



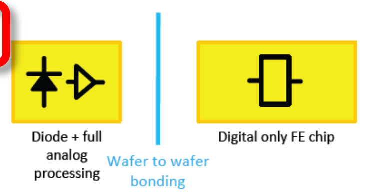
Standard MAPS: Charge collection by diffusion → slow and prone to radiation induced trapping



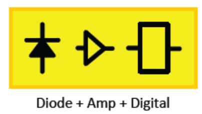
- Hybrid Pixels with "smart" diodes
  - HR- or HV-CMOS as a sensor (8")
  - Standard FE chip
  - Ex: CCPD on FE-I4



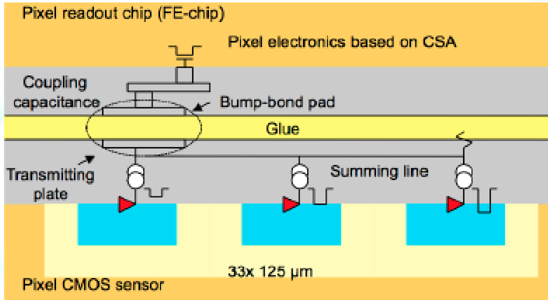
- CMOS Active Sensor + Digital R/O chip
  - HR- or HV-CMOS sensor + CSA (+Discriminator)
  - Dedicated "digital only" FE chip



- Monolithic Active Pixel Sensor on a fully depleted substrate (DMAPS)
  - HR-CMOS process

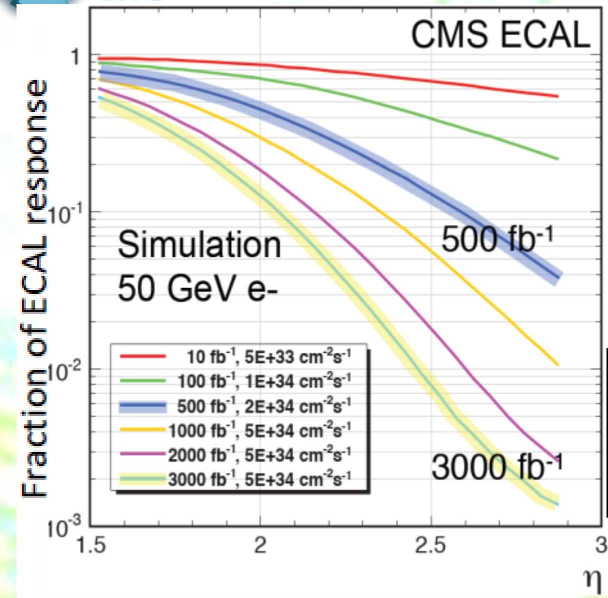


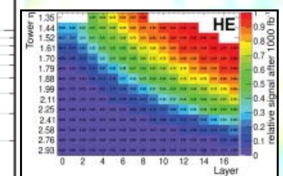
Smart pixel approach: reuses circuitry developed for passive pixel sensor read-out but still needs new chip submissions and hybridisation step



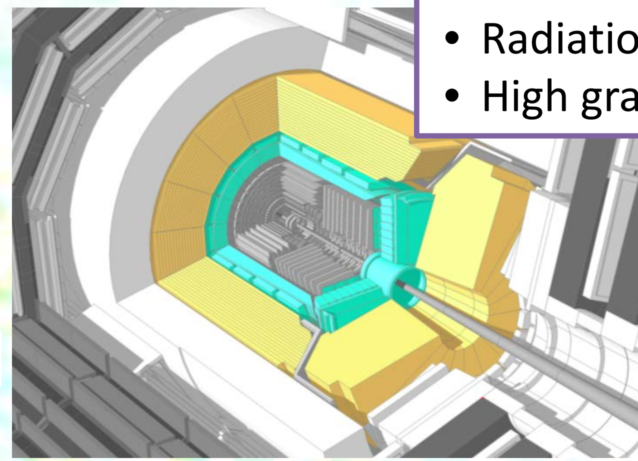
- ATLAS is studying all variants of HV/HR-CMOS for possible replacement of its tracking layers, particularly at intermediate radii where there is more area to cover, but radiation is less of an issue. **Largest current pixel cost component is the bump-bonding**.
- For strips, the planar sensor with 4 rows of 2.45cm strips at 80μm pitch could be replaced by a CMOS sensor which encodes the z position but then is still connected to a modified version of the current development strip ASIC

CMS Phase-II Calorimeter



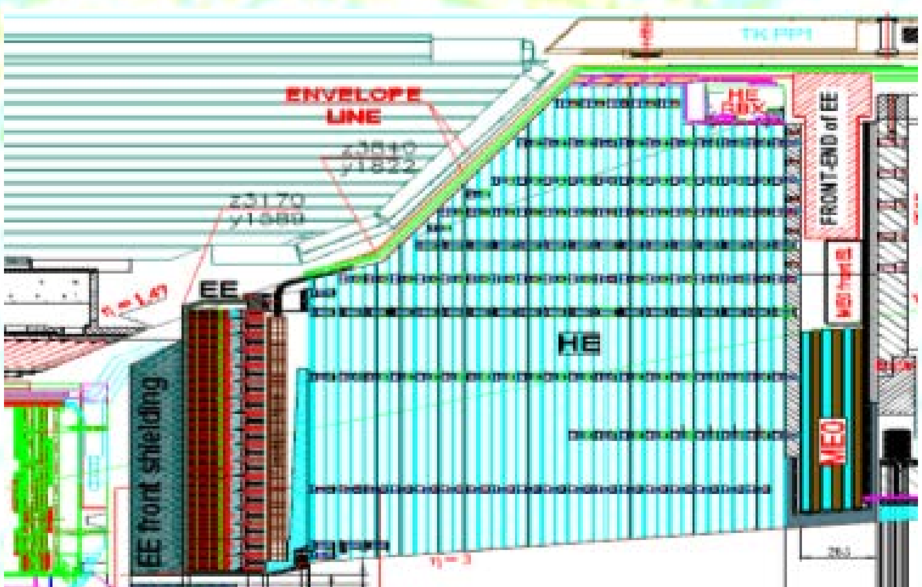


Predicted HCAL Endcap signal response after 1000fb-1 versus active layer and η

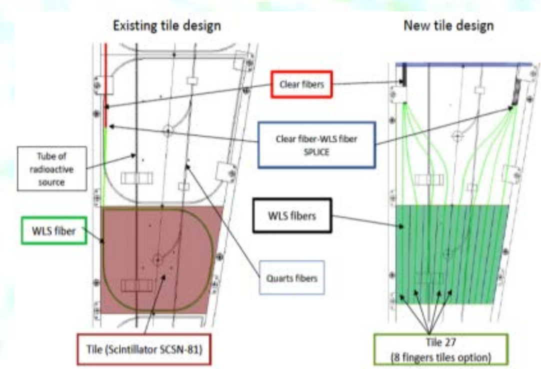


New Endcap Calorimeters
- Radiation tolerant
- High granularity

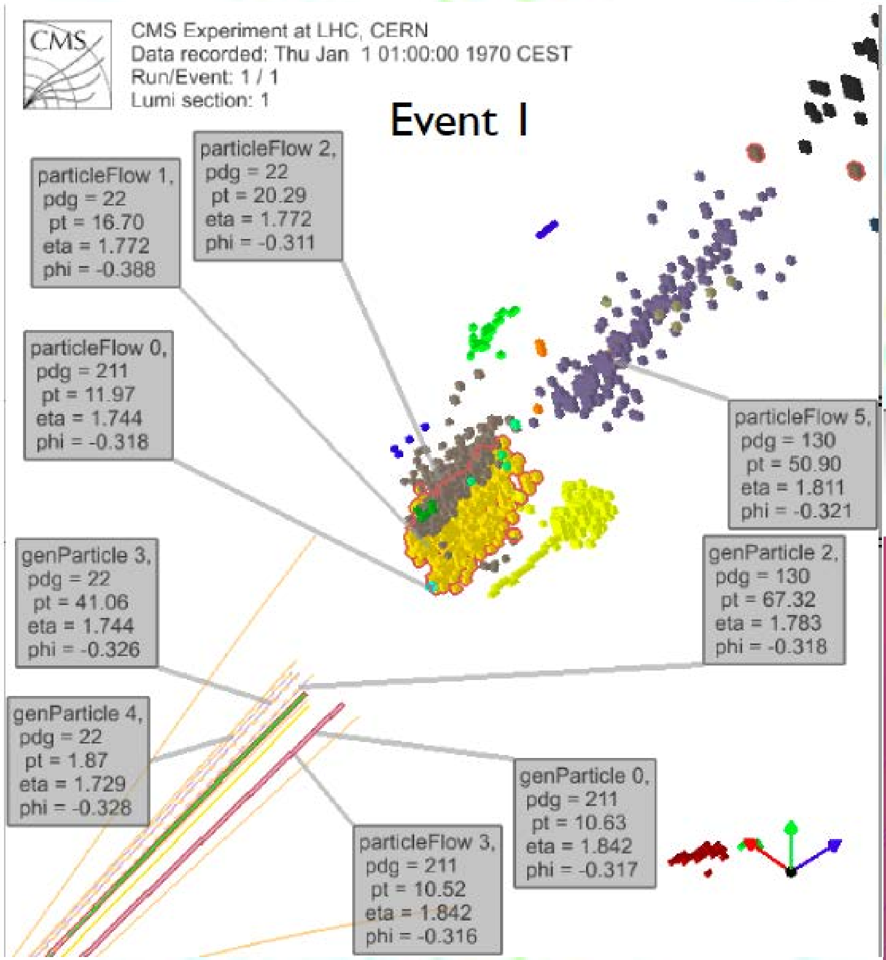
CMS need to replace ECAL and HCAL end-cap calorimeters due to radiation damage



CMS scintillator-based HCAL with 30% of volume replaced by finger tiles to reduce optical path and attenuation



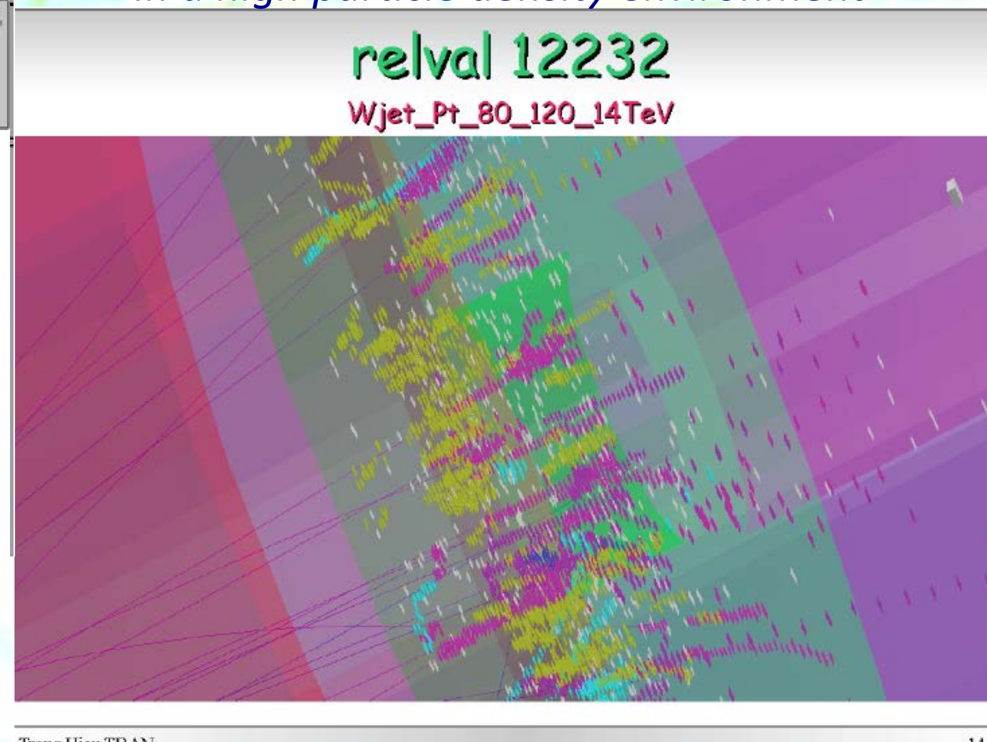
Si-HGC Event Displays



Si-HGC extends Tracking into Calorimeter

Provides good cluster energy resolution, very detailed topological information and excellent two-particle cluster res0lving power

Ideally suited for Particle Flow reconstruction in a high particle density environment

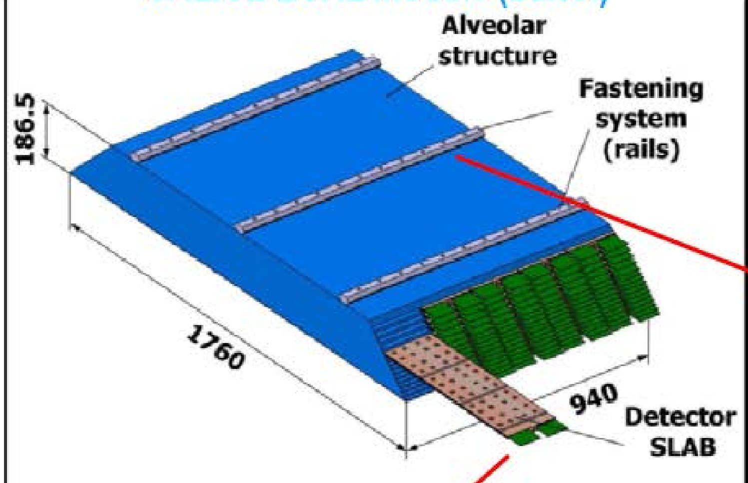


marcello.mannelli@cern.ch

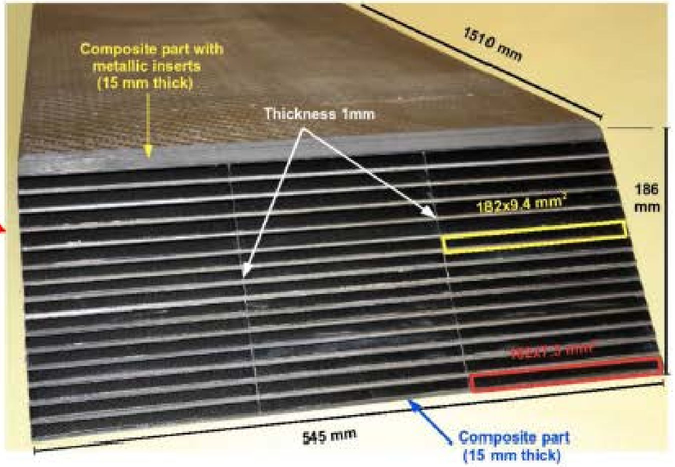
ILC /CLIC-like HGCAL

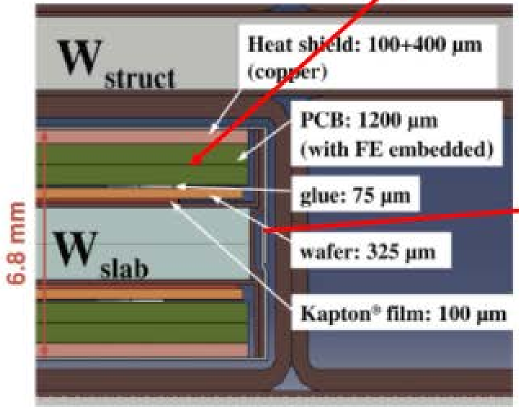
Reminder of the CALICE ECAL concept

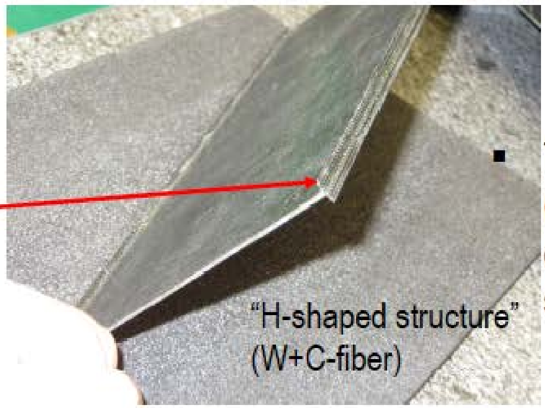
CALICE ECAL module (barrel)



- Half of the tungsten plates is incorporated into a self-supporting **alveolar composite structure** (carbon)





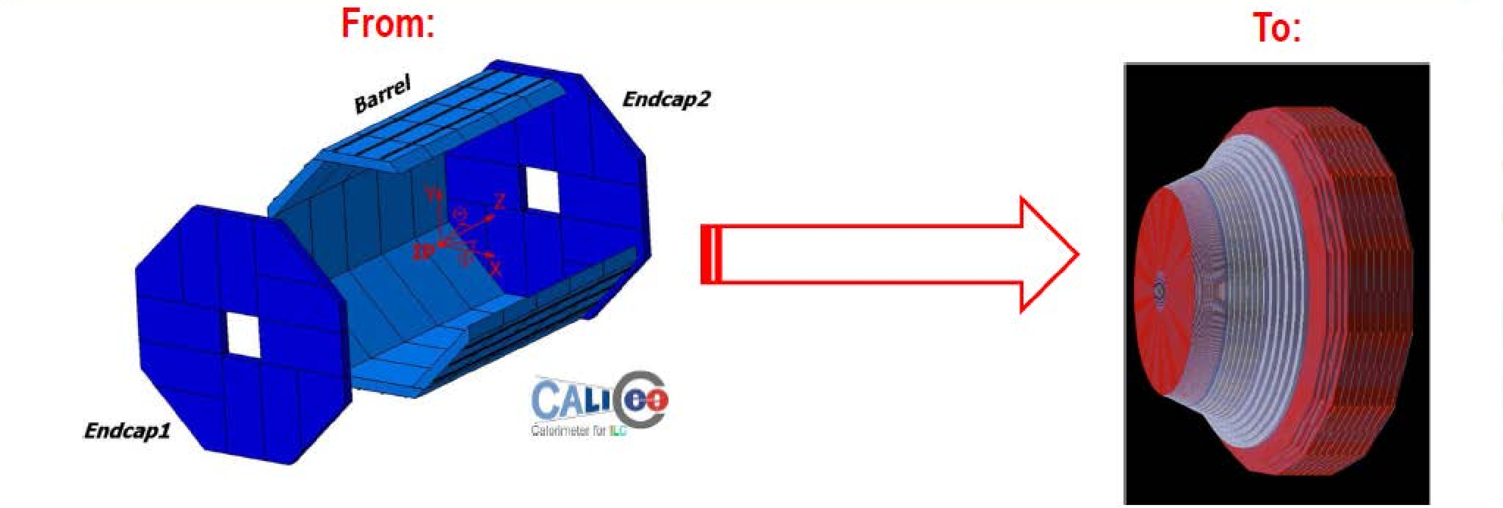


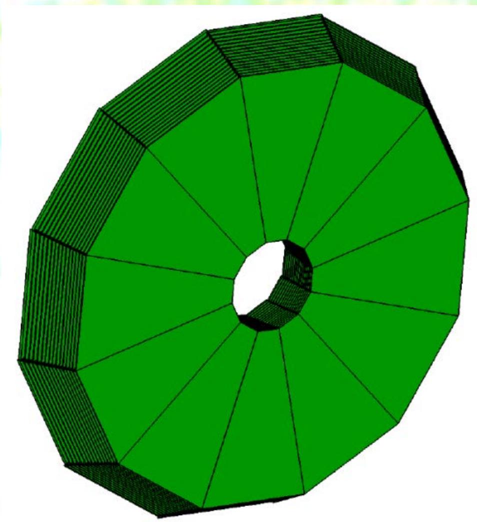
- The other half of the W plates in supports (H-shaped structure) called **detector SLAB (or "drawer")**, slide inside each cell.

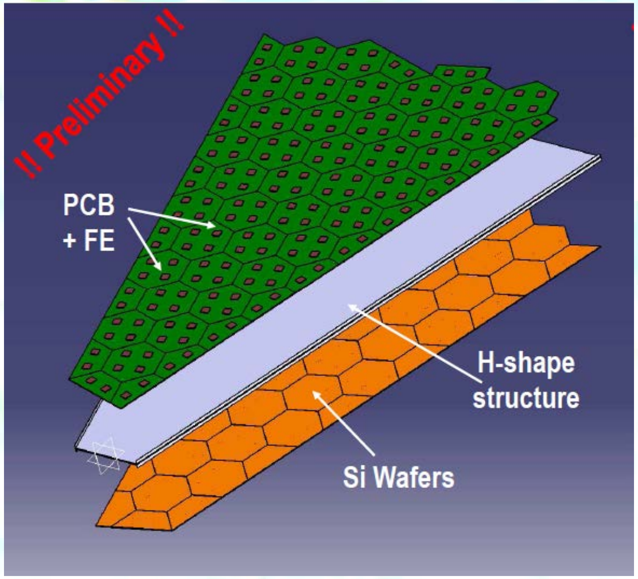
3

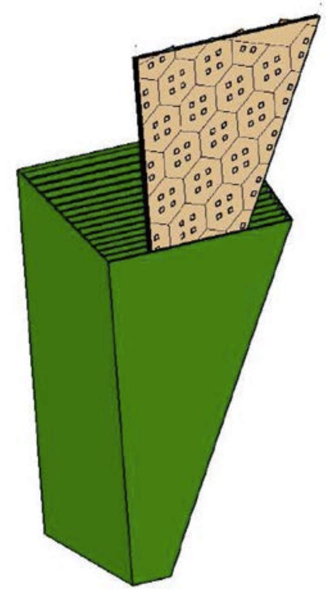
ILC /CLIC-like HGCAL

Adaptation to CMS Endcaps

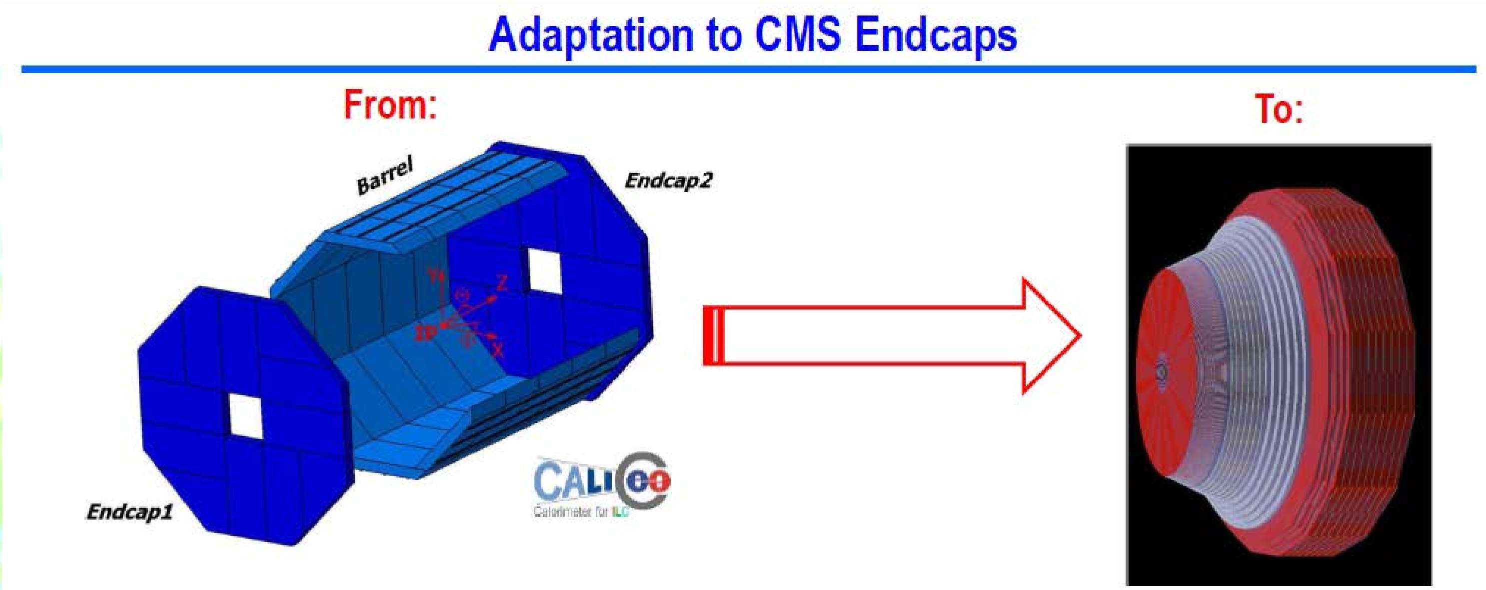








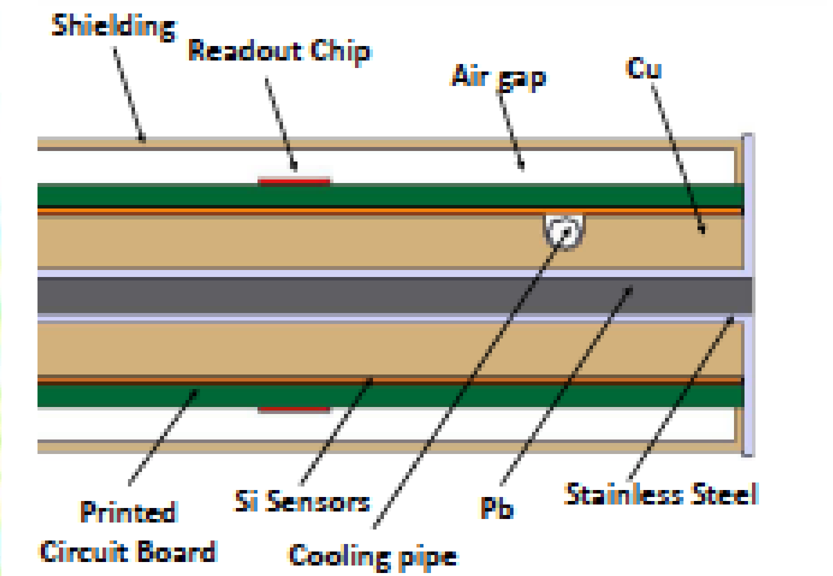
ILC-like structure for FCC-HGC



Big Differences include

- **Power consumption, cooling, & Data rates**
- **Radiation and -30^{0}C operating temperature**
  - **Thermal enclosure & services feed-troughs**
- **Profit from synergy with Tracker R&D**
  - **Sensors, cold operation & CO_2 cooling, Power & Read-Out**

Power consumption, cooling & data rates - CMS study



Power ranges from ~ 100W/m^2 in Barrel (300um thick sensors and 1cm^2 cell size)

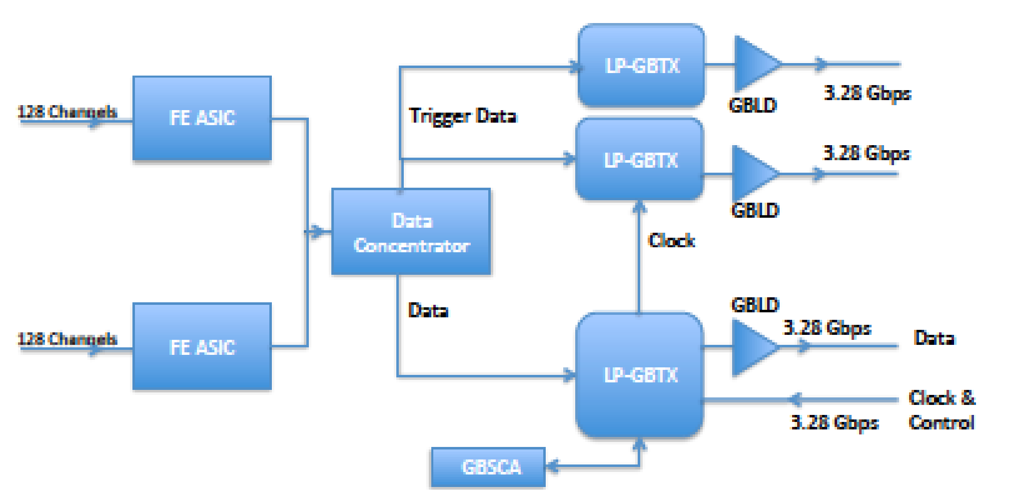
Up to ~ 250W/m^2 in End-Cap (100um thick sensors and 0.5cm^2 cell size)

Operate Silicon at -30C^0 (-35C^0 if possible)

Exploit low cell occupancy and steeply falling energy spectrum, with simple data compression algorithm

CMS: from 1~2Gbps/Module up to ~8Gbps/Module in End-Cap; Dominated by L1 Trigger data

Expect ~ *2 at FCC



Input parameters, assumptions, disclaimers

Simple model based on today's computing models, but with expected HL-LHC operating parameters

ATLAS Input Parameters at HL-LHC (LOI = the ATLAS Letter of Intent for Upgrade Phase-2)

Output HLT rate: 10kHz (5 to 10 kHZ in LOI)
Reco and Simul Time/Evt: from LOI
Nr Events MC / Nr Events Data = 2
Fast Simulation: 50% of MC events
LHC live seconds /year: 5.5M

CMS Input Parameters at HL-LHC

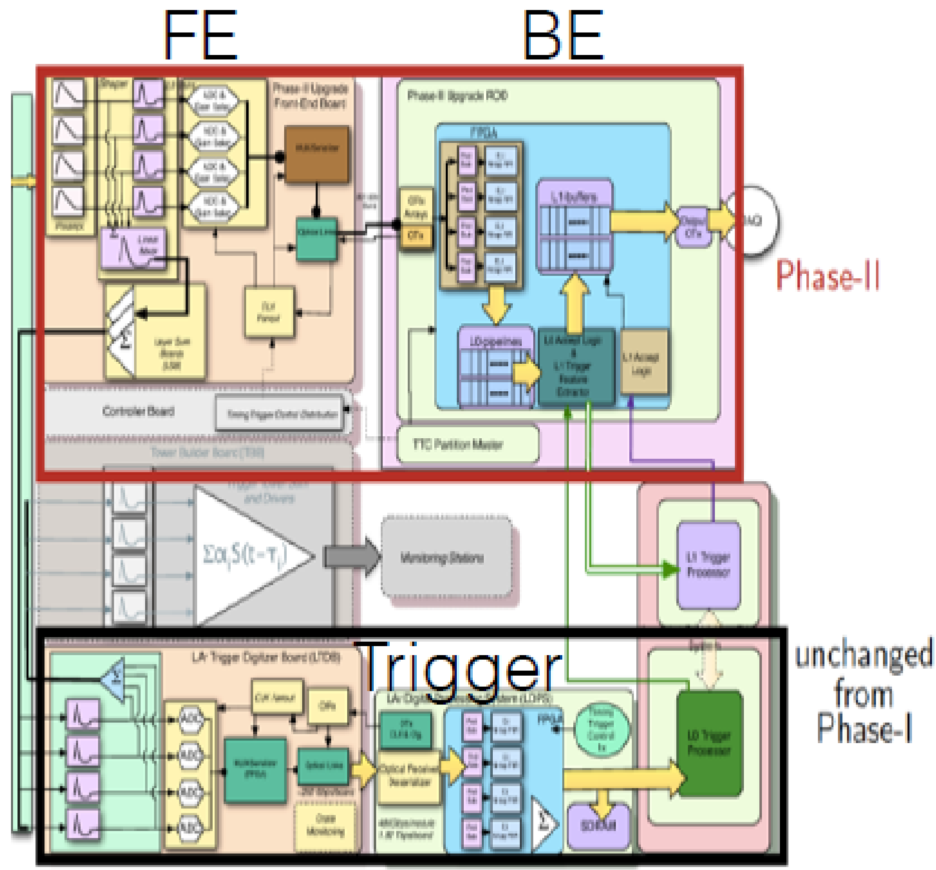
Output HLT rate 7.5 kHz
LHC live seconds /year: 6.0M
Dataset overlap factor: 1.2
Reco and Simul Time at mu=200
Nr Events MC / Nr Events Data = 1.3
Analysis estimated as +60% of all other CPU usage

Simplified Computing Model with respect to 2016/2017 resource requests:

Legacy from previous years not taken into account
=> Little difference at the beginning of the Run-4 but huge difference for Run-2 and Run-3

overview

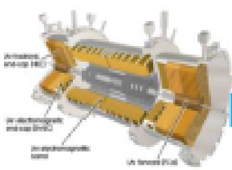
- Motivation:
  - Phase II trigger latency will be longer (>x4), current system cannot buffer enough data.
  - “Free-running” mode : data will be shipped to BE at 40 MHz
  - Current readout system limited to 100kHz, but 1-4MHz needed by L1/L0.
  - Radiation tolerance need factor of ~3 improvement
- Phase I (2019/20): x10 finer granularity super-cells, 40MHz to L0 trigger.
  - will remain unchanged.

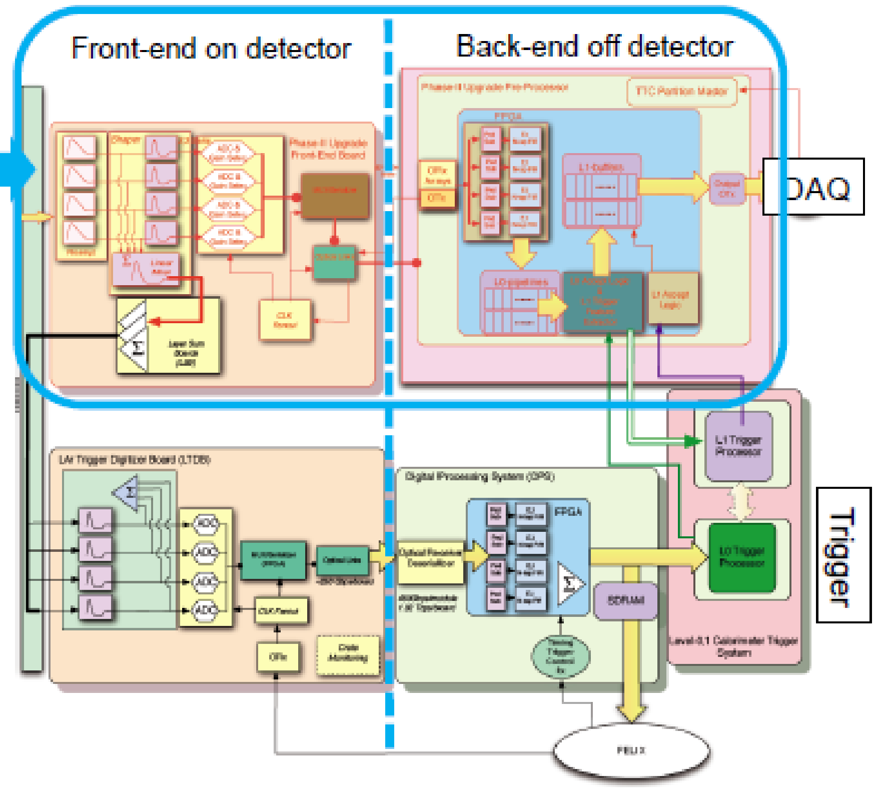


Upgrade of LAr Calorimeter Electronics

- LAr readout system requires upgrade for HL-LHC because:
  - current analog pipeline on front-end is not compatible with x4 longer L0 trigger latency of 10 μs
  - front-end and back-end systems are limited to 100 kHz readout - much less than foreseen L0 accept rate of 1-4 MHz
  - radiation tolerance requirements increase by factor 3

- Phase-II upgrade (LS3, 2024-26):
  - free-running 40 MHz readout of all LAr calorimeter cells
  - input to higher trigger levels/DAQ
  - off-detector long-latency data buffering





- Phase-I upgrade (LS2, 2019/20):
  - super-cell readout readout
  - x10 better granularity to first hardware trigger level than today
  - 40 MHz input to future L0 trigger

HL-LHC ATLAS Target Menu: Lepton triggers

Assumes Instantaneous Luminosities up to 7.5 10^{34}

Analysis Thresholds in **GeV**, Rates in **kHz**

Description	Run 1 Threshold	HL-LHC Threshold	L0 Rate	EF Rate
isolated e	20-25	22	200	2.20
di-electron	17, 17	15, 15	90	0.08
forward e	–	35	40	0.23
single γ	40−60	120	66	0.27
di-photon	25, 25	25, 25	8	0.18
single μ	25	20	40	2.20
di-muon	12, 12	11, 11	20	0.25
e-μ	17, 6	15, 15	65	0.08
τ	100	150	20	0.13
di-tau	40,30	40, 30	200	0.08

Total non-hadronic L0 rate: ~750 kHz, EF rate: 5.7 kHz

HL-LHC ATLAS Target Menu: Hadronic triggers

Assumes Instantaneous Luminosities up to 7.5 10^{34}
Analysis Thresholds in **GeV**, Rates in **kHz**

Description	Run 1 Threshold	HL-LHC Threshold	L0 Rate	EF Rate*
single jet	200	180	60	0.6
large-R jet	–	375	35	0.35
four jet	55	4 x 75	50	0.50
forward jets	–	180	30	0.30
HT	–	500	60	0.60
MET	120	200	50	0.50
JET + MET	150, 120	140, 125	60	0.30

assumes b-tagging

includes mult-jet + inv mass triggers

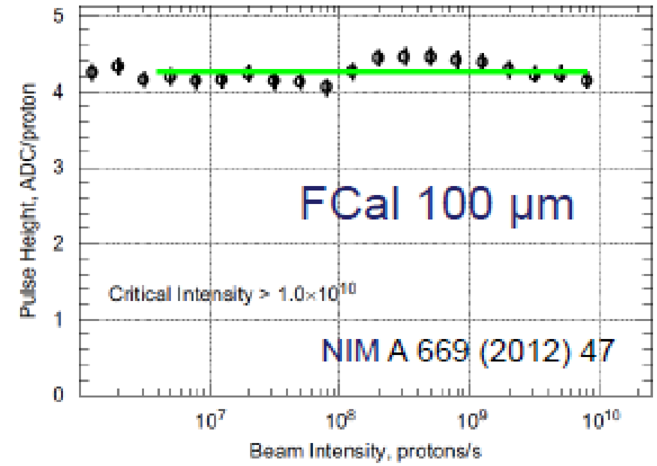
Total hadronic L0 Rate: ~**250 kHz**, EF Rate: **3.15 kHz**

750 kHz (leptonic) + **250 kHz** (hadronic) = **1000 kHz**

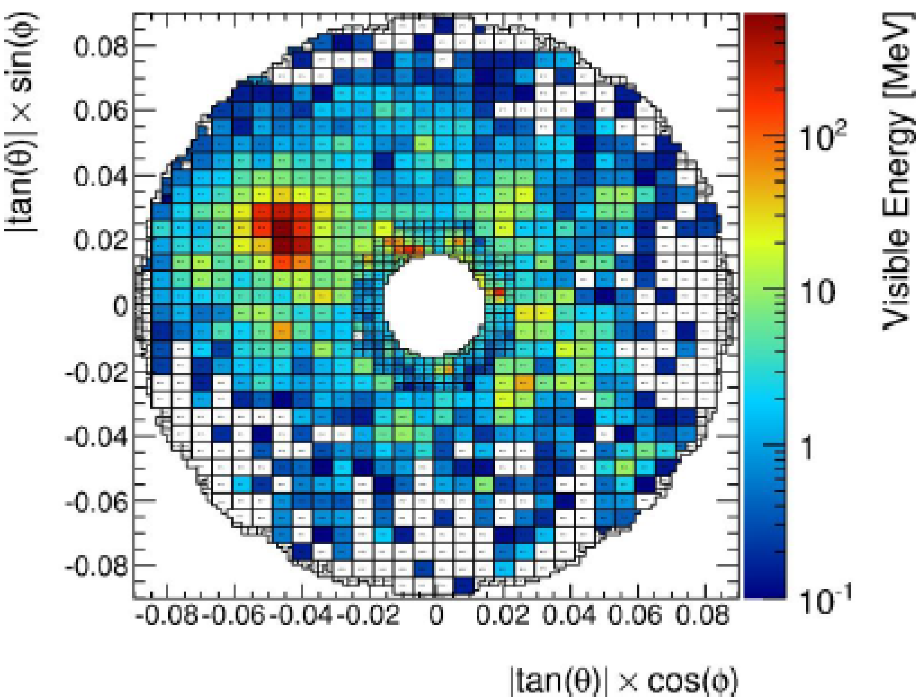
A High-Granularity sFCal

- High-granularity sFCal:
    - smaller LAr gaps: approx 100 μm for FCal1
    → proven to work in HiLum testbeam
    - no summing of channel groups in FCal1
    → x4 higher granularity in FCal1 at $3.2 < |\eta| < 4.3$

→ improved pile-up suppression in particular in combination with ITk tracker extension to high $|\eta|$



simulated single jet in FCal1



simulated single jet in sFCal1