PCIExpress Communications Subsystem Progress Report

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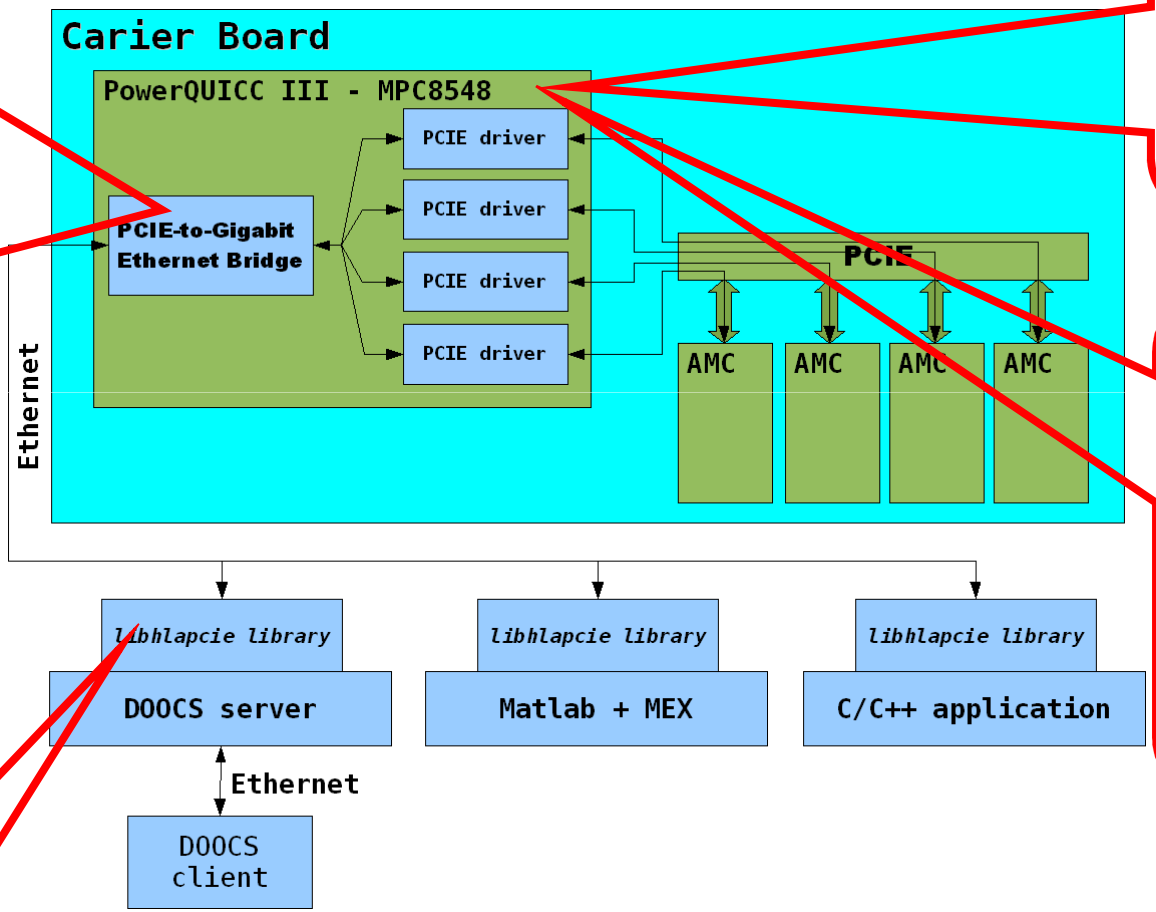
WP Status

WP	STATUS
Development of operating system and low level drivers for Power Quick III processor	80%
End user application for PCIe transmission	95%
Design and implementation of PCI express communication in DOOCS environment (drivers, client-server applications)	90%
Design and implementation of PCI express Root Complex (software)	100%

System Overview
PCIExpress Software Layer

WP 3.4.7
Design and implementation of PCI express communication in DOOCS environment (drivers, client-server applications)

WP 2.3.12
Development of operating system and low level drivers for Power QUICC III processor



WP 3.4.2
Design and implementation of PCI express Root Complex (software, MPC8568)

WP 3.4.4
End user application for PCIe transmission

WP 3.4.2
Design and implementation of PCI express Root Complex (software)

A. Piotrowski, G. Jabłoński

- Deliverables: Set of patches for Freescale MPC8568 Board Support Package enabling the MSI interrupts and root-complex functionality. The drivers to direct communication with the register sets implemented on the peripheral boards (MPC8568 microprocessor).

Current status

- Linux OS with kernel 2.6.25.4 was installed
- Pathes to enable MSI support in OS kernel were designed and implemented
- Low level drivers for communication with PCIExpress device was designed and implemented
- Manuals for software, example applications
- Report and acceptance test procedure

- **Task status – 100%**

WP 2.3.12
Development of operating system and low level drivers for Power Quick III processor

A. Piotrowski, D. Makowski, G. Jabłoński

- Deliverables: Source code for low level drivers for diagnosis of PCI Express subsystem, several patches for Linux operating systems to enable the MSI interrupt support, port of Freescale Board Support Package to RadiSys board (Freescale MPC8548 microprocessor).

Current status

- Linux OS with kernel 2.6.25.4 was installed
- Low level drivers for communication with PCIExpress device
- Pathes to enable MSI support – in progress
- No progress
  - serious problems with RadiSys Carrier Board

- Task status – 80%

WP 3.4.4
End user application for PCIe transmission

A. Piotrowski, D. Makowski

- Deliverables: Source code for library performing communication between end-user applications and PCI Express to Ethernet bridge.

Current status

- Communication library for end user application was designed and implemented
- Example test DOOCS server, to check behaviour of library was implemented
- Matlab MEX extension was implemented to make communication between Matlab and PCIExpress device possible
- Tests of the behaviour of the library under Linux and SunOS operating systems – in progress
- Preparation of documentation for library – in progress

- Task status – 95%

WP 3.4.7
Design and implementation of PCI express communication in DOOCS environment

A. Piotrowski, D. Makowski

- Deliverables: Source code for client-server application responsible for reliable communication between PCI Express driver and external TCP/IP servers. Source code for Linux driver responsible for reading and writing data directly from PCI Express devices.

Current status

- Modular client-server application was designed and implemented
- Linux driver to perform communication with PCIExpress device was designed and implemented. Separate versions for MPC8568 and MPC8548 were created
- Test of the behaviour of the client-server application
- Preparation of documentation and report – in progress
- Implementation of additional functionality – in progress
  - problem with deliverables
  - problem with tests
- Task status – 90%

Tests in extension hall

- Test of ADC Readout System located in Extension Hall
- Hardware
  - AdLink Carrier Board
  - TEWS 900 AMC board
- Software
  - Linux Debian on AdLink Carrier Board
  - DOOCS Example Server
  - PCIE device driver
  - PCIE-to-Ethernet bridge server
  - libhlapcie library

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Acceptance test procedure

- Proposed acceptance procedure was designed to test correctness of entire PCIExpress-based software communication layer. For that reason, one procedure is proposed for tasks enumerated below:
  - LLRF WP 2.3.12 - Development of operating system and low level drivers for Power Quick III processor,
  - LLRF WP 3.4.7 - Design and implementation of PCI express communication in DOOCS environment (drivers, client-server applications),
  - LLRF WP 3.4.4 - End user application for PCIe transmission,
  - LLRF WP 3.4.6 - Integral Interface for PCIe,
  - LLRF WP 3.4.3 - Low level drivers for PCI express communication (FPGA)
  - LLRF WP 3.4.2 – Design and implementation of PCI express Root Complex (software)

Thank You