Agenda

- **Deliverables – current state**
- **Development of software for AMC_B module**
- **Development of diagnostic application for ATCA carrier board**

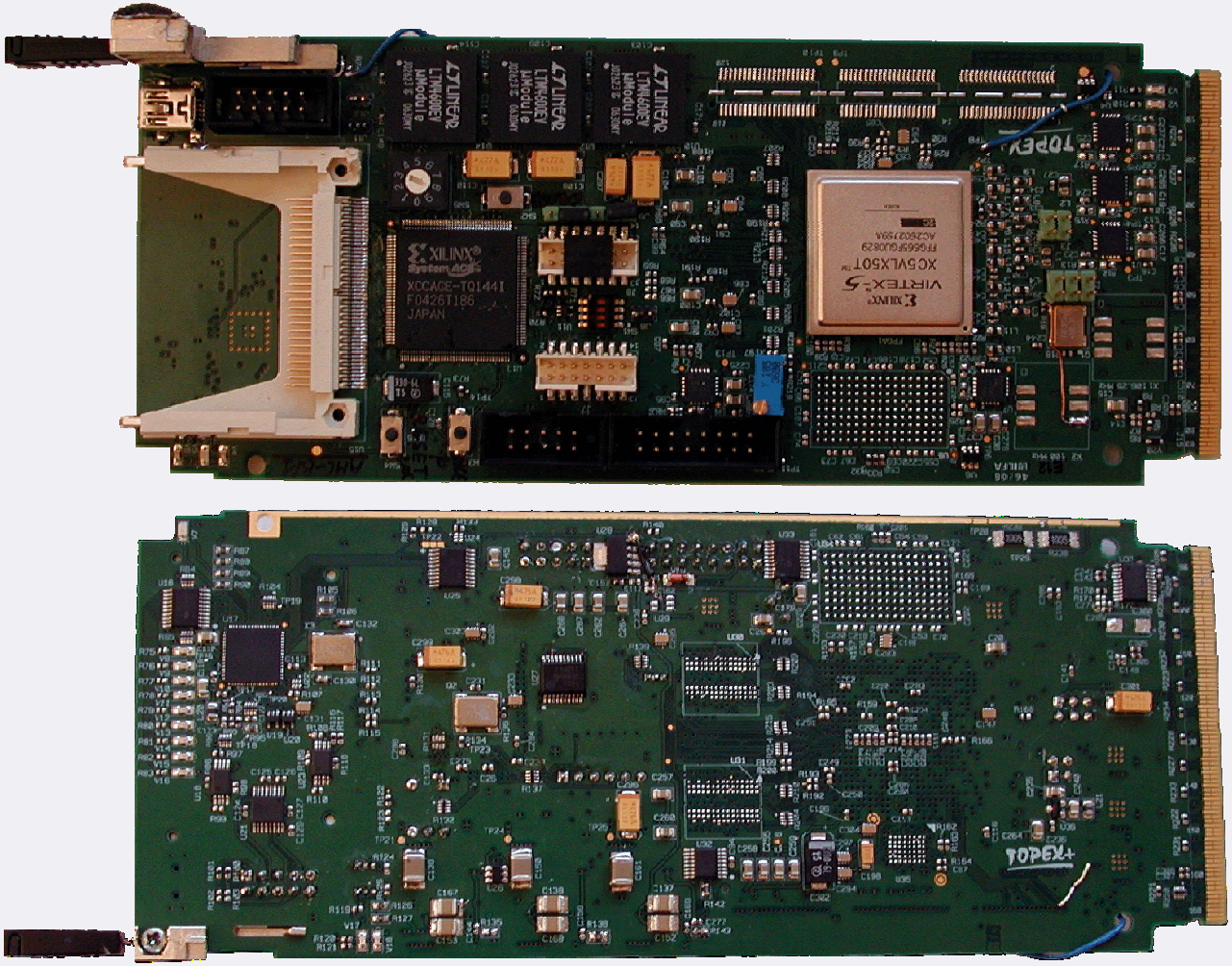
Deliverables – current state

Subtask / Item	Progress	Deliverable	Res. person	Problems
Preparation of requirement for Digital Feedback in Enterprise Architect	25%	The requirements for ATCA carrier boards and AMC modules will be delivered in Enterprise Architect. Requirements and documentation for submodules of the ATCA-based feedback system.	Dariusz Makowski	No final architecture defined (distributed-centralized)
Development of diagnostic application for ATCA carrier board	100%	Application for PC computer and procedures written in C/C++ for the IPMC microcontroller will be delivered. ATCA carried with IPMC controller will be used as a demonstrator.	Dariusz Makowski	The person responsible for this task chaged
Design of PCIe Root Complex mezzanine board with Power Quick III processor (hardware)	20%	Mezzanine module with PowerQuick III processor with high-speed connectors.	Dariusz Makowski	Depends on the architecture of carrier-board. First prepare requirements for carrier then for PQ III module
Development of IPMI ATCA board with Renesas microcontroller	50%	ATCA carrier board with Renesas Microcontroler.	Dariusz Makowski	-
Development of IPMI software for Atmega microcontroller	75%	Software and low level drivers for ATMEGA 1281 microcontroller for ATCA-IPMI carrier board.	Dariusz Makowski	No AMC_B module - now we can continue
Application for configuration data storage in configuration data base (software)	5%	The set of procedures for storing and reading firmware from database will be delivered.	Bartosz Sakowicz	Partly defined how to program FPGAs and microcontrollers, probably carrier V2 is required
Development of second version of ATCA carrier board	50%	Schematic diagrams will be created and the ATCA carrier board will be delivered.	Dariusz Makowski	First version, requirements then second carrier
Development of operating system and low level drivers for Power Quick III processor	80%	Source code for low level drivers for diagnosis of PCI Express subsystem, several patches for Linux operating systems to enable the MSI interrupt support, port for Freescale Board Support Package to RadiSys board.	Adam Piotrowski	Serious problems with RadiSys - linux with PCIe support for ADLINK
ATCA and AMC PCB templates for Mentor Graphics	100%	A library with ATCA and AMC template for Mentor Graphics will delivered	Dariusz Makowski	-
Preparation of requirements for Communication Interfaces in Enterprise Architect	5%	Requirements for Communication Interfaces based on PCIe bus architecture in the form of Enterprise Architect project file.	Adam Piotrowski	
Low level drivers for PCI express communication (FPGA)	100%	Source code for the Packet Interface – Address/data bus bridge, tested on the Freescale MPC8568 Evaluation Board and ML-506 Virtex 5 Evaluation Board.	Grzegorz Jabłoński	
End user application for PCIe transmission	95%	Source code for library performing communication between end-user applications and PCI Express to Ethernet bridge.	Adam Piotrowski	Not well defined specification - new requirements

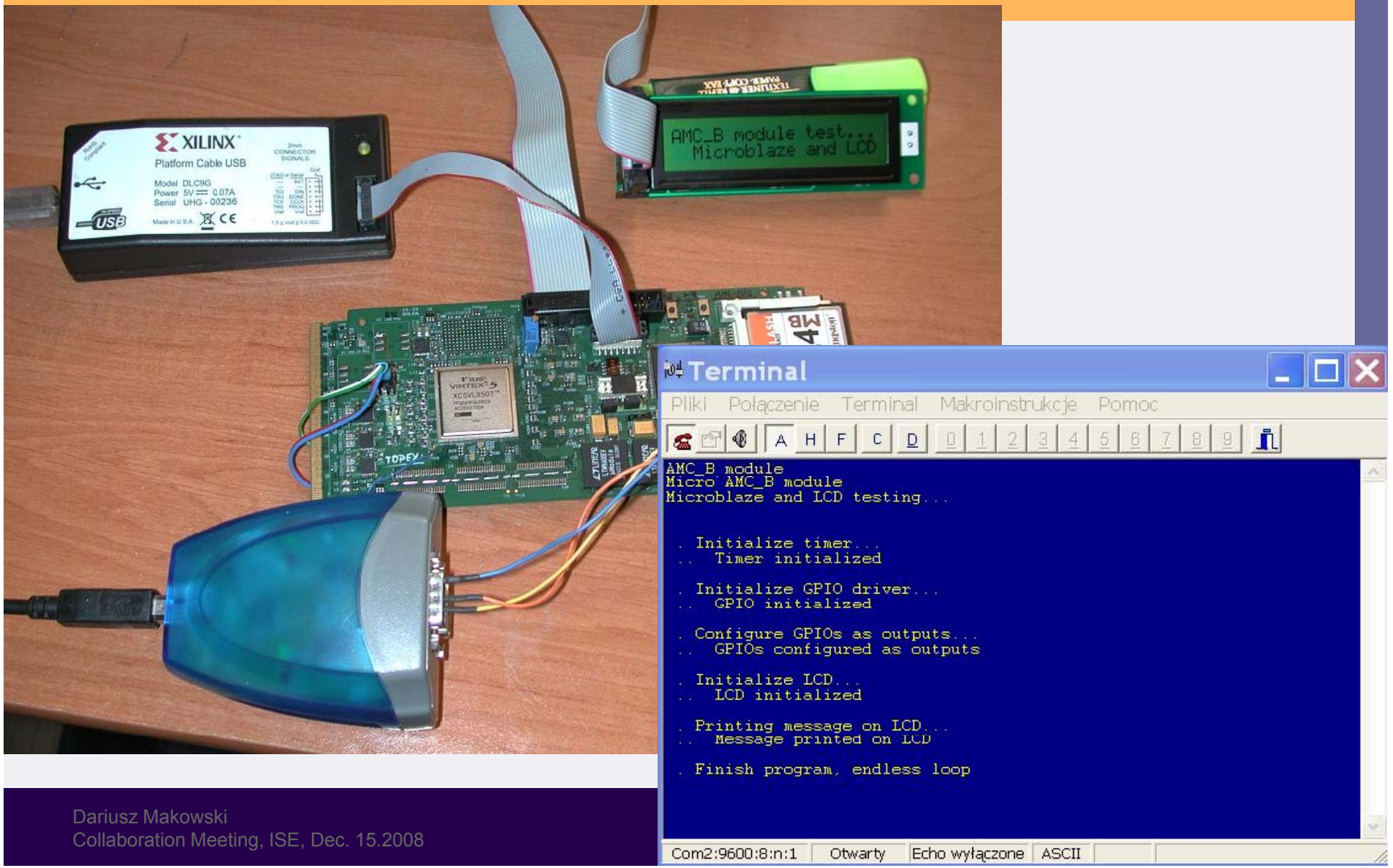
Subtask / Item	Progress	Deliverable	Res. person	Problems
Development of software for TEWS 900 module (ADC, FIFO, configuration registers, PCIe endpoint, DMA, DDR II)	80%	Source codes for TEWS 900 firmware. The codes will be tested during September tests at DESY.	Grzegorz Jabłoński	
Integral Interface for PCIe	100%	Source code for the Integral Interface generator, producing the VHDL template and C header files for communication with the control modules implemented in VHDL.	Grzegorz Jabłoński	
Design and implementation of PCI express communication in DOOCS environment (drivers, client-server applications)	90%	Source code for client-server application responsible for reliable communication between PCI Express driver and external TCP/IP servers. Source code for Linux driver responsible for reading and writing data directly from PCI Express devices.	Adam Piotrowski	
AMC-based Radiation monitoring detector	55%	Single AMC_A prototype board with RadFET and SRAM-based radiation sensors.	Piotr Krasiński (Dariusz Makowski)	
Development of software for AMC_B module	80%	A set of VHDL codes for Virtex V5 will delivered.	Dariusz Makowski	Long delay with AMC_B
Tasks moved to the next year				
Development of software for AMC_A Vector Modulator module	0%	A set of VHDL codes for Virtex V5 will delivered.	Dariusz Makowski	Long delay with AMC_B
Development of software for AMC_A Timing Module	0%	A set of VHDL codes for Virtex V5 will delivered.	Dariusz Makowski	Long delay with AMC_B
Development of PCIe drivers for ATCA carrier	0%	Source codes for low level drivers for the first version of carrier board	Dariusz Makowski	Long delay with carrier
Development of IPMI software for Renesas microcontroller	0%	Software and low level drivers for Renesas M16C65 microcontroller for ATCA-IPMI carrier board.	Dariusz Makowski	
Application for management and monitoring of ATCA devices using IPMI standard (software)	0%	Application with GUI for PC computer and set of procedures written in C/C++ will be delivered. ATCA carried in version one with IPMC controller will be used as a demonstrator.	Dariusz Makowski	
Preparation of requirements for radiation monitoring	25%	Requirements for Radiation Monitoring in the form of Enterprise Architect project file.	Dariusz Makowski	
Distributed radiation monitoring system	-	The architecture of the distributed radiation monitoring system will be delivered. Supervising device with exemplary three detector nodes and CAN cable will be delivered. The system is going to be tested in Linac II accelerator (if it possible, if not in	Dariusz Makowski	No carrier
Application for data acquisition from AMC-based RadMon detectors	-	The application for IPMC, Power Quick processor and Linux operating system will be delivered.	Dariusz Makowski	No carrier

Development of software for AMC_B module

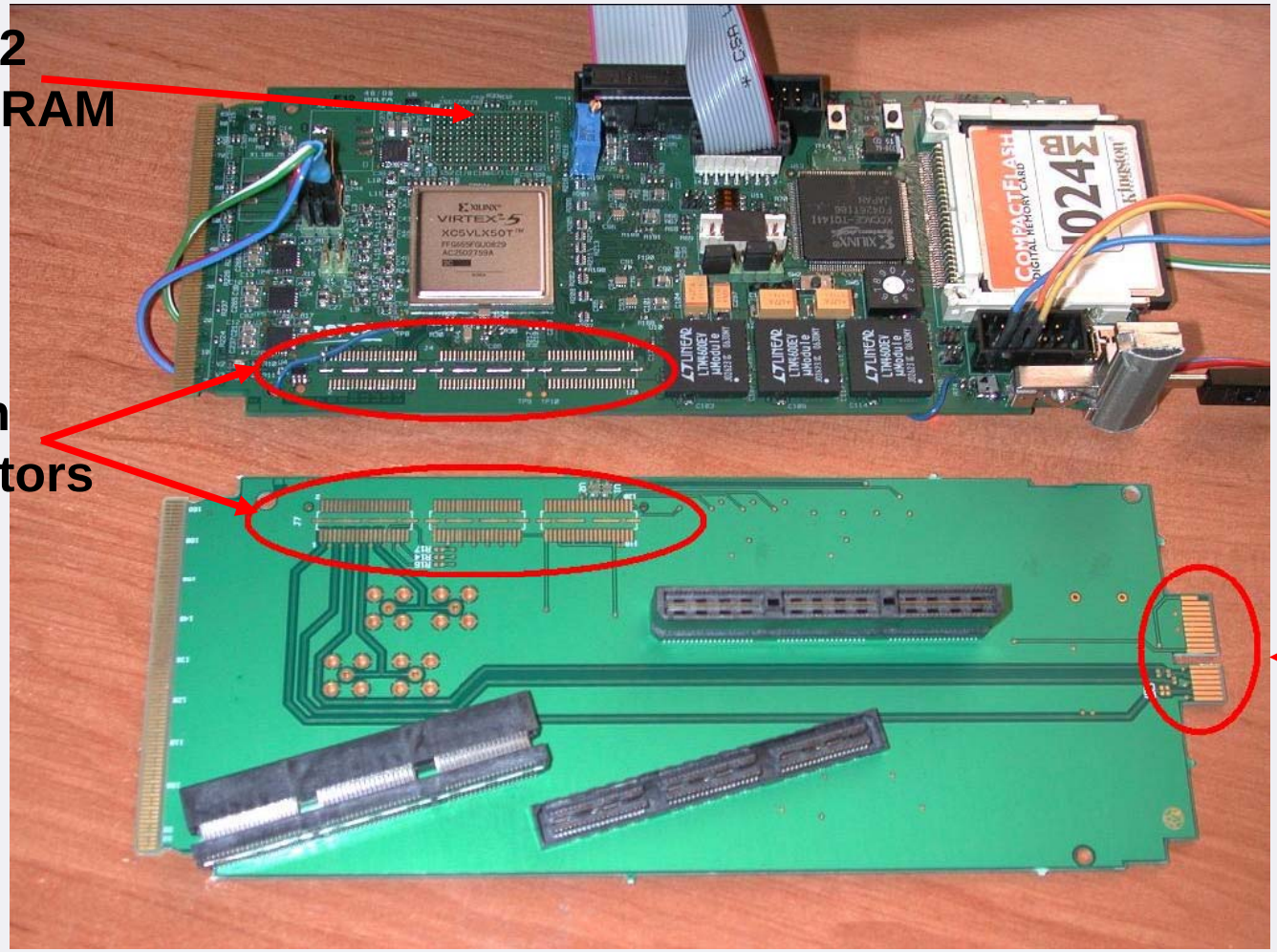
Development of software for AMC_B module



Development of software for AMC_B module



Development of software for AMC_B module - problems



Development of software for AMC_B module - summary

Already tested:

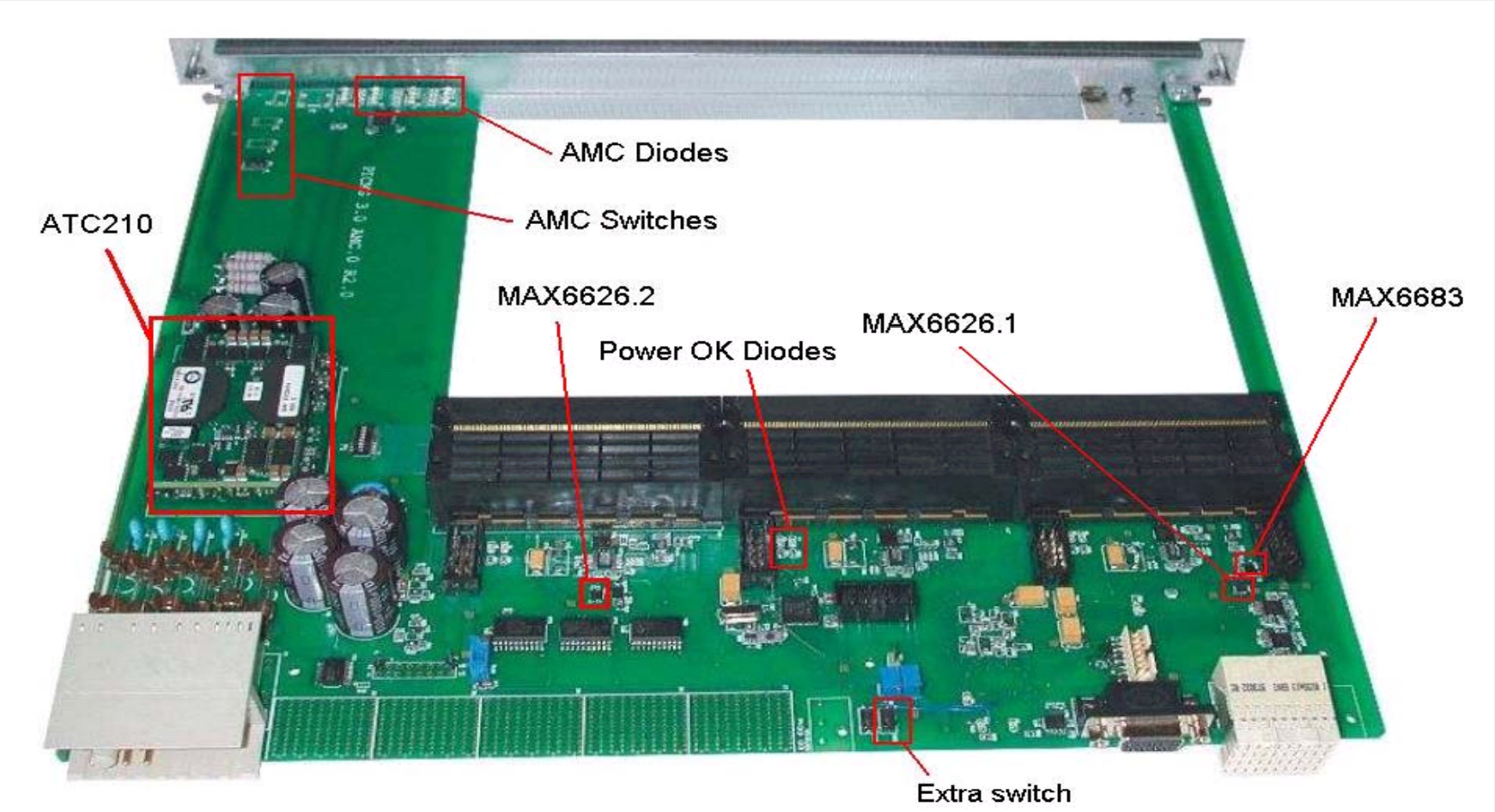
- Power supply is in operation:
- (**+1 V, +2V5, +3V3**, +1V1, 2x +1V2, +1V5, +1V8, +5V, +12V),
- Reference clock 33 MHz, 100MHz
- FPGA and microcontroller are in operation (programming, UART, IOs, LCD)
- SystemACE is in operation

Under development:

- DDR2 SRAMs and DRAMs have not yet been tested (devices not soldered)
- PCIe not tested (no connector, no carrier-board with AMC bays)

Development of diagnostic application for ATCA carrier board

Development of diagnostic application for ATCA carrier board



Development of diagnostic application for ATCA carrier board

```
>> help

Available commands:
help
reset
diodes
switches
pgood
pflags
presence
poweron
enable
adc
fpgapower
i2cenable
extraswitch
temperature
voltage
current
control
geoadd

Type 'command help' for more inf

>>
```

```
>> temp r MAX6626.1 a

Temperature reading             : 44.7500 C     Raw = 0x1660
Thigh register value            : 70.0 C        Raw = 0x4600
Tlow register value             : 65.0 C        Raw = 0x4100

>> volt r MAX6683 a

2.5 V Voltage reading           : 2.509 V       Raw = 0xc1
1.8 V Voltage reading           : 1.172 V       Raw = 0x7d
5 V Voltage reading             : 3.640 V       Raw = 0x8c
Vcc Voltage reading             : 3.320 V       Raw = 0xc1
High 2.5 V voltage limit        : 2.743 V       Raw = 0xd3
High 1.8 V voltage limit        : 1.978 V       Raw = 0xd3
High 5 V voltage limit          : 5.486 V       Raw = 0xd3
High Vcc (3.3 V) voltage limit  : 3.629 V       Raw = 0xd3
Low 2.5 V voltage limit         : 2.249 V       Raw = 0xad
Low 1.8 V voltage limit         : 1.622 V       Raw = 0xad
Low 5 V voltage limit           : 4.498 V       Raw = 0xad
Low Vcc (3.3 V) voltage limit   : 2.976 V       Raw = 0xad

>>
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Preparation of requirement for Digital Feedback

Preparation of requirement for Digital Feedback

XFEL project

Specification for
WP 02 (LLRF)

ATCA carrier board for LLRF system
WP 2.3

Work package delivery number	LLRF WP 2.3.11
Responsible author	Dariusz Makowski
Name of faculty/institution:	TUL, DESY
Date:	December 1, 2008
Report revision:	2.0
Reviewer 1:	
Reviewer 2:	

Preparation of requirement for Digital Feedback

Table of contents

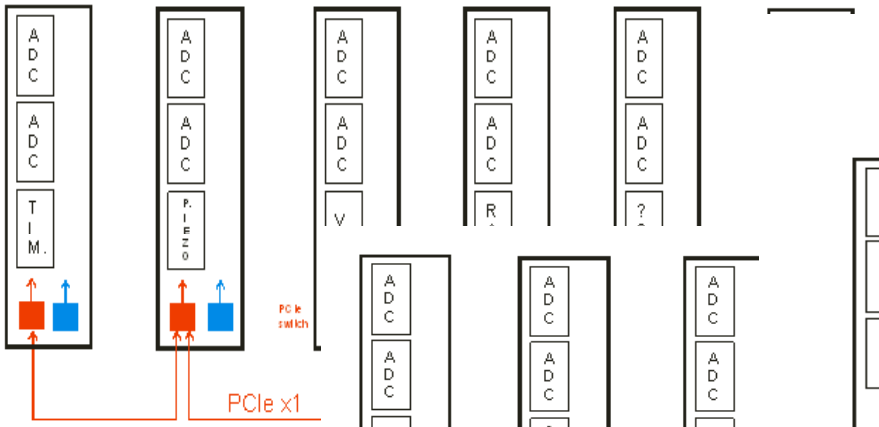

Figure 1A. A block diagram of tl

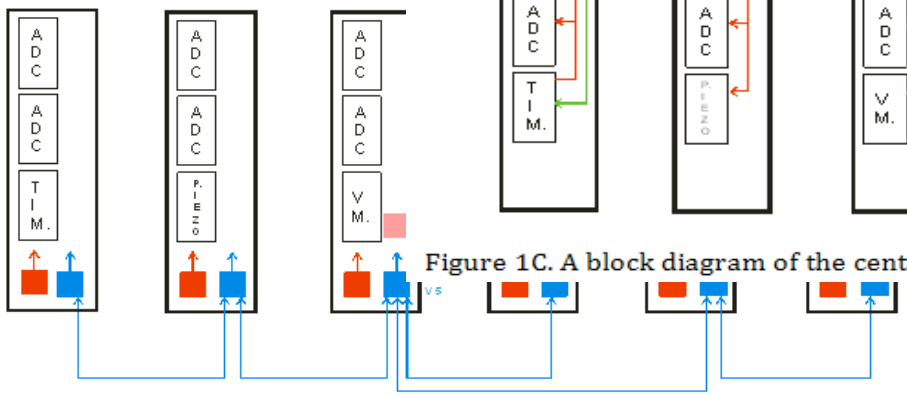

Figure 1B. A block diagram of the centralised controller – low latency links.

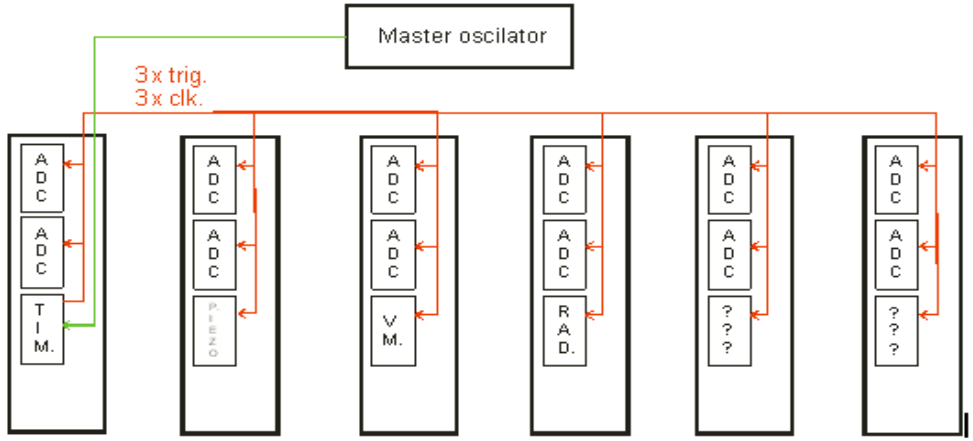

Figure 1C. A block diagram of the centralised controller – clock and trigger distribution.