Development of Software for TEWS TAMC900 Module

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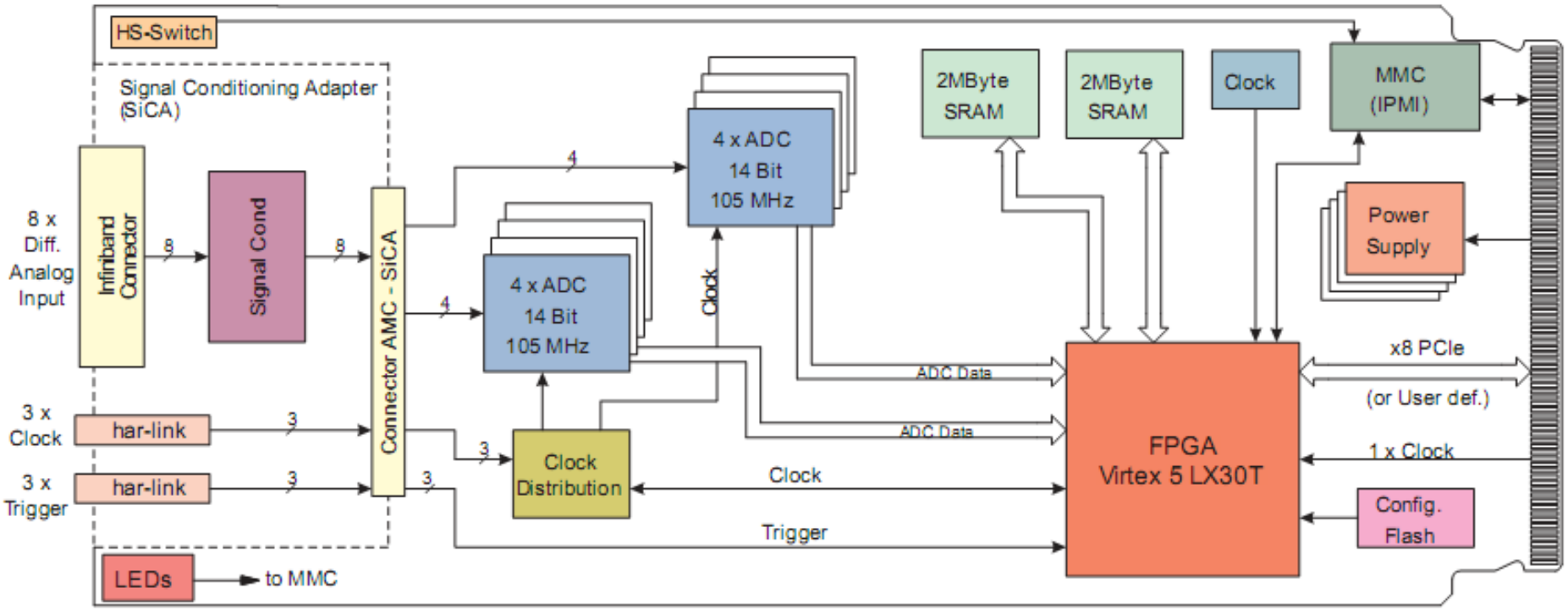
Overview

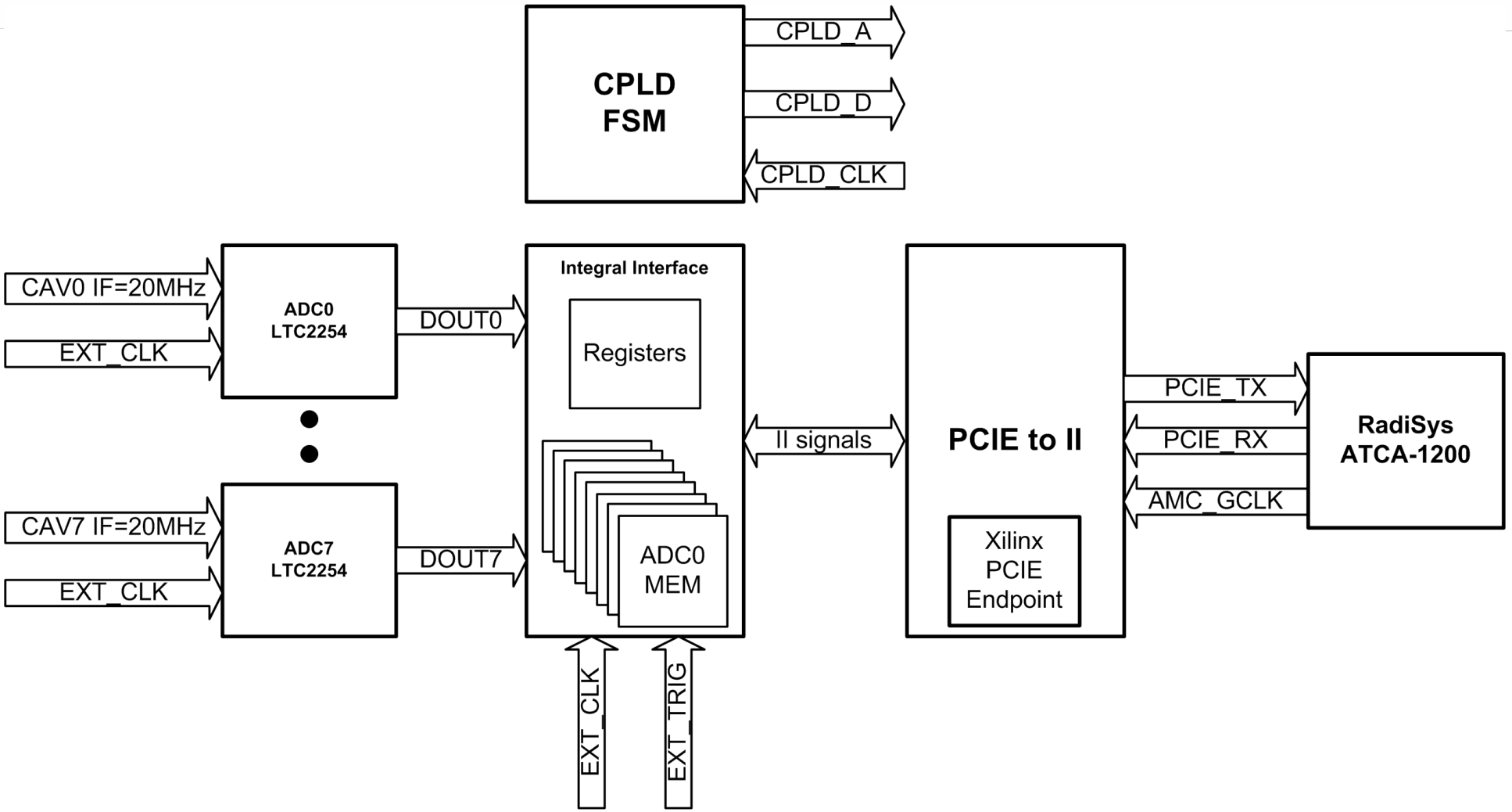
- *The TAMC900 board is a high speed analog-to-digital signal converter AMC.*
- *It consists of 8 fast LT2254 ADCs, Virtex-5 FPGA and 4MB of QDR-II SRAM.*
- *Data from ADCs can be transmitted to the CPU by up to 8X PCI Express link.*
- *The configuration of the on-board peripherals is maintained by XC95144XL CPLD.*

Block Diagram

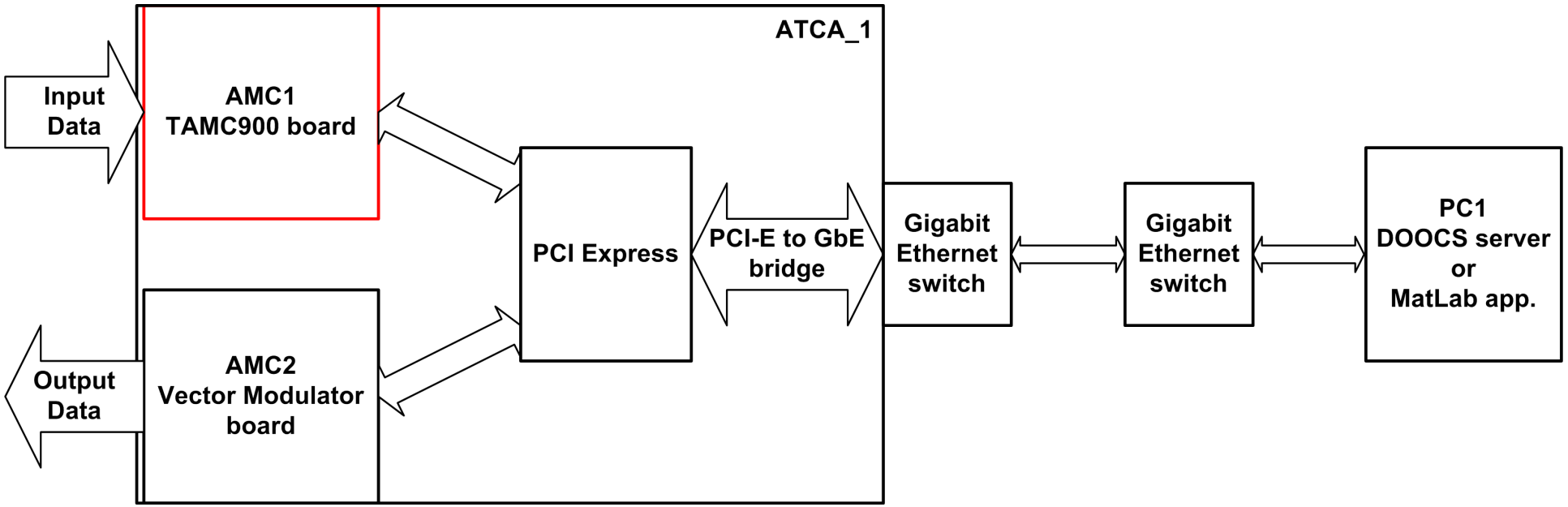


- ***The TAMC900 provides three clock inputs and three trigger inputs.***
- ***The three external clock inputs and the PCI Express reference clock are routed to a flexible clocking scheme that allows independent clocking of the ADCs in two groups.***
- ***The trigger inputs are routed directly to the FPGA.***

Software Block Diagram

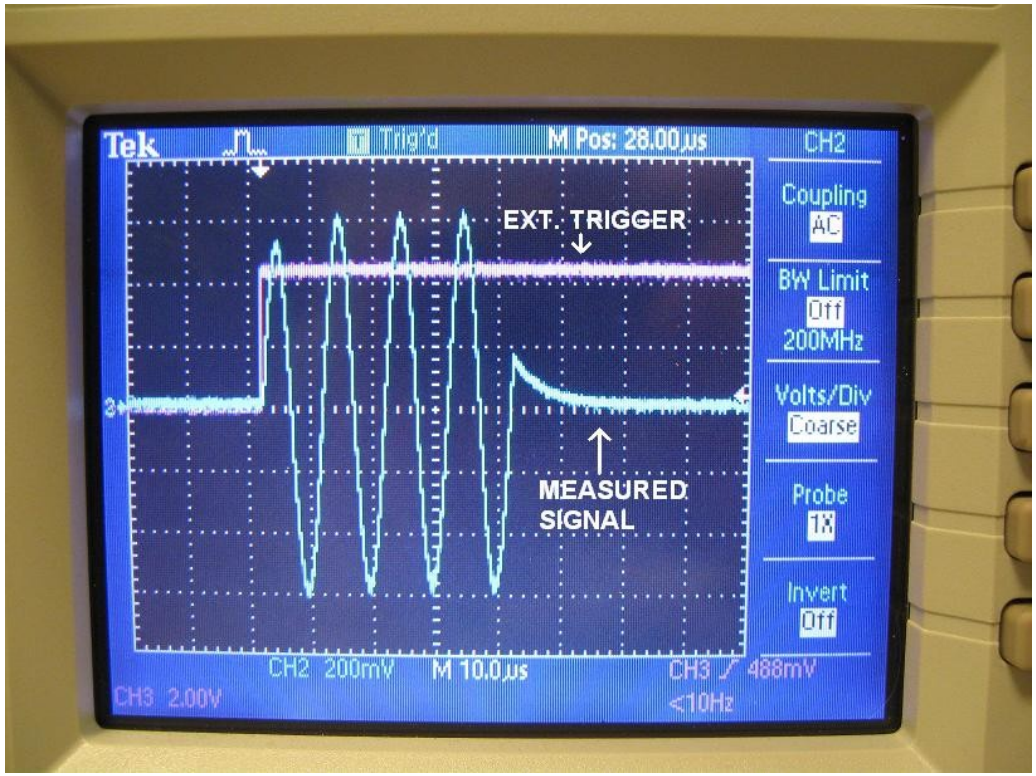


TAMC900 As A System Component



Tests

- ***Tested in the lab with the Radisys 1200 Board***



- ***Tested with accelelator signals with ADLINK ATCA-6900 Blade***

Current Status

- *Communication via PCIe with the board has been established*
- *ADC converters are working correctly*
- *The data acquisition application has been tested*
- *The tests were successfull*
  - *sampling at 81 MHz not yet tested*