Week's summary

25 August 2016

W.T. Fedorko on behalf of the team

Summary of Activities

- ABCN' Emulation (Kevin):
  - Completed a loopback setup with NexysV
    - 'Mini'-CHESS II emulator still used
  - Working on port to ML605 to support 3-CHESS II configuration
    - Fighting with Ethernet cores
  - Last week of work...

Summary of Activities

- Adaptor Card (Dave with input from Jaya John, Wojtek, Colin):
  - Collectively arrived at strategy which should support several available dev-kits:
    - Nexys V, ML605, Genysys 2, KC705, VC707, VC709
    - Bank LA (LPC) will carry all signals to lower array as well as all SACI, SPI and (single ended) CHESS?_CLK40
    - Remaining LA pairs and HA bank will carry LVDS signals from/to upper two arrays
      - Middle array 'split' between LA and HA; no indication of line length matching within banks anyway on most boards; HB not supported on KC705; HB would need additional powering scheme
    - Voltage translators will be needed since CHESS II only speaks 3.3 V and we can only do LVCMOS 2.5 out of the FPGA banks (1.8 V on the VC70x); decided to add voltage translators to SPI also.
      - Preliminary choice: http://www.ti.com/product/sn74avc4t234
        - Inconvenient package – better suggestions?
      - Need to suply VCC_A to the translator; on all boards checked the same supply that drives the FMC I/O banks connects to VADJ pins on FMC– so translation should automatically match the FPGA signalling levels
    - Orientation of connectors specified by Larry
    - Dave progressing with design/layout