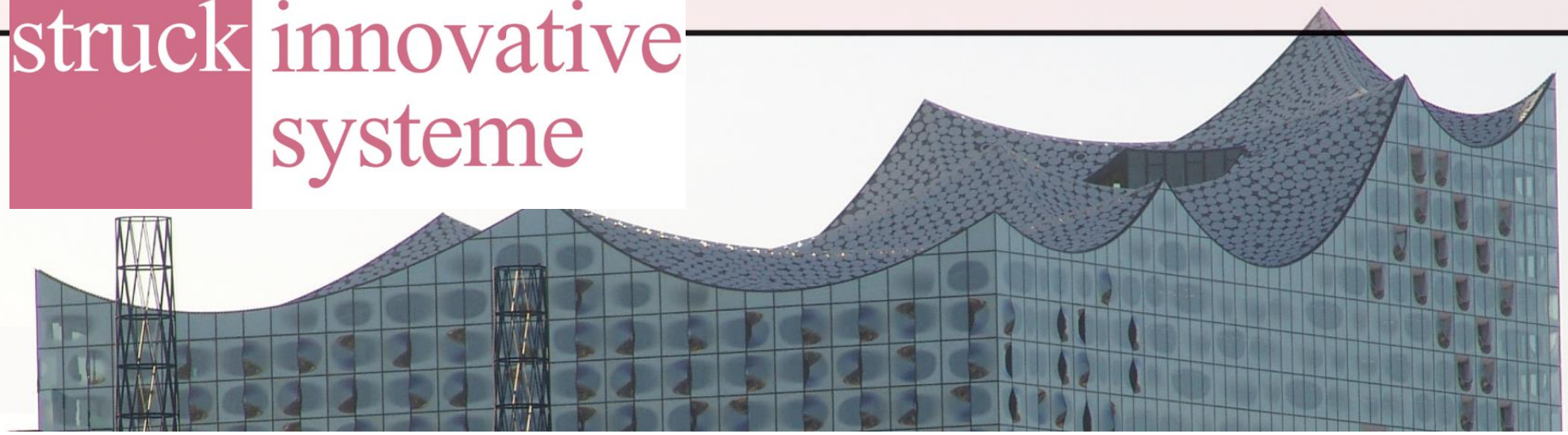
struck innovative systeme



Kintex Ultrascale based MTCA digitizer cards, the SIS8300-KU and beyond

Dr. Matthias Kirsch

SIS8300-KU
10 channel 125 MSPS 16-bit digitizer
(250 MSPS 14-bit stuffing option)

History

Virtex 5 based

2010 SIS8300 initial development, first MTCA.4 board

2011 SIS8300 V2 > 340 units in field (in part 8 channel 250 MSPS 14-bit BPM)

Virtex 6 based

2014 SIS8300-L > 150 units in field

2015 SIS8300-L2x > 750 units in field (L2S, L2D,…)

SIS8300-KU

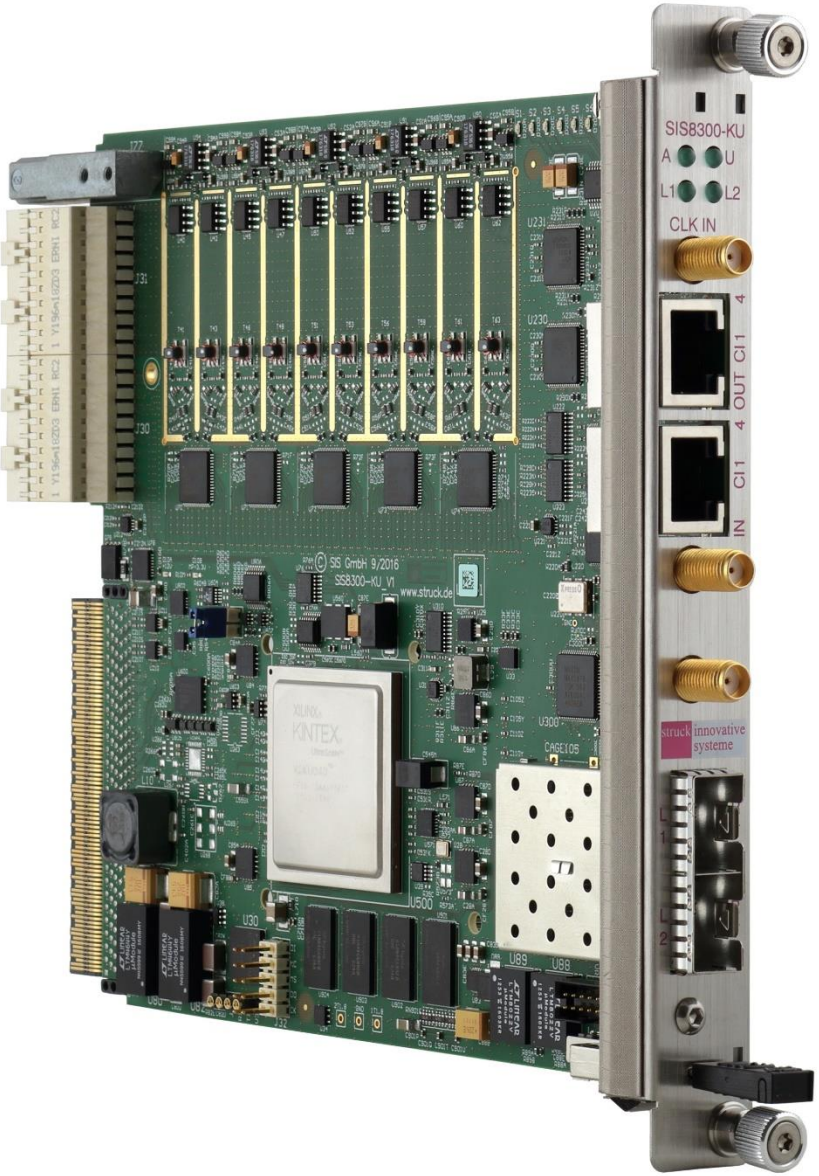
First of all thanks to:

Lund University
For driving the development with the initial 5 unit order and a development cost contribution

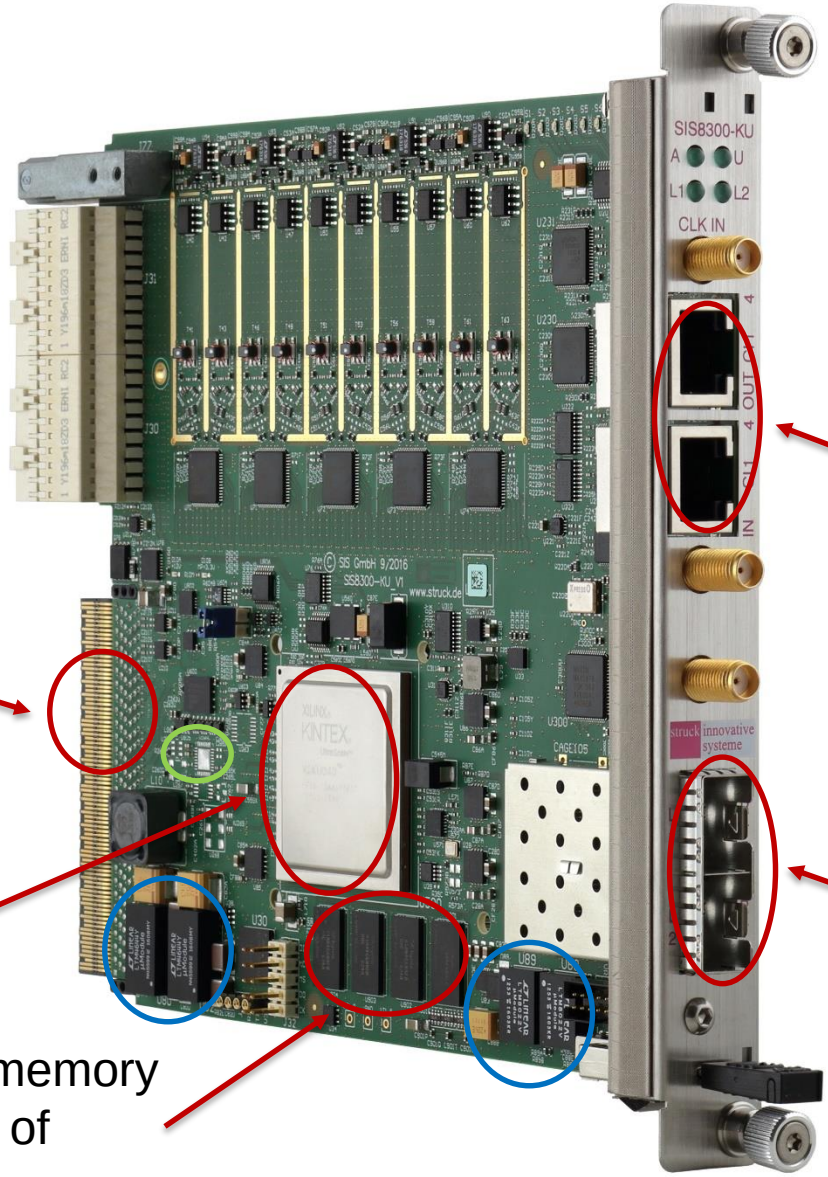
DESY
For continued support with the SIS8300-x developments. In particular KU power supply development considerations and upcoming SIS8300-KU/DWC8300 LLRF qualification (amplitude and phase noise, time jitter and amplitude stability)

Andreas Grüttner
For yet another ready to ship Rev. 1 schematic and layout

One of the first 10 SIS8300-KU‘s



SIS8300-KU versus L2 changes



New Power Supply Scheme

WR Option

RJ45 I/O instead of Harlink

PCIe Gen3 instead of Gen1/2

Kintex Ultrascale instead of Virtex 6

SFP+ instead of SFP

DDR4 memory instead of DDR3

SIS8300 Properties
(refer to flyer in conference bag also)

- 10 Channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s Per Channel Sampling Speed
- AC or DC Input Stage
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit 250 MS/s DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Multi Gigabit Link Port Implementation to Backplane
- Twin SFP+ Card Cage for High Speed System Interconnects
- White Rabbit Clock Option for SFP+ Ports
- Two RJ45 Connectors (One Clock + 3 Data or 4 Data In/Out)
- XCKU040-1FFVA1156C Kintex Ultrascale FPGA
- 2 GByte DDR4 Memory (flexible partitioning scheme)
- 4 lane PCI Express Gen3 Connectivity
- Dual boot
- MMC1.0 under DESY license LV91
- In Field Firmware Upgrade Support
- Zone 3 class A1.0, A1.0C or A1.1CO Compatible

Technical Aspect I: PCB Layer Stack

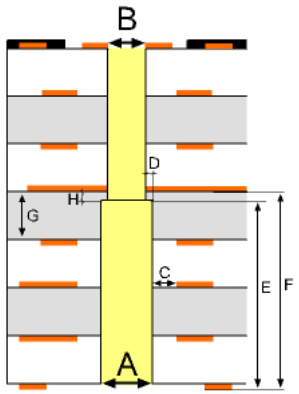
			CU	PP = Pregreg		nominale		geschätzte
			Aufgabe	LA = Laminat		unverpresste	Copper	verpresste
	Layer / Kerne /Prepreg	Mat.	Verwendung	Mat.-Bez.	Style / Dicke	Stärke(µm)	Coverage %	Stärke(µm)
		Lötstop				25		25
	17+25 galv. Cu L1	Cu-Folie	Signal			37	100 fix	37
	3313	Prepreg		FR4 PP 1650 V	3313 / 104µ	102		101
	L2	Cu	Powerplane			35	78	35
	Core 50um + 35um CU	Laminat		FR4 LA 1755 V	106 / 50µ	50		50
	L3	Cu	Powerplane			35	76	35
	3313	Prepreg		Megtron PP R-5670	3313 / 98µ	98		94
	L4	Cu	Signal			18	43	18
	Core 100um + 18um CU	Laminat		Megtron LA R-5775	3313 / 100µ	100		100
	L5	Cu	Signal			18	42	18
	3313	Prepreg		Megtron PP R-5670	3313 / 98µ	98		94
	L6	Cu	Powerplane			18	77	18
	Core 100um + 18um CU	Laminat		Megtron LA R-5775	3313 / 100µ	100		100
	L7	Cu	Signal			18	42	18
	3313	Prepreg		Megtron PP R-5670	3313 / 98µ	98		91
	L8	Cu	Signal			18	43	18
	Core 100um + 18um CU	Laminat		Megtron LA R-5775	3313 / 100µ	100		100
	L9	Cu	Powerplane			18	76	18
	3313	Prepreg		Megtron PP R-5670	3313 / 98µ	98		94
	L10	Cu	Signal			18	41	18
	Core 100um + 18um CU	Laminat		Megtron LA R-5775	3313 / 100µ	100		100
	L11	Cu	Signal			18	42	18
	3313	Prepreg		Megtron PP R-5670	3313 / 98µ	98		94
	L12	Cu	Powerplane			35	77	35
	Core 50um + 35um CU	Laminat		FR4 LA 1755 V	106 / 50µ	50		50
	L13	Cu	Powerplane			35	78	35
	3313	Prepreg		FR4 PP 1650 V	3313 / 104µ	102		101
	17+25 galv. Cu L14	Cu-Folie	Signal			37	100 fix	37
		Lötstop				25		25
						1602		1577
							Werte aus CNC20539	

Megtron 6 layers because of Gen3 PCIe and SFP+ speeds

Maintain FR4 on outer layers for „hand“ configuration soldering

Note: like all SIS8300-x PCBs produced by Heger in Norderstedt

Technical Aspect II: Backdrilled Vias

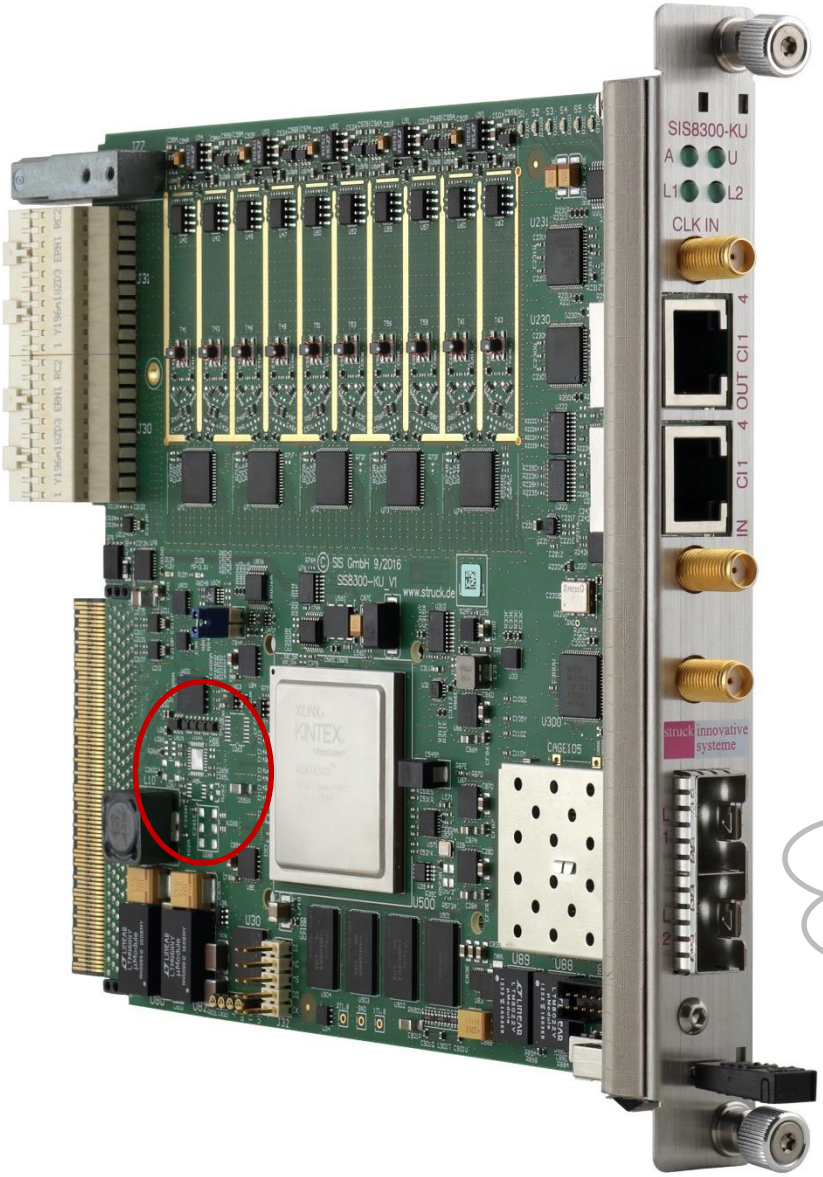


Decreasing via stub length by backdrilling significantly reduces a particularly problematic form of signal distortion called deterministic jitter. Because Bit Error Rate (BER) is strongly dependent on deterministic jitter, any reduction in deterministic jitter by backdrilling will significantly reduce the overall BER of the interconnect – often by many orders of magnitude. Other key advantages to backdrilling PTH vias include less signal attenuation due to improved impedance matching, increased channel bandwidth, reduced EMI/ EMC radiation from the stub end, reduced excitation of resonance modes and reduced via-to-via crosstalk.

48 backdrilled vias for 4 PCIe lanes and SFP+ MGTs

Drawing source: www.multi-circuit-boards.eu
Text source: www.sanmina.com

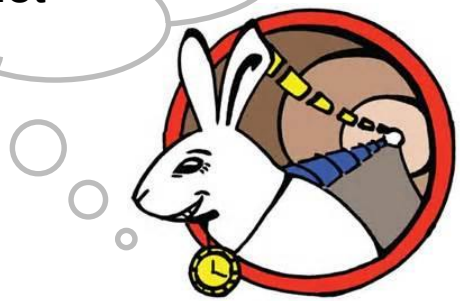
SIS8300-KU White Rabbit (WR) Ready



- PLL Clock Synthesizer
- VCO, VCXO
- DACs for VCO Control
- Additional Power

No known Kintex Ultrascale White Rabbit PTP Core (WRPC) yet

What is WR?
Sub ns synchronisation
Synchronous Ethernet
IEEE 1588 PTP



FPGA Resources/Performance

Used FPGA	XC6VLX130T-2FFG1156C (SIS8300-L2)	XCKU040-1FFVA1156C (SIS8300-KU)
System Logic Cells	128 K	500 K
CLB LUTS/Flip-Flops	80/160 K	242/484 K
Block RAM/FIFO w/ECC (36Kb each)	264	600
Block RAM/FIFO (18Kb each)	528	1200
Total Block RAM (Mb)	9.5	21.1
DSP Slices	480	1920
GTH speed	6.6 Gb/s	16.3 Gb/s
PCIe	Gen2	Gen3
Memory Controller	DDR3	DDR4

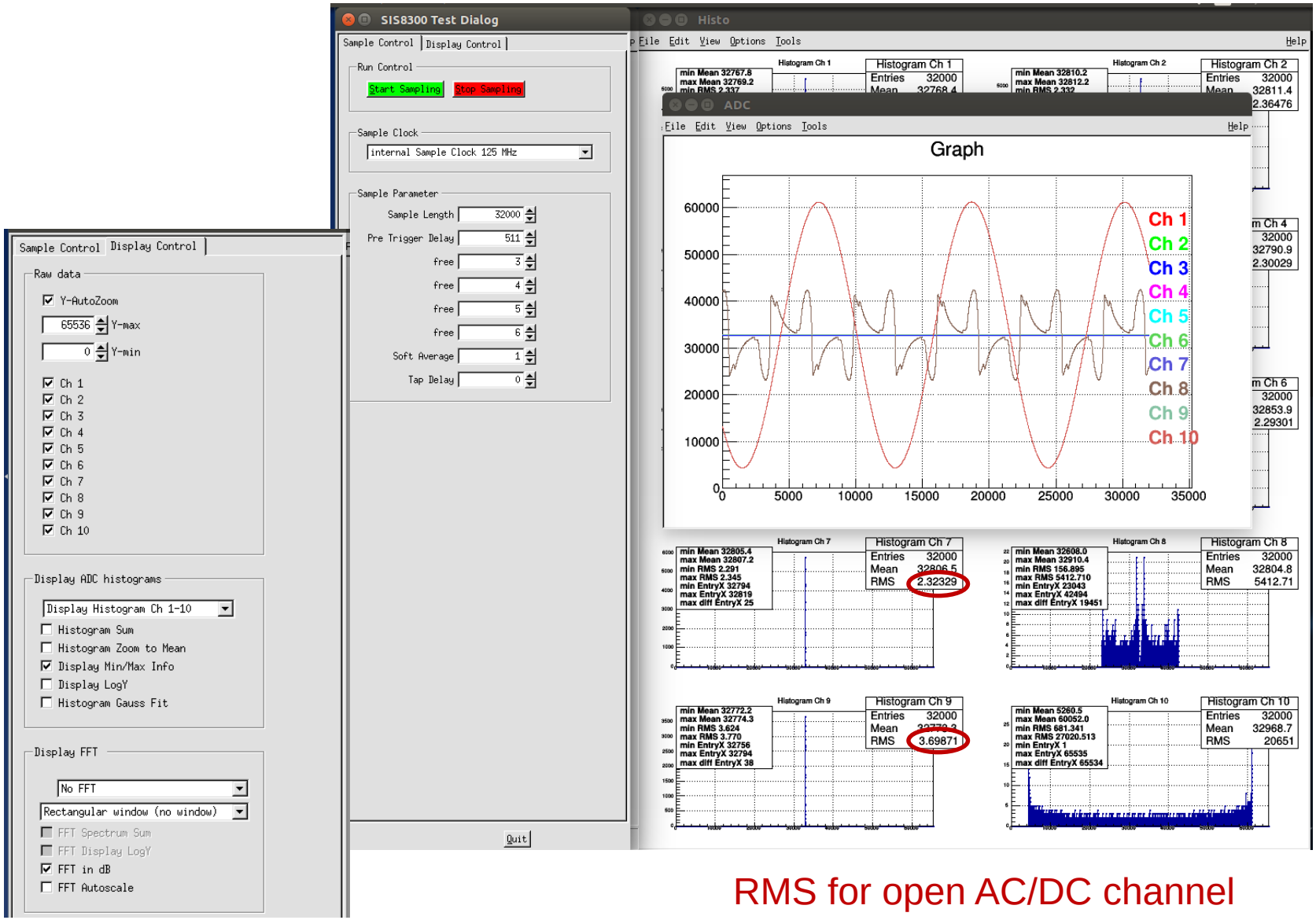
SIS8300-KU to SIS8300-L2

Payload Power Consumption Comparison
Comparable Firmware Design
(currently more memory/diagnostics in KU)

Board Type Firmware Design	SIS8300-L2 8302100F	SIS8300-KU 83039905 (prelim)
Power Up	2,9 A	2,6 A
P2P and FP Link Test	3,1 A (1Gbit/s)	2,8 A (10Gbit/s)
Memory Test	3,2 A	2,8 A
ADC „ROOT“ Test	3,5 A	3,2 A

Conclusion:
About 10% lower at (partially) substantially higher performance

SIS8300-x ROOT GUI
SIS8300-KU 8AC2DC with SIS8900 RTM



RMS for open AC/DC channel

SIS8300-KU Availability

10 Unit Prototype series (all 8AC2DC DZ3 configuration) out of stuffing mid November 2016, all in working order

- First Lund University and ESS/ERIC shipments next week
- One unit for DESY reference/cross L2 measurements
- One reference unit at Struck

Production of initial 20 unit production batch under way

- Xilinx FPGAs confirmed for next week
- PCBs confirmed for week 3 of 2017
- Availability of cards mid February 2017

JESD204B

JEDEC Solid State Technology Association, formerly known as the Joint Electron Device Engineering Council (**JEDEC**)

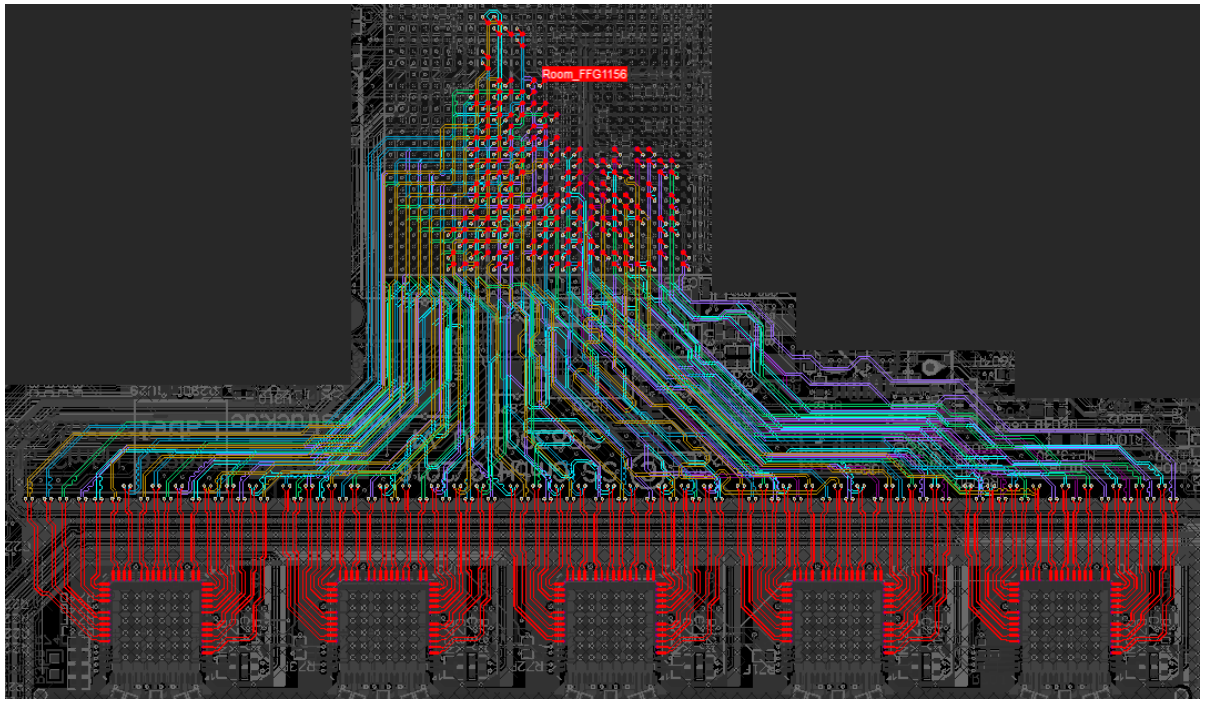
Independent semiconductor engineering trade organization and standardization body

- 2006 JESD204 multigigabit serial data link between converter(s) and a receiver
- 2008 JESD204A multiple aligned serial lanes, lane speed up to 3.125 Gbps
- 2011 JESD204B provisions to achieve deterministic latency, lane speed up to 12.5 Gbps
- Future JESD204C, Line rates from 1 Gb/s to 32 Gb/s and 64B/66B encoding

JESD204B Advantages I
→ basis for many new digitizer chips

Layout/Routing

Classic: 18 differential LVDS signal pairs per dual 125 MSPS 16-bit ADC



JESD: one or two pairs/lanes plus sync.

JESD204B Advantages II
→ basis for many new digitizer chips

- Lower power at higher speeds
- Constant power draw
- No multiple synchronous bit flips
- Serial data stream rather than data to strobe at the right point in time (FPGA tap delay)

Recommended Reading

Analog Devices:
JESD204B Survival Guide

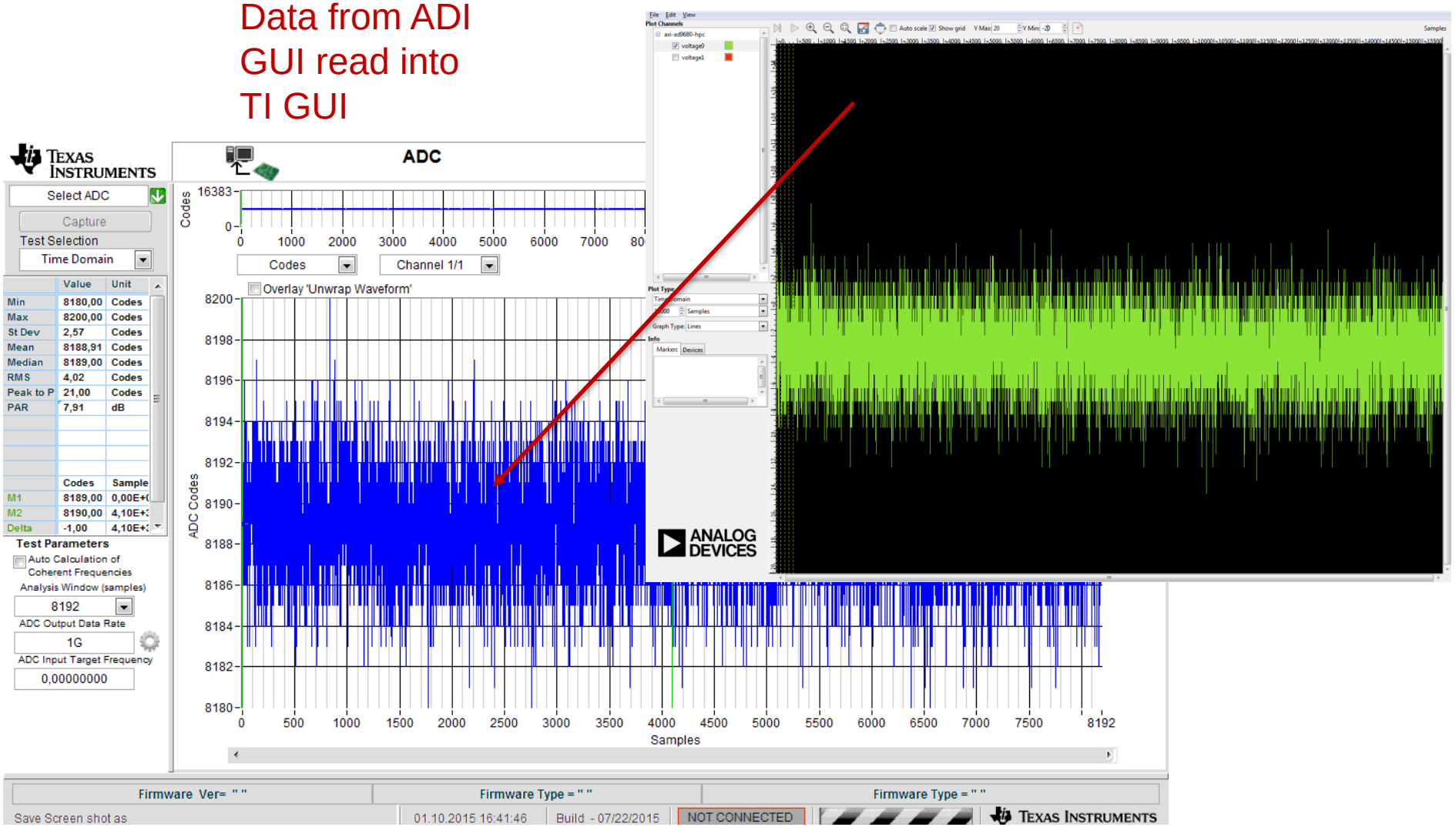
Some High Speed JESD204B Digitizer Chips

Source	Chip	Sampling Speed MSPS	Bits	Chs	BW in MHz	Lanes	PWR per Channel in W
TI	ADS54J54	500	14	4	900	8	0,9
TI	ADS54J60	1000	16	2	1200	4/8	1,4
ADI	AD9680	1000/1250	14	2	2000	4	1,7
ADI	unreleased	2500	14	2	5000	8	1,7

→ XCKU060-1FFVA1156C or “better” required for MGT availability reasons on higher channel count MTCA boards

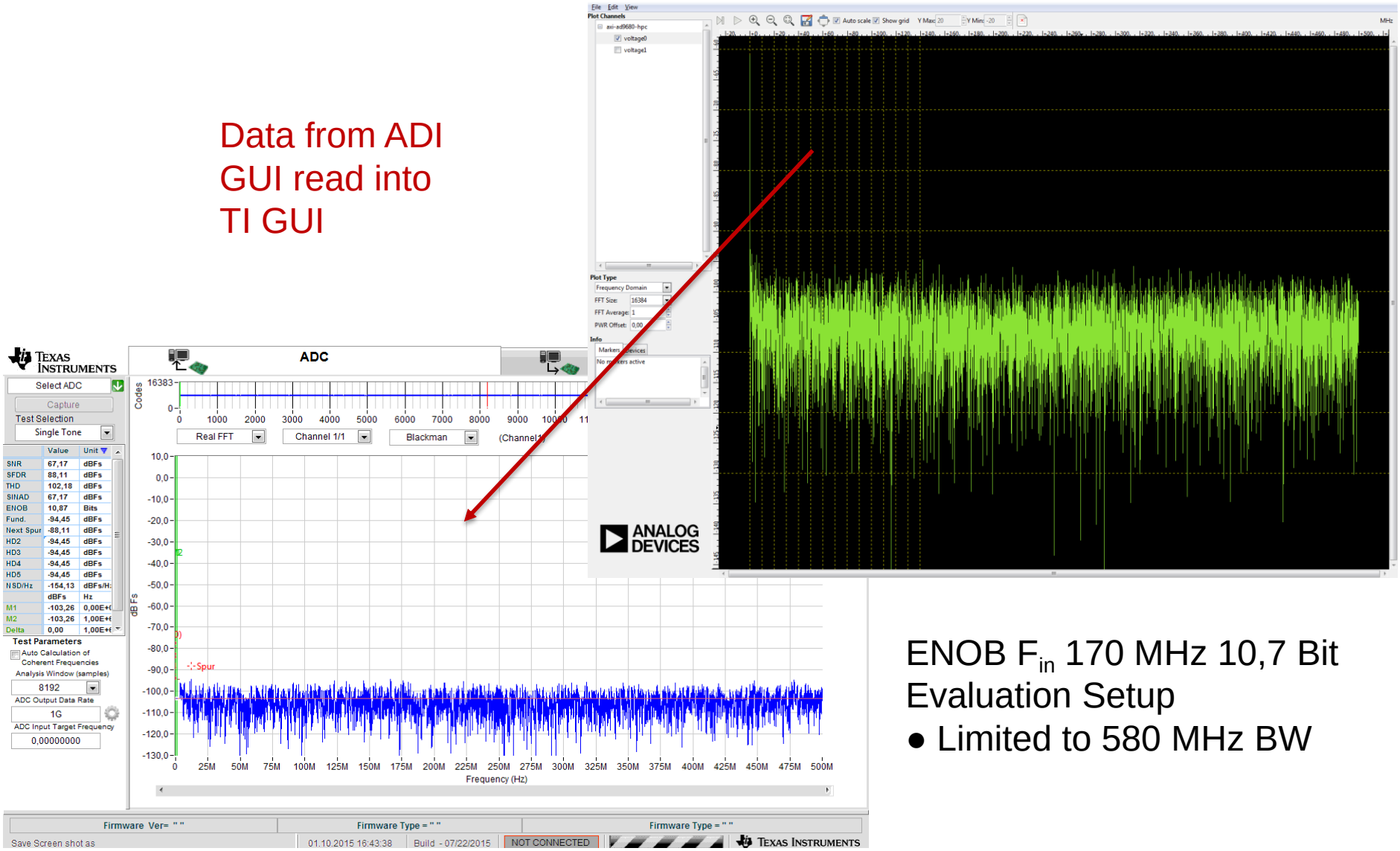
ADI AD9680 Dual GSPS 14-bit Eval Kit (Avnet *AES-KCU-JESD-G*)

Data from ADI GUI read into TI GUI



ADI AD9680 Dual 1000 MSPS 14-bit

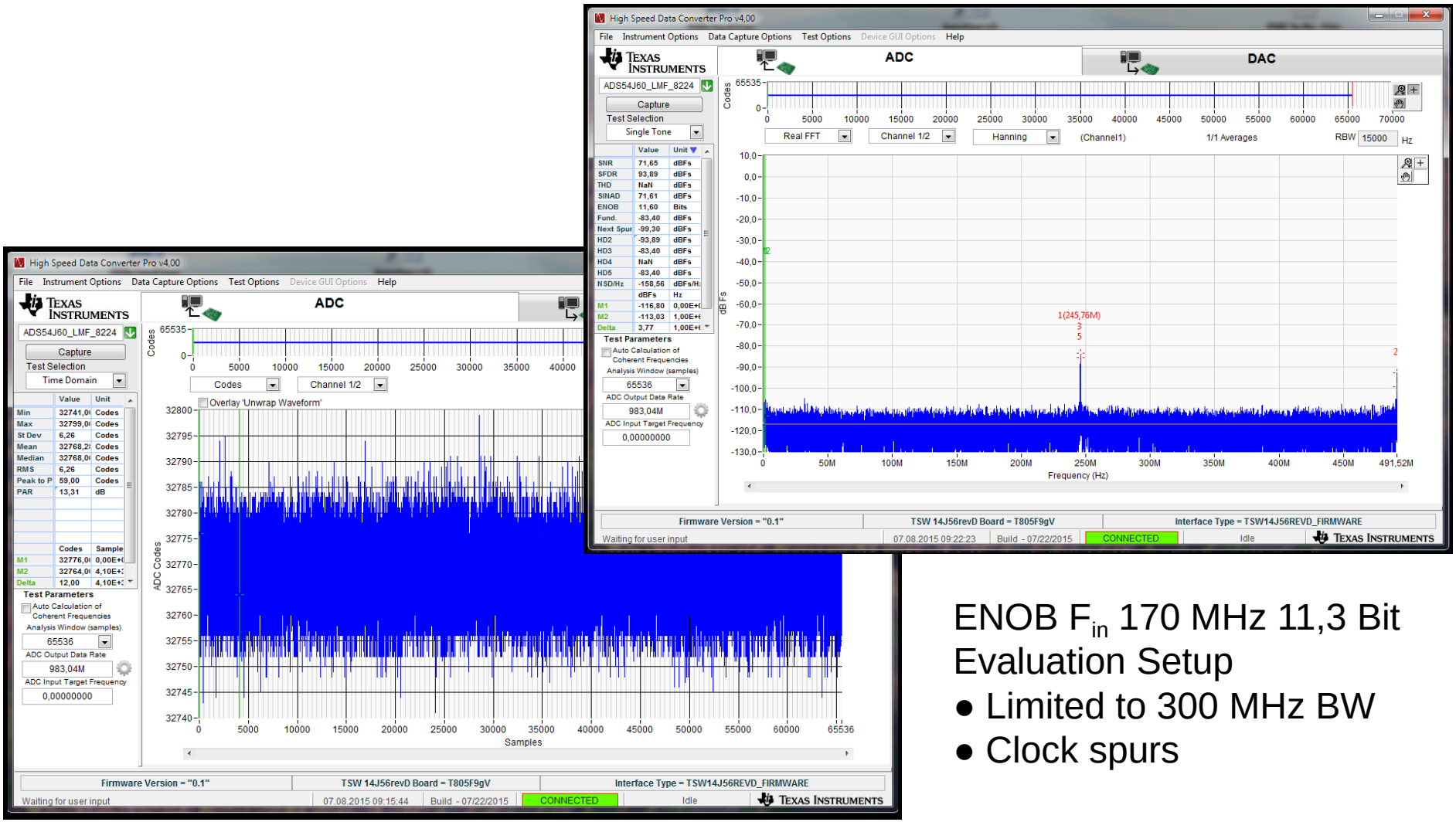
Data from ADI GUI read into TI GUI



ENOB F_{in} 170 MHz 10,7 Bit Evaluation Setup

- Limited to 580 MHz BW

TI ADS54J60 Dual GSPS 16-bit Eval Board (FMC+Intel Arria Carrier)

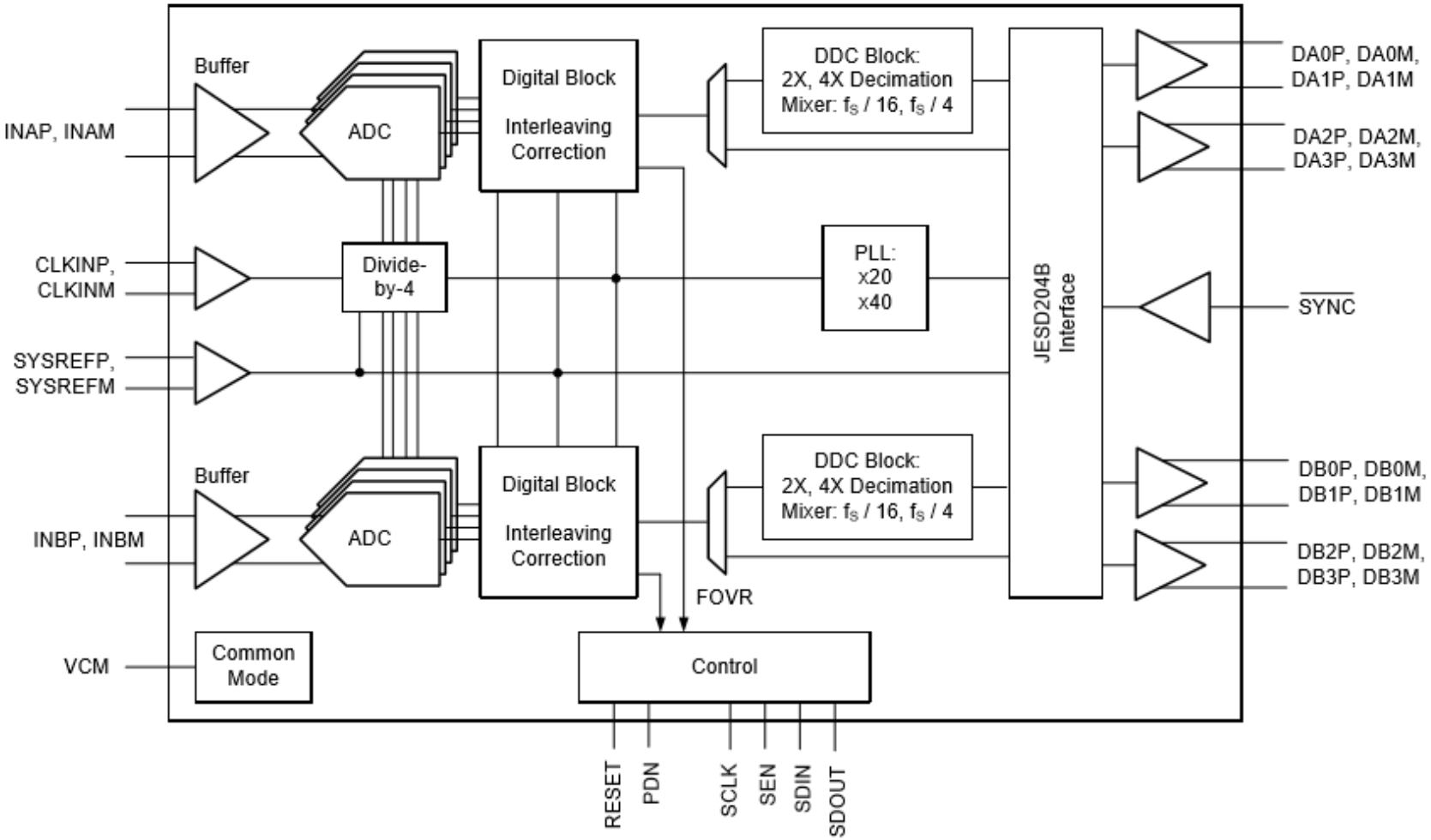


ENOB F_{in} 170 MHz 11,3 Bit

Evaluation Setup

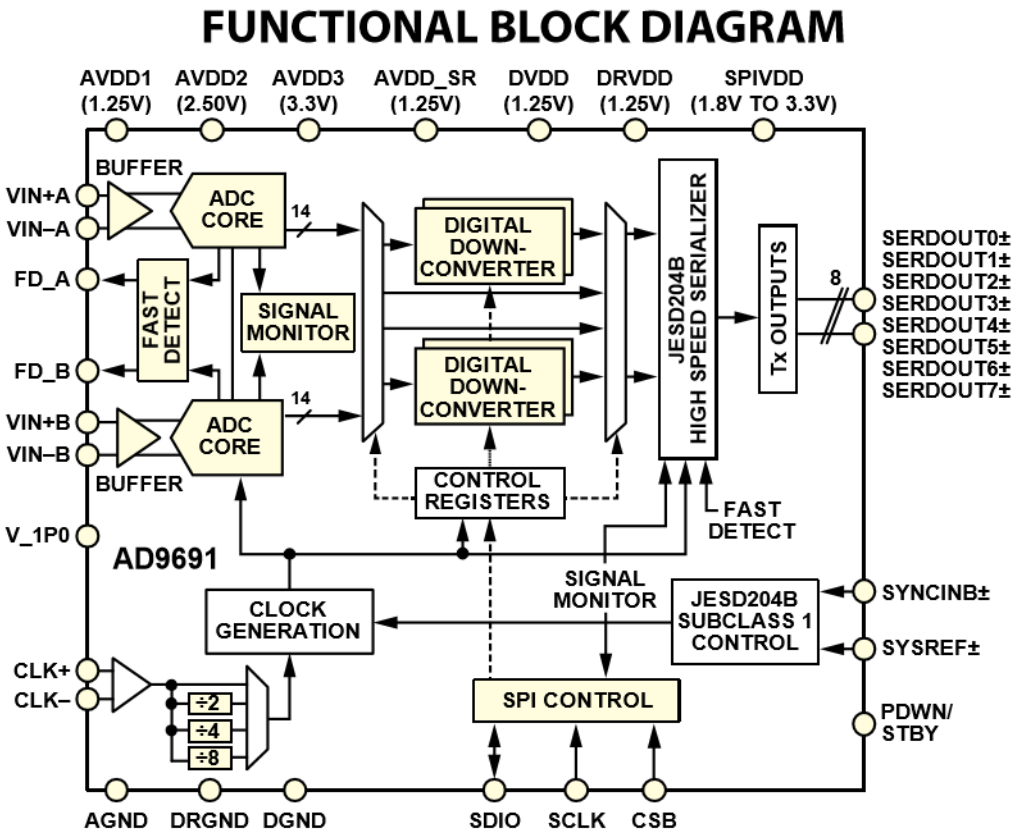
- Limited to 300 MHz BW
- Clock spurs

Architecture Example ADS54J60 (multiple cores)



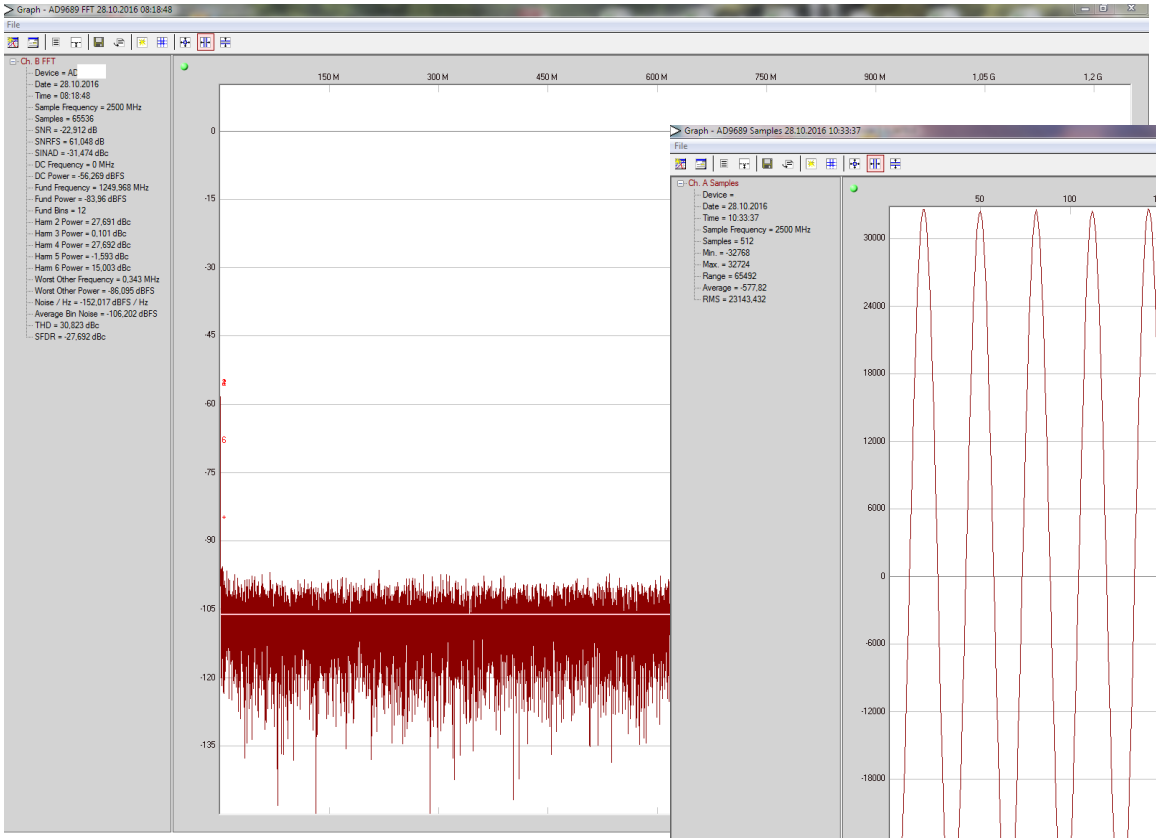
ADI unreleased Dual 2.5 GSPS 14-bit

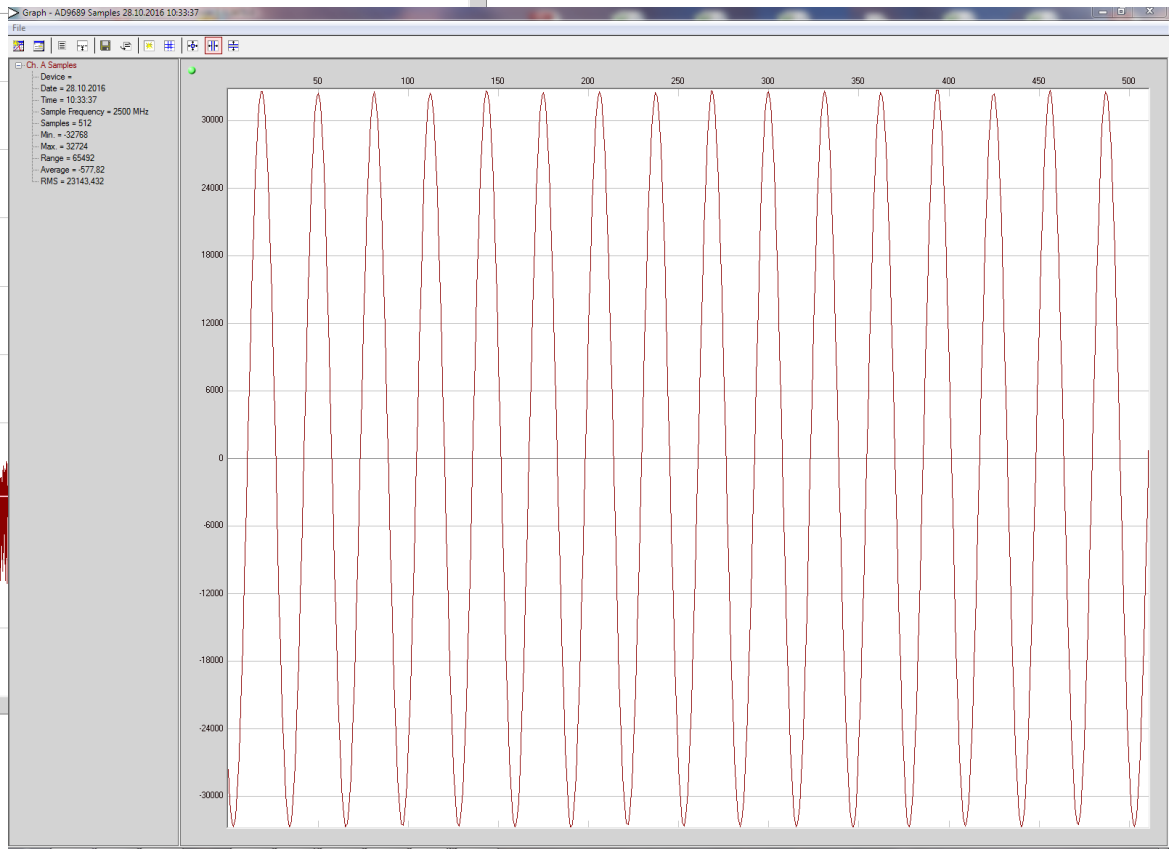
Architecture aequivalent to AD9691



ADI unreleased Dual 2.5 GSPS 14-bit Eval Board („FMC“+Xilinx Virtex 7 Carrier)

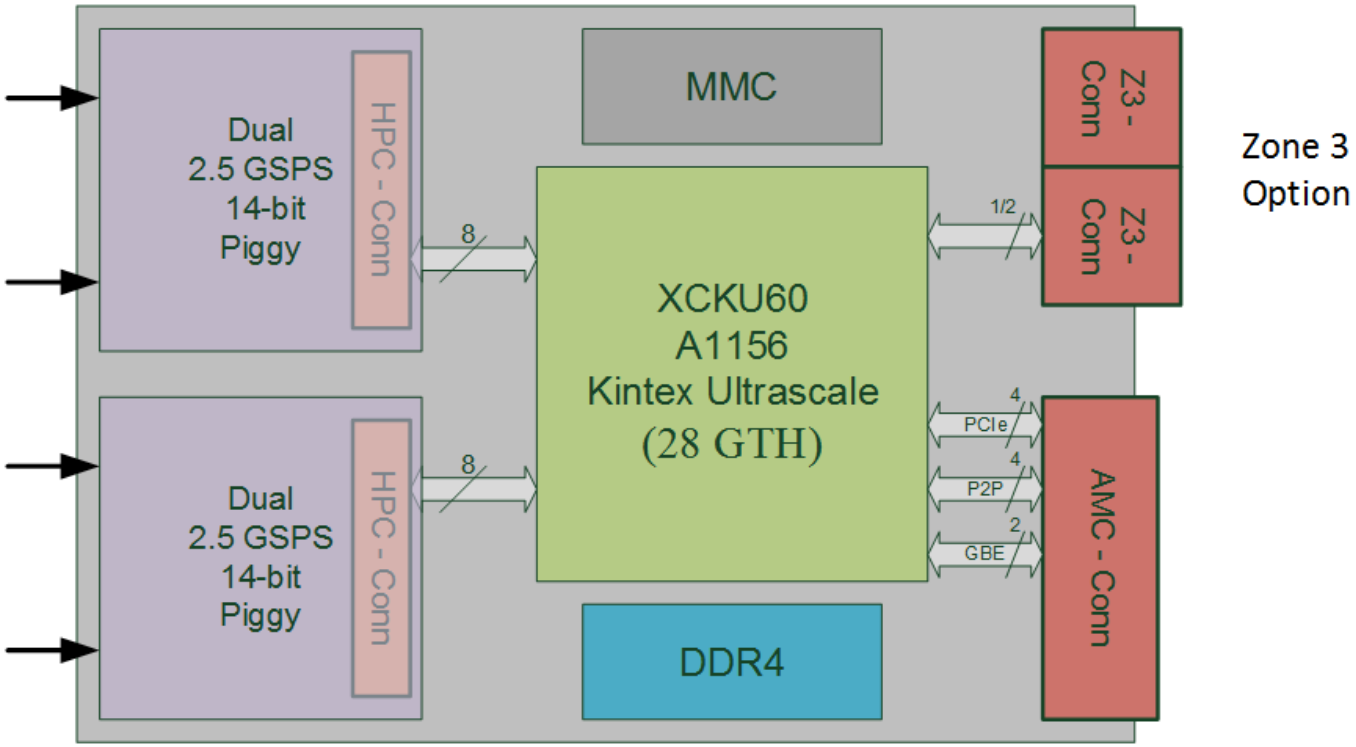
80 MHz sine
Axis scaled to 16-bit





Prelim user manual: f_{IN} = 170 MHz, ENOB = 10,2 bits, analog bandwidth 5 GHz

Possible new MTCA Product
SIS8310 Quad 2.5 GSPS 14-bit Digitizer
(Reduced Dual Channel Option)



Same carrier can be used for 8 channel 14/16-bit GSPS design
FMC or custom tbd.

MTCA.4 Relevance
current Struck user base

AU	Australian Synchrotron*
BR	LNLS*
CN	IHEP Beijing, SINAP
CZ	ELI (Inst of Physics, Praha)
DE	DESY, HZDR, PTB, MPG, KIT, HZB, GSI, DESY Zeuthen
ES	ESS Bilbao*
FR	ITER, Saclay*
IN	TIFR
JP	KEK, SPring-8
KR	PAL
RU	ITER
SE	ESS, Lund University
US	SLAC, NSCL/FRIB, ANL

expected to join shortly: TR TARLA, US ORNL

* new in 2016

Questions/Discussion

Backup: DDC Block of AD9691