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How to build your own 3 GHz Signal Analyzer and achieve -155dBm/Hz noise floor

A virtual dive into the signal chain, challenges, pitfalls and solutions

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TECHNICAL SUPPORT MANAGER NORTH GERMANY

5th microTCA Workshop, 8th December 2016

Signal Analyzer - Agenda

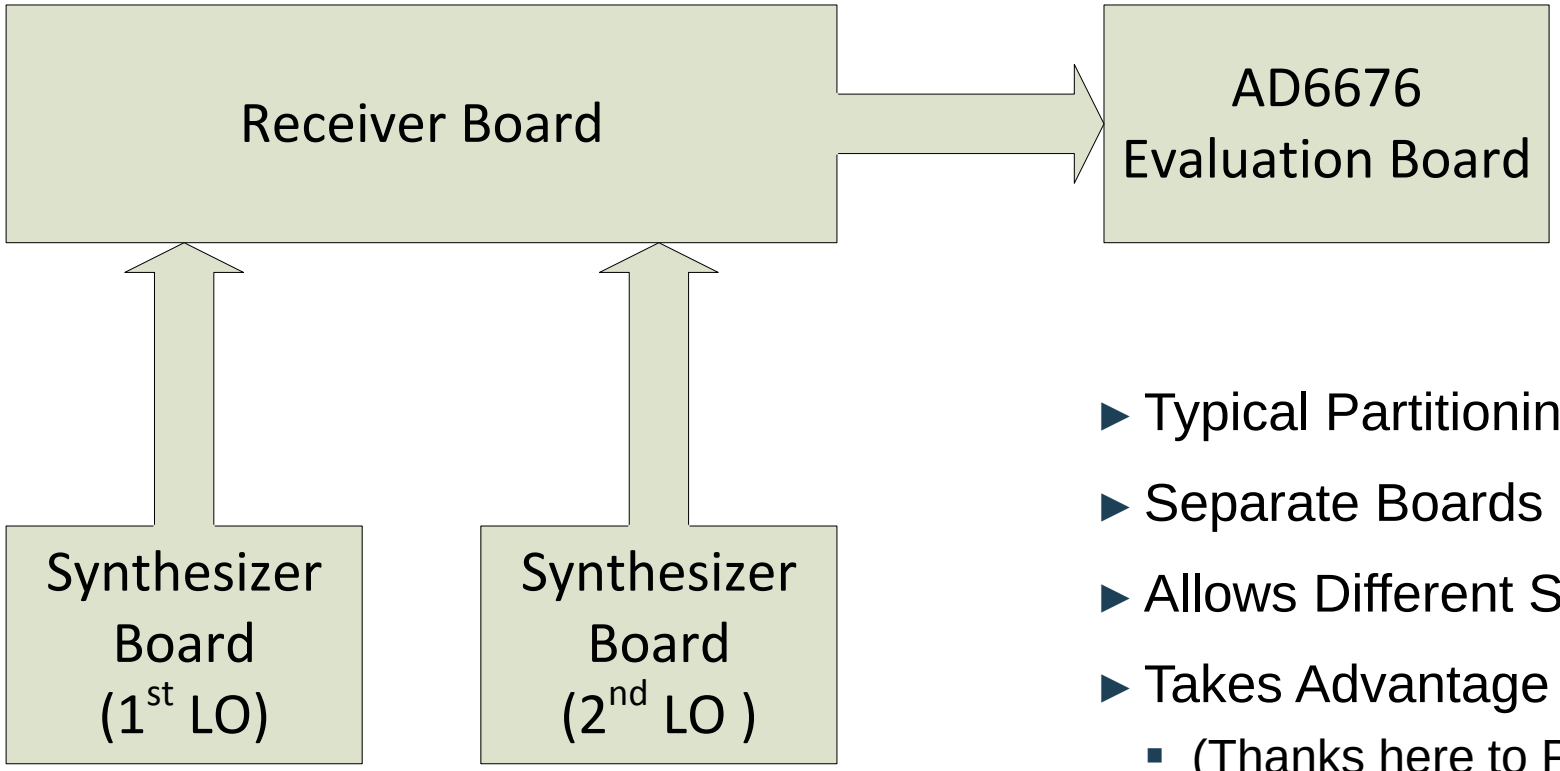
- Signal Analyzer
  - Comparing Signal Analyzer vs. Spectrum Analyzer
  - Design partitioning
- Details of Receive Board
  - Signal Chain
  - Component Selection
- Phase combined ADF4355 PLLs with integrated SiGe-VCO for low noise LO
  - The idea
  - Tools to solve the challenges
- Digitizing the last IF: AD6676 IF digitizing ADC – Subsystem
  - Evalboards and Software Implementation

Signal Analyzer vs. Spectrum Analyzer

- Signal Analyzer
  - Uses ADC
    - To measure any signal
    - Can display constellation (I/Q) of demodulated data
  - Mix of Analog and Digital Filters
  - ADC dynamic range limits measurement dynamic range
  - Fast sweeps
    - Tunes 10-500 MHz at a time
      - Function of ADC BW and digital filters
      - FPGA intensive
    - Thus fewer frequency steps

- Spectrum Analyzer
  - Uses Log Amp
    - To measure CW (ideally) signal
    - Can demodulate FM
  - Analog Filters
  - Log amp limits measurement range to about 80 dB
  - Slow sweeps
    - Tunes Hz or kHz at a time
    - Thus more frequency steps

Signal Analyzer Design Partitioning



- Typical Partitioning in Industry
- Separate Boards “Easy” to Debug
- Allows Different Synthesizers and ADCs
- Takes Advantage of AD6676 Software
  - (Thanks here to Paul Hendriks!)

Low phase noise synthesizer design uses
4 parallel ADF4355 PLL/VCOs and a Novel Phase Combiner for 6 dB improvement in Phase Noise

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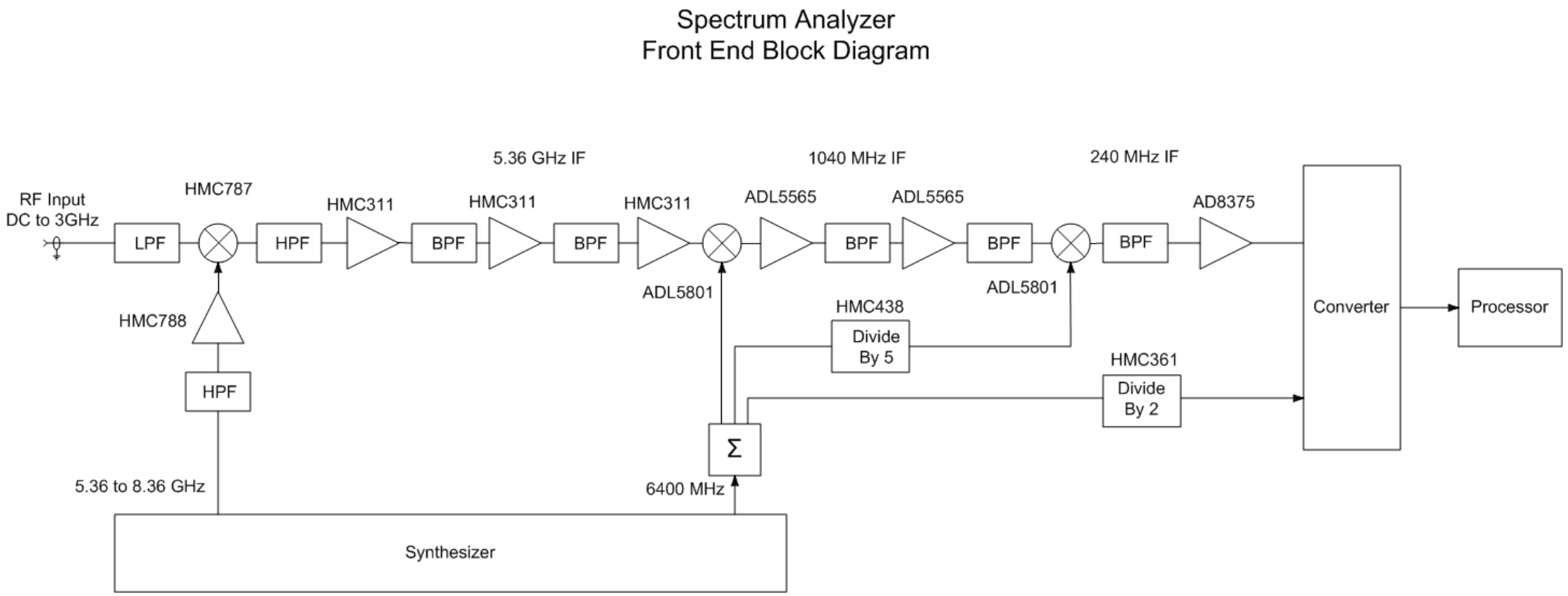
Details of Receive Board Design

Receiver Functional Block Diagram



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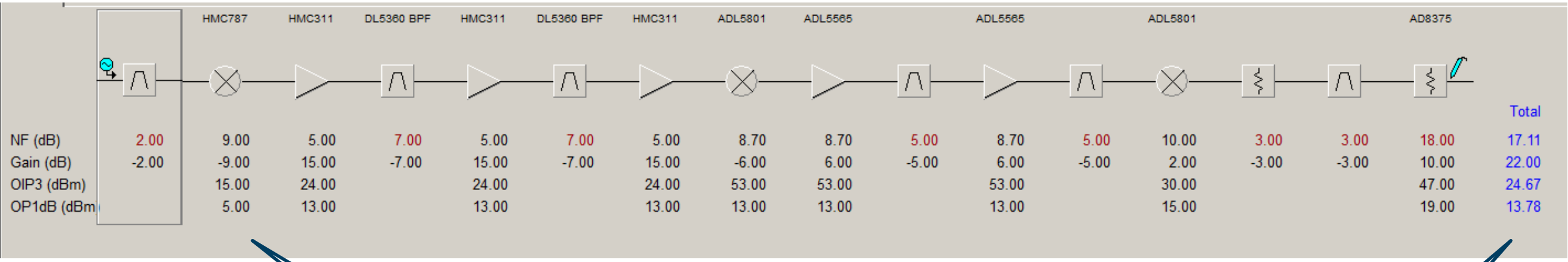
Cascaded Noise Figure and Intercept Analysis (ADIsimRF)

Part Numbers



																Total
NF (dB)	2.00	9.00	5.00	7.00	5.00	7.00	5.00	8.70	8.70	5.00	8.70	5.00	10.00	3.00	3.00	18.00	17.11
Gain (dB)	-2.00	-9.00	15.00	-7.00	15.00	-7.00	15.00	-6.00	6.00	-5.00	6.00	-5.00	2.00	-3.00	-3.00	10.00	22.00
OIP3 (dBm)		15.00	24.00		24.00		24.00	53.00	53.00		53.00		30.00			47.00	24.67
OP1dB (dBm)		5.00	13.00		13.00		13.00	13.00	13.00		13.00		15.00			19.00	13.78

User Entries Per Part

Cascade Results

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Component Selection

- Needed a LF-3+ GHz upconverting passive mixer
  - Passive to maximize IP3 and minimize noise
  - Best choice available was HMC787 wideband mixer connected backwards (input to IF, output from RF)
    - Plus HMC788 LO driver amplifier
  - OIP3= 15 dB, would prefer 10-15 dB higher
  - Also measured ADL5801 (+30 dBm IP3) but its performance rolled off too much as upconverter
  - Note: Mixers designed for signal analyzers are very high performance… stay tuned to this space!

- Used ADF4355 for 1st pass at synthesizer design
  - Sacrificed frequency range to maximize 1st pass success
  - ADF5356 (re-spin of ADF5355 PLL/VCO) coming soon – pin compatible part with higher frequency range
  - ADF41513 and new VCOs also coming soon – can swap in evaluation board for synthesizer

IF Component Choices

- ADL5801 for the second and third mixer stage
  - Fully differential output simplifies IF path and filtering – fewer worries about where RF ground is
  - Very high IP3 <5 GHz as downconverter.
    - **“Can use in both sockets” – or so we thought!**
    - **will replace as third mixer, due to high order spurs, with future differential-output passive mixer**
  - Input frequency (1st IF) a bit high so it will be a bit noisy (i.e., a higher noise figure but it’s at IF so not as critical)

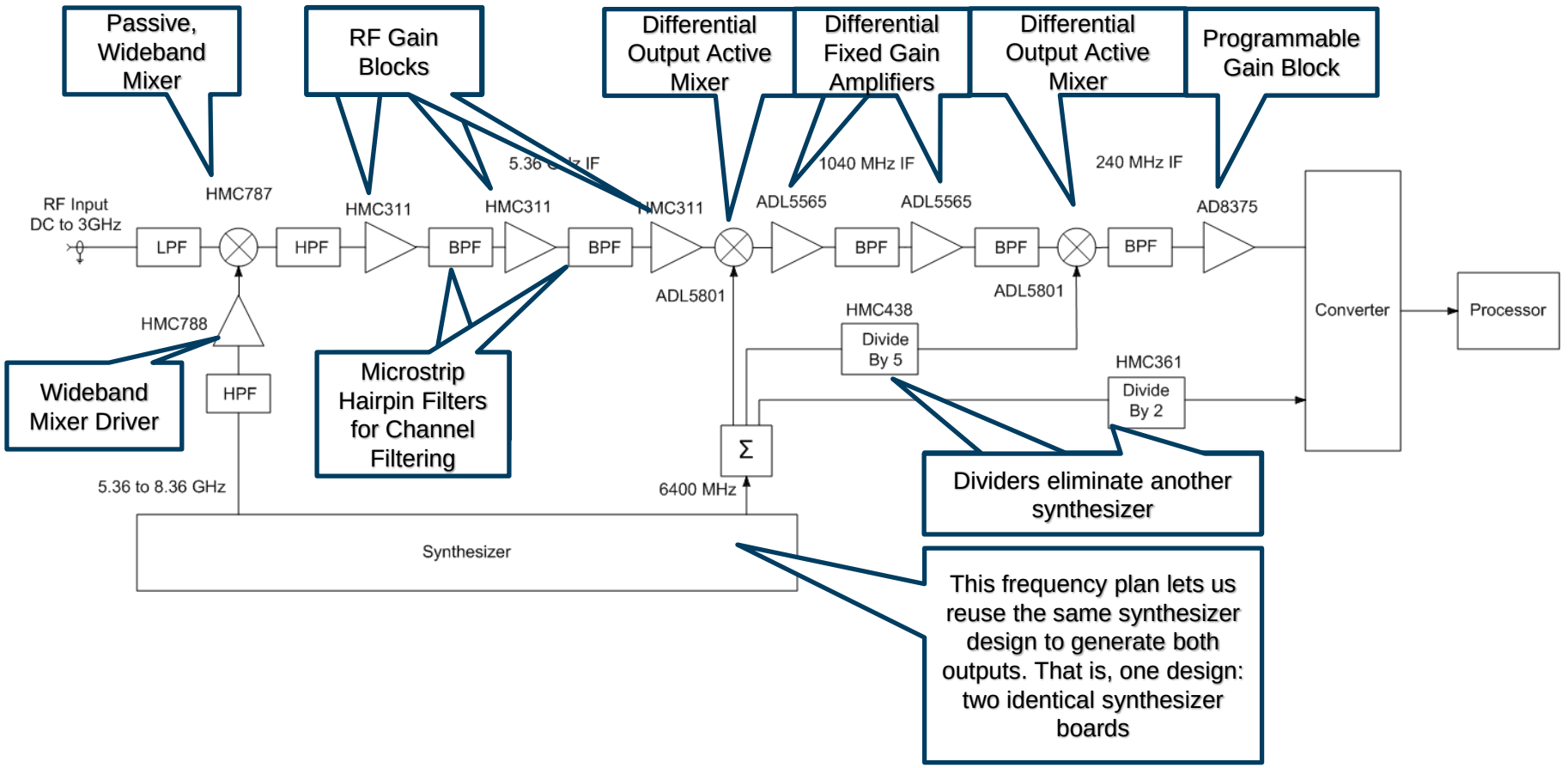
  - 0 dBm LO drive – no separate driver amplifier necessary
  - But can be noisy
  - Will replace third mixer with passive mixer as soon as one becomes available with differential output

- ADL5565 ADC driver as an IF amplifier
  - Fixed gain
  - Differential Input and Output
  - Very Low Distortion

Why HMC311? Why dividers? Why AD8375?

- The HMC311 gain blocks compensate for the insertion loss of the cascaded filters
- The dividers derive the third LO and ADC clock from the second synthesizer – eliminates the need for more synthesizers and a separate clock generator
- The ADL8375 VGA is used to set the signal level going into the ADC board
  - Programmed by DIP switches

Summary of receiver board component selection



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Phase Combined ADF4355 PLLs for Low Noise LO

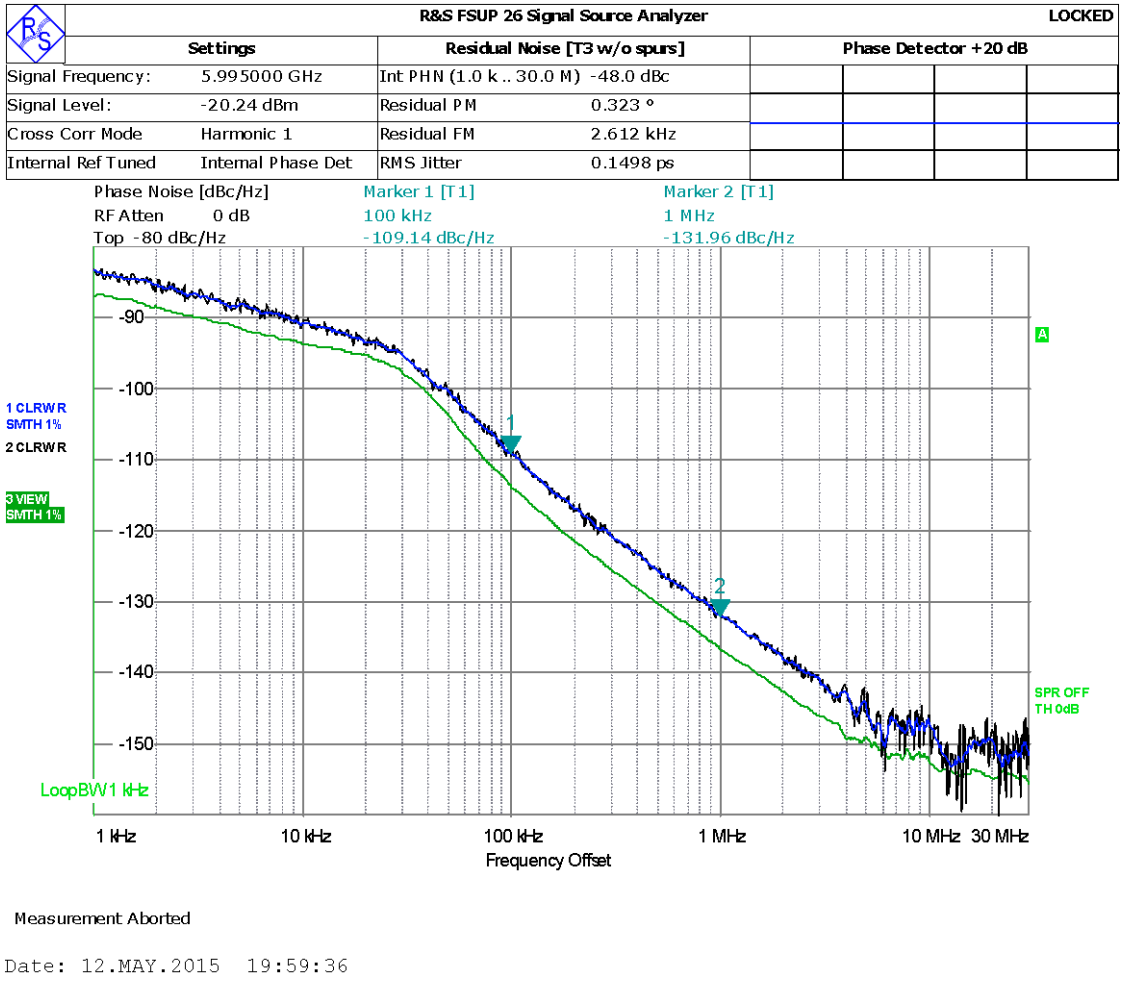
CAN USE THE SAME LO TWICE AS

LO FREQUENCIES FALL INTO THE SAME FREQUENCY BAND

LO1 = 5.36 … 8.36GHZ

LO2 = 6.4GHZ

Combining Four PLLs in Phase – Benefits and Challenges



▶Benefits

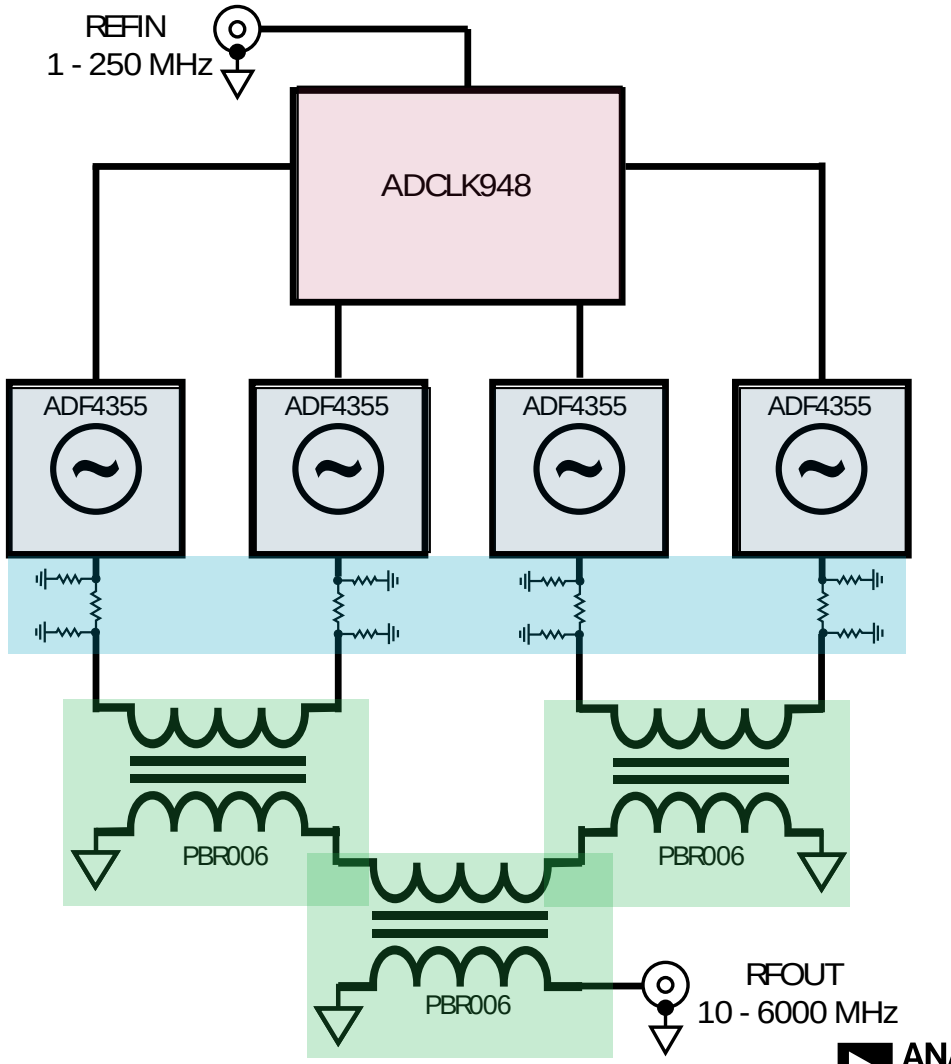
- 6 dB improvement over datasheet specifications at 1 MHz offset.
- Allows SiGe oscillators to approach YIG Oscillator performance.
- YIG Oscillators are expensive, power hungry, and unreliable.

▶Challenges

- REFIN distribution
- Isolation of each PLL
- Combination of output signals

Simplified Schematic

- ADCLK948 clock buffer used to provide reference to 4 x ADF4355 parts.
- Software Phase Adjust Feature used to align output waveforms for phase coherency.
- High isolation combiners used to give 6 dB lower phase noise.
- Optional resistive attenuation pads at RF output to improve isolation if necessary.



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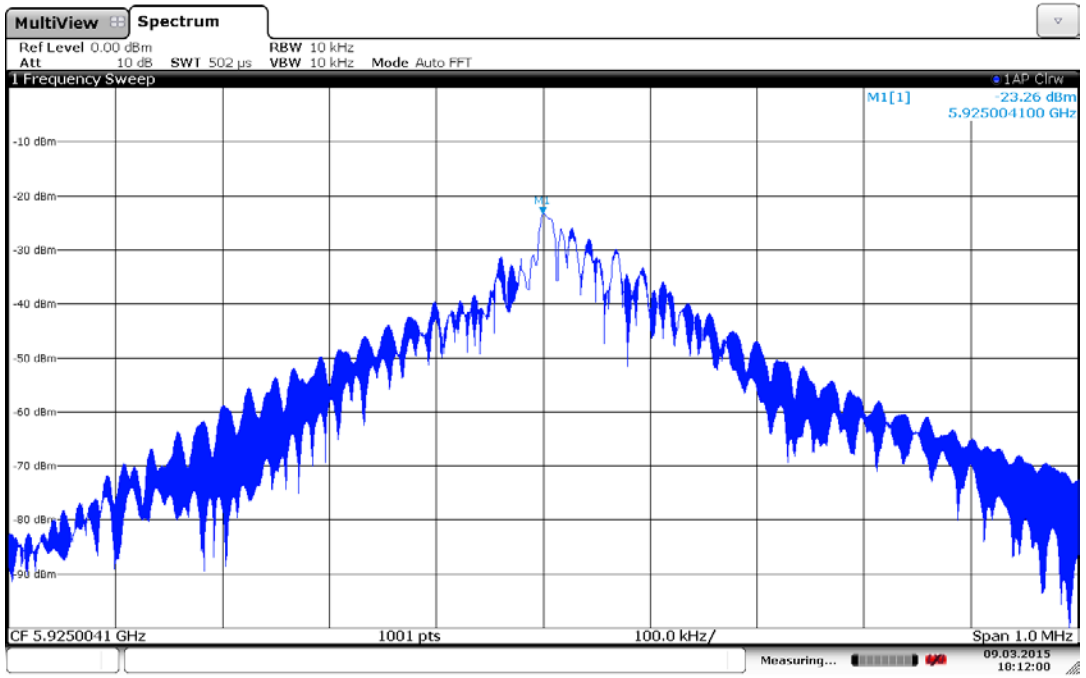
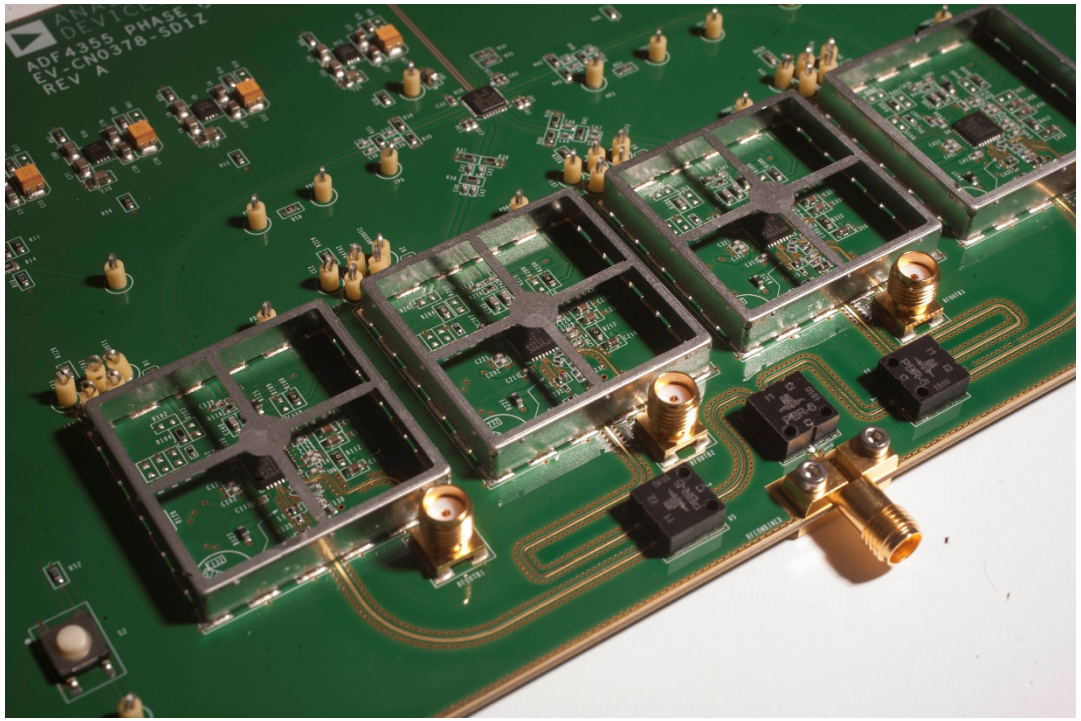
With Multiple PLLs On One Board, What Could Possibly Go wrong?

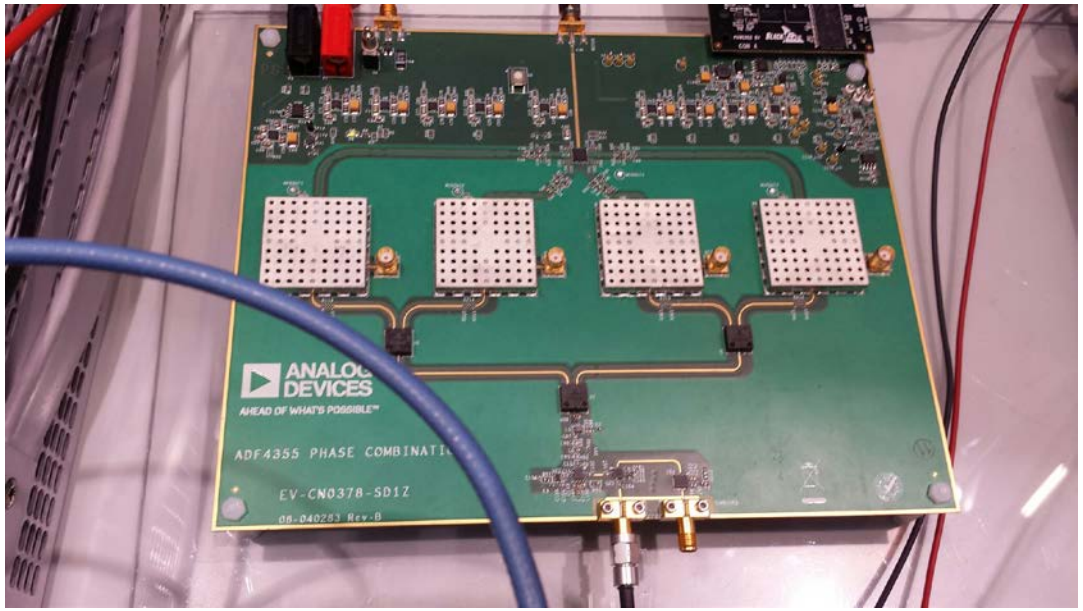


- INJECTION LOCKING!
  - Phenomenon where tones from one synthesizer couple to a nearby synthesizer, and interfere with the normal locking process. The competing lock mechanisms cause modulation and lead to degraded phase noise and spurs.
  - Defeats purpose of circuit!

Cure: Isolation.



- Shielding reduces far field effects.
- Provides 40 – 50 dB of isolation.
- Improved Board Layout.



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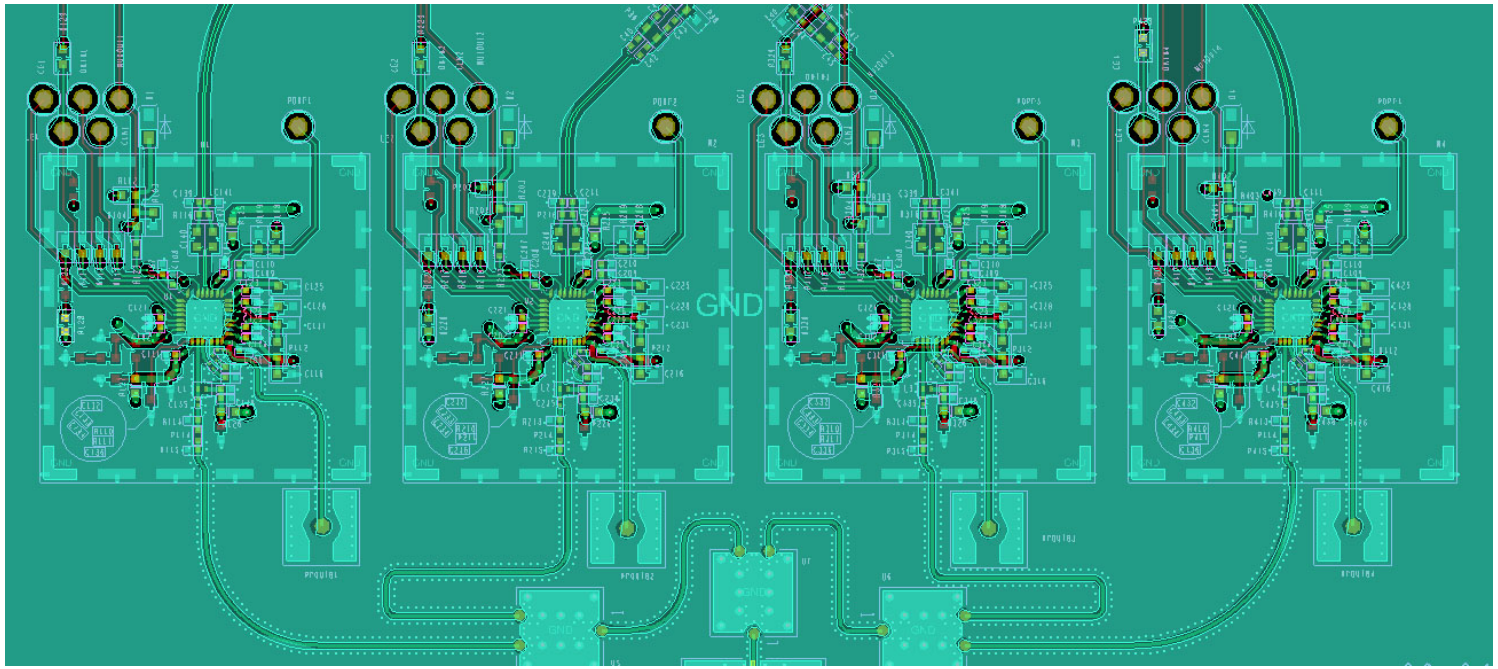
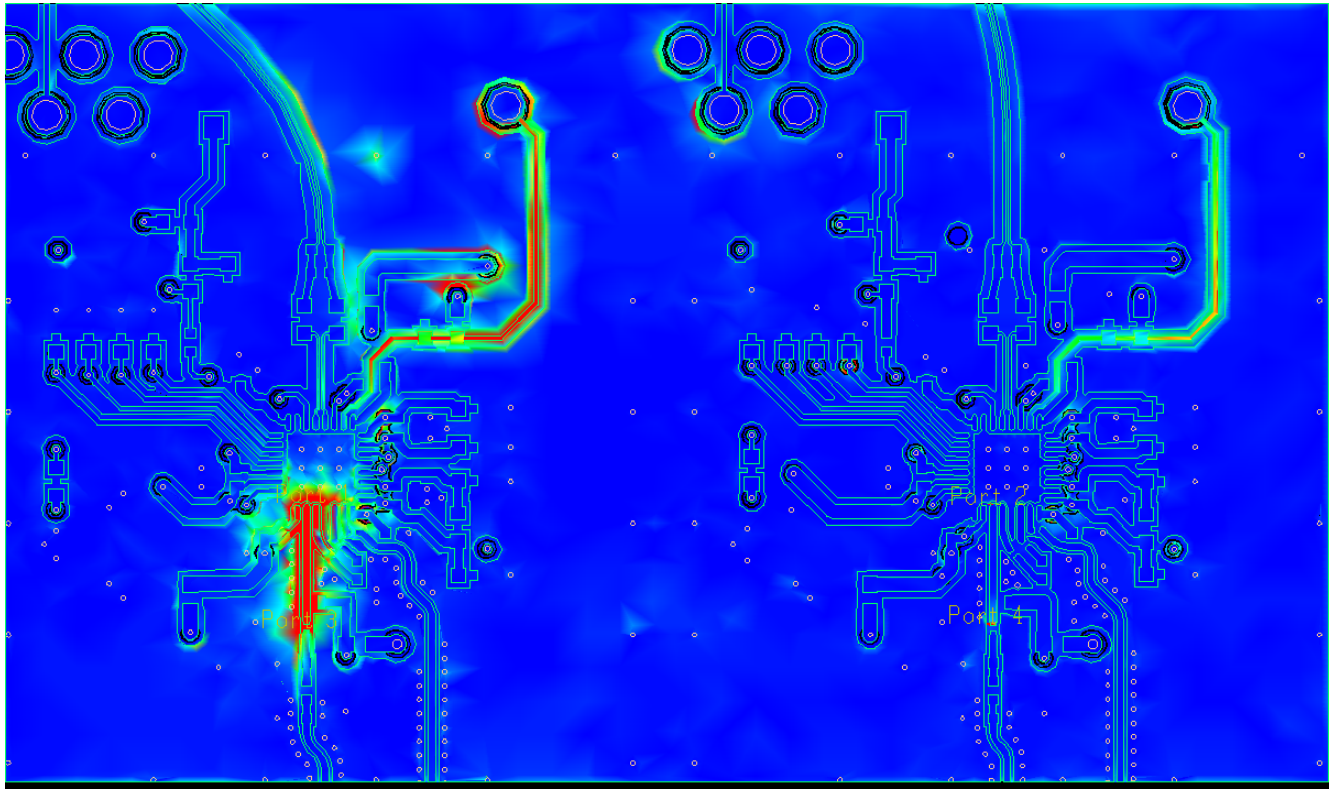
Layout Change: Import to Keysight ADS



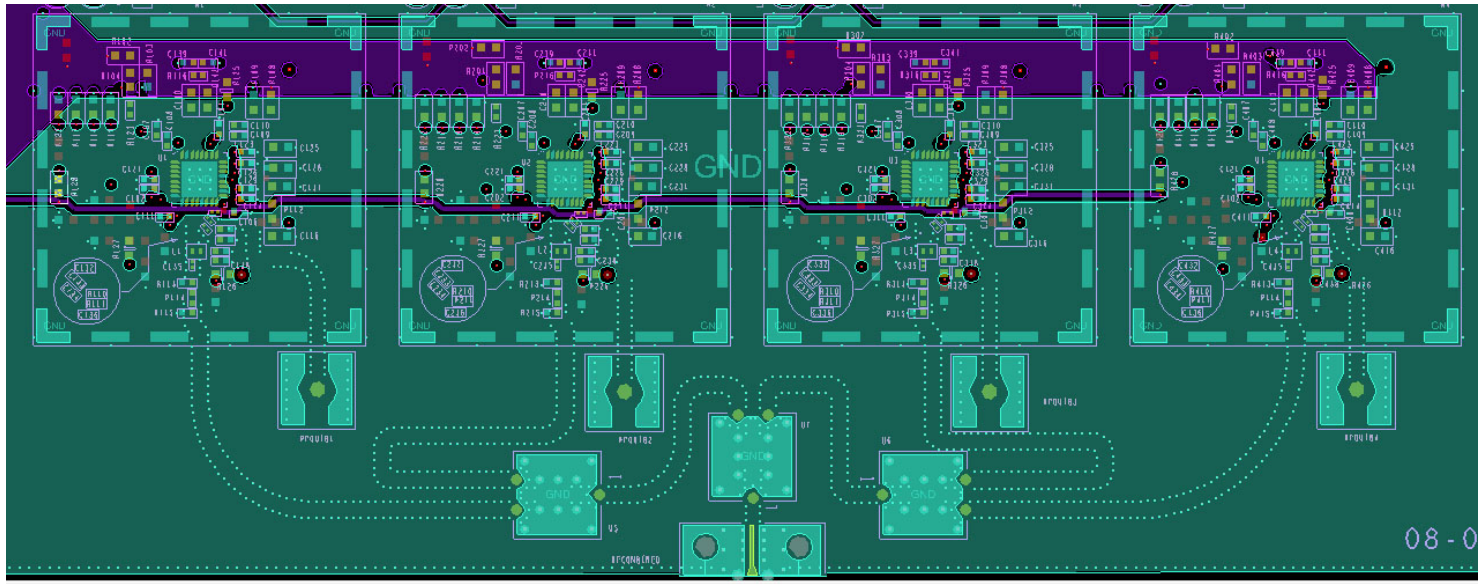
- Cadence Allegro permits export to .adfi which is easily imported to Keysight ADS software for 2.5D simulation.
- Highlights layout weakness, reduces board iterations.

3D Visualization



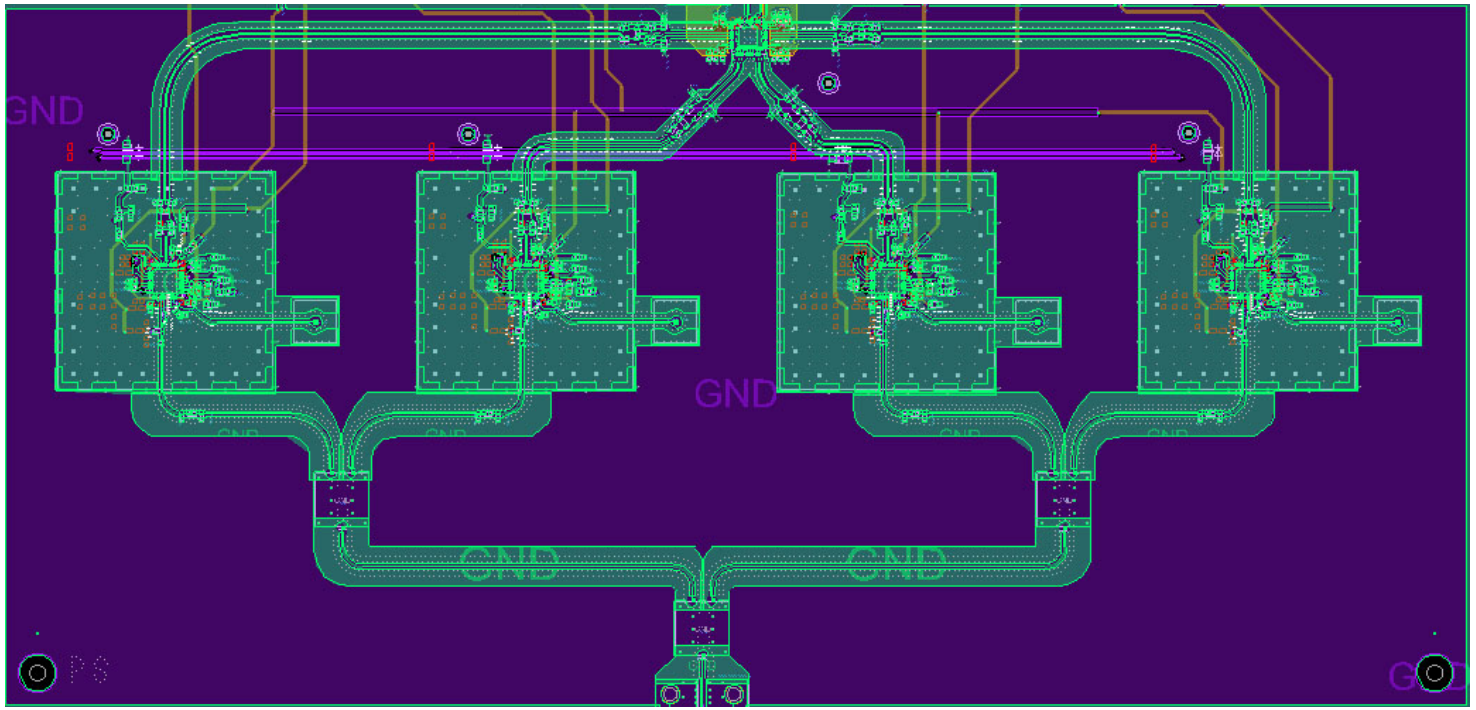
- Long interface lines acting as antennae.
  - Solution: Shorten or where possible, remove.
- More vias to GND required.
- Increase physical distance between synthesizers.

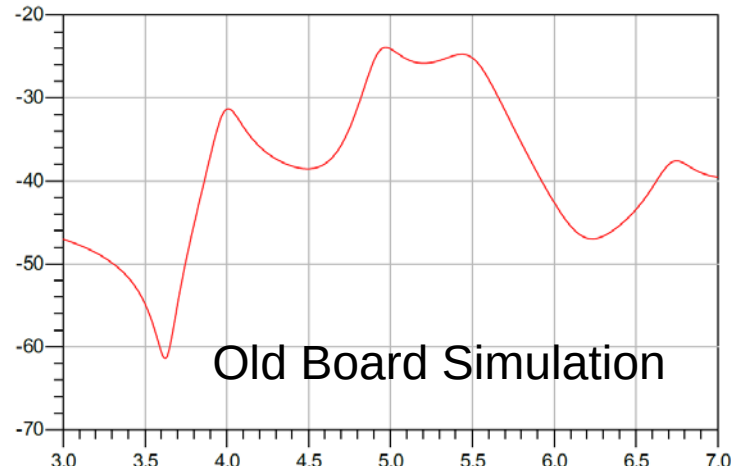
Changes in next layout

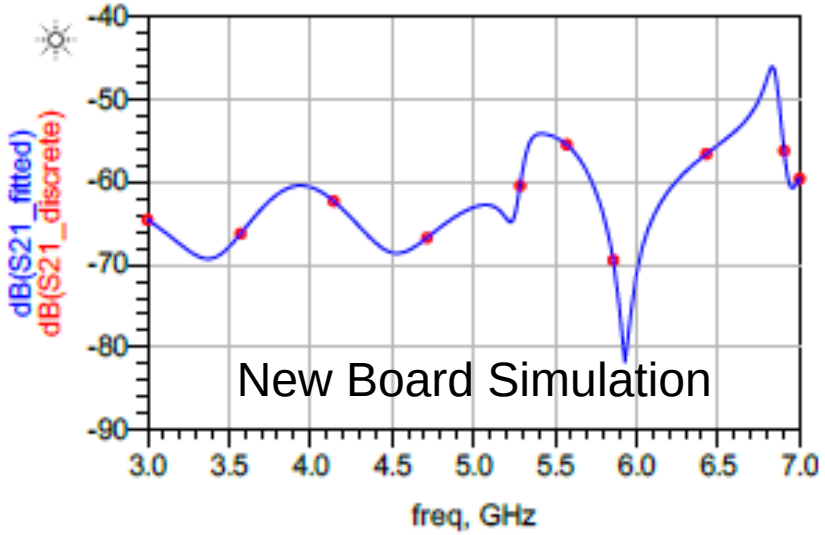


- Reroute CE line (purple line above). This degrades isolation, by coupling RF out to each synth on board layer 3.
  - (Proven by measuring coupling from synth 4 to synth 3 and comparing it to synth 3 to synth 2.
  - Less coupling from S43 to S32.
- Reroute output stage such that RF outputs go ‘directly’ to couplers and not around corners, as above.

Next layout. Design Goal: Isolation.







- Shortened / Moved digital interface lines.
- Increased physical distance between synthesizers. (Used board area).
- New symmetrical routing of RF stage.
- Additional GND vias.
- Equal length lines ensure all synthesizers are at same phase, which helps minimises inj locking.
- Calibration circuit placed at output.
- 20-30dB improvement in isolation – solved injection locking issues!

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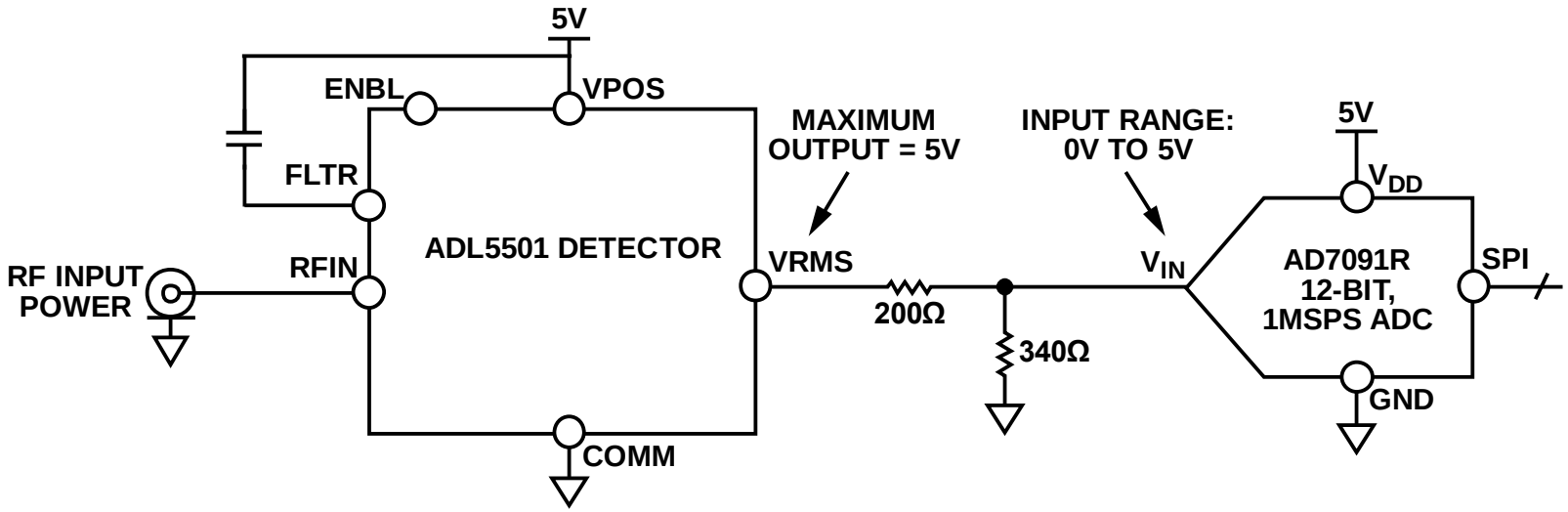
Calibration Circuit. Power Detector Choice.



- Use directional coupler plus rms detector to measure power levels.
- ADL5501 produces output which is more accurate at high power levels than at lower power levels.
  - Maximum power level is when four waveforms are in-phase.
    - Rotate ADF4355 phase, check power, keep rotating until maximum power has been achieved.
  - Fine tuning phase is more important as maximum power approaches, whereas lower power levels don't need much accuracy. Hence Linear V/V detector in preference to log Amp.
  - Software will be used to rotate phase until power has been maximized.
  - Will also require a directional coupler/switch and amplifier to sniff off power from main circuit.
  - Proven in lab. Will be incorporated into hardware/software for Signal Analyser.

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Digitizing The Last IF: AD6676 EVB and Software

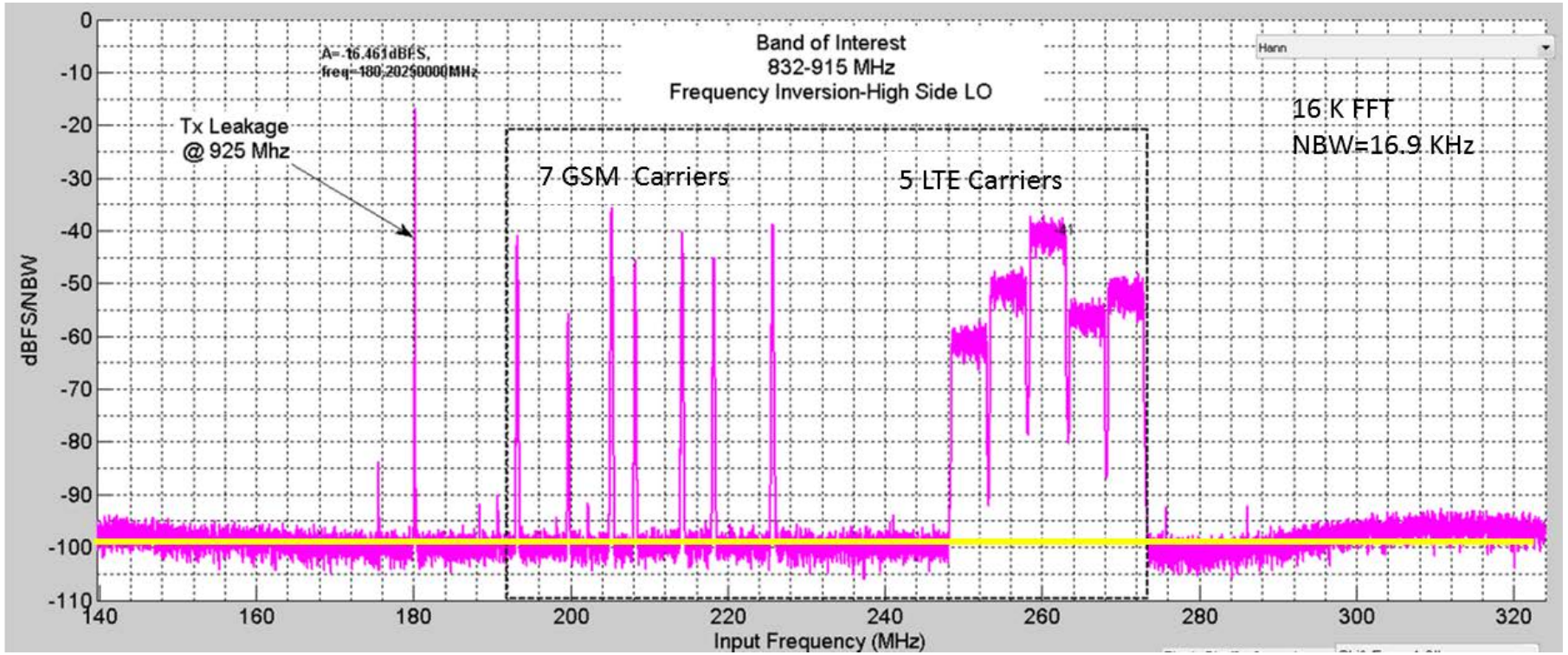
SIGNAL ANALYZER ON A CHIP!

(STRICTLY SPEAKING THIS IS A QUADRUPLE CONVERSION RECEIVER AND THE LAST DOWNCONVERSION IS DONE IN THE AD6676!)

SLIDES BY PAUL HENDRIKS

AD6676 Wideband IF Receiver Subsystem

Enables true Multi band/Multi mode Software Defined receivers



- The large dynamic range of the AD6676 significantly eases Multiband Communication System and *Signal Analyzer* designs

http://www.analog.com/AD6676

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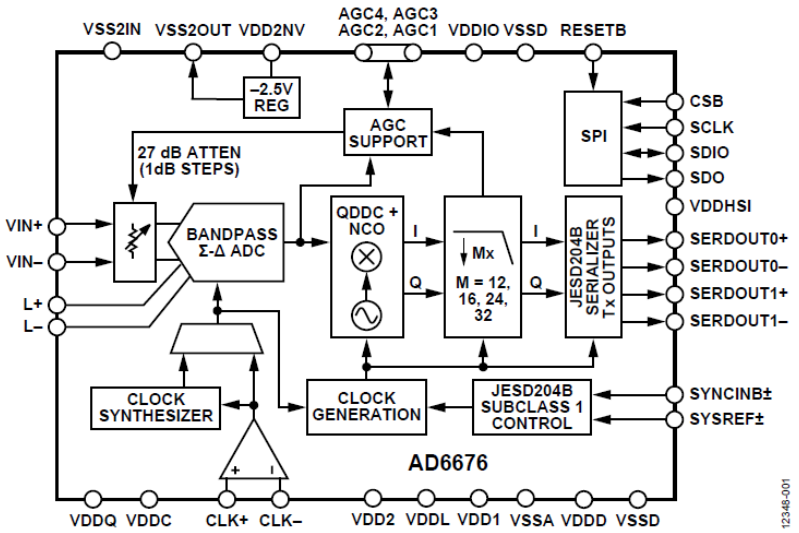
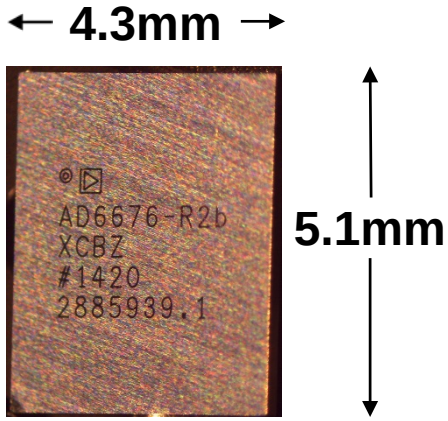
AD6676 Wideband IF Receiver Subsystem

- Industry leading Dynamic Range
  - NSD of -159dBFS/Hz, IMD3 of -96dBc
  - IIP3 up to +36dBm, NF of 13dB
  - Swept Spurious < -99 dBFS
  - Nominal PIN_0dBFS = -2 dBm
    - Adjustable over +13 to -14 dBm range
    - Easy to drive ZIN of 60 ohms



- Based on “Reconfigurable” oversampled BP ΣΔ ADC technology
  - Continuous-Time ΣΔ ADC
  - Eliminates SAW filter, DGA and IF Gain
    - PCB area savings up to 70%
    - “Simple” RF-to-IF mixer interface with LPF
  - Very wide tunable IF/BW Rx platform
    - Same mixer-to-bits line-up can support 0.7-3.8 GHz



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AD6676 Wideband IF Receiver Subsystem

- Enables “Reconfigurable” Wideband IF Rx Subsystem
  - Support Direct Sampling VHF or Heterodyne UHF Receivers
    - IF Frequency tunable from 70-450 MHz
    - Usable Passband BW tunable from 20-160 MHz
  - “Profile Feature” allows up to 4 different IF/BW combinations that can be switched within 1 µs.

- High Level of Integration/Functionality
  - IF Digital Attenuator with AGC Support (Detection/Gain Control)
  - High Dynamic Range SDADC
  - On-chip DSP includes QDDC and Decimation filters
  - I/Q 16-bit data via 1 or 2 lane JESD204B interface
  - Optional Clock Synthesizer (2.94-3.2 GHz operation)

- Power Consumption of 1.2 W (w/ 1.1 V and 2.5 V supplies
  - Mixer-to-bits Rx chain of < 2 W (w/ mixer+PLL/VCO)

AD6676 Evaluation software platform

- MATLAB based user-intuitive graphical interface
- Ability to sweep various receiver parameters to test the performance of the AD6676 receiver in user applications
- Allows users to easily configure the receiver in various modes

http://wiki.analog.com/resources/eval/ad6676-wideband_rx_subsystem_ad6676ebz

http://www.analog.com/AD6676

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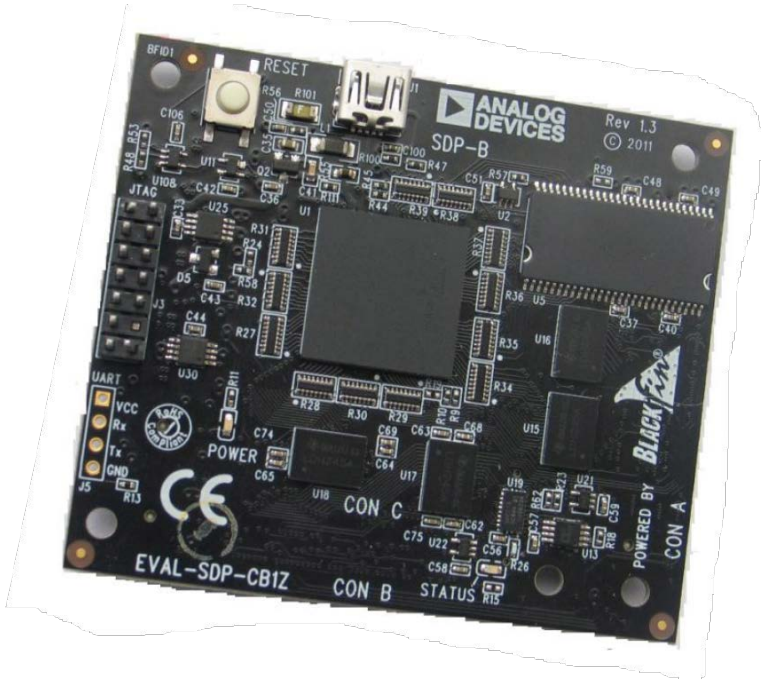
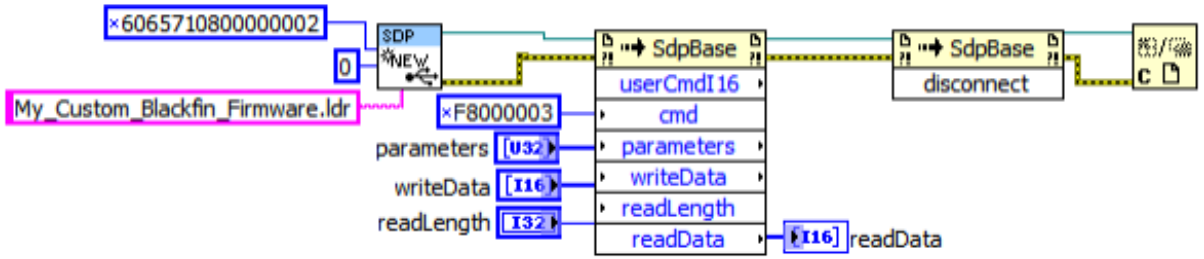
Accelerating SDP Application Performance with Custom Blackfin Functions: Offer SDP Software for Synthesizer, RF Down-Conversion, and ADC

- Problem: Each USB transaction on the SDP platform can take at least 1mS and is **not** deterministic
  - This can be an issue for applications that need to access peripherals frequently or have stringent timing requirements
- Our application has a calibration algorithm that requires many cycles of peripheral read and writes with calculations performed in between each cycle
  - If calculations are performed on the PC side, thousands of cycles add up to a very perceptible lag to the user
  - We do not want this lag to be accidentally equated with the performance of the ADI solution being demonstrated!
- Solution: Perform the critical tasks on the SDP hardware
  - Custom DSP functions can be written and called from SDP API, either in LabVIEW or .NET
  - In the SDP-B Blackfin source code, hooks already exist to add this functionality
  - In our case, performing the peripheral read and write combined with calculations on the DSP will eliminate the overheard of thousands of cycles of USB transactions





Calling user function from SDP API in LabVIEW

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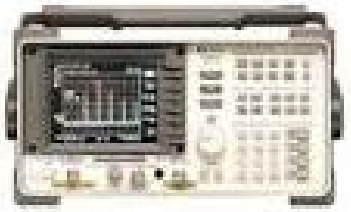
Signal Analyzer from ADI compared to some Low to Mid Performance Commercial Spectrum Analyzers

Model	Maximum Frequency	Noise Floor, preamp off	IIP3 @ 1GHz	Price
Keysight N9913A	4 GHz	-139 dBm/Hz	15 dBm?	$10,795
Keysight N9340B	3 GHz	-139 dBm/Hz	10 dBm	$8,599
Keysight E4402B	3 GHz	-150 dBm/Hz	16 dBm	$24,948
R&S FSH3	3 GHz	-144 dBm/Hz	13 dBm	??
Anritsu MS2711E	3 GHz	-141 dBm/Hz	20 dBm	$6,950
Advantest U3741	3 GHz	-145 dBm/Hz	10 dBm ?	$7,980
HP8591A	1.8 GHz	-145 dBm/Hz	+5 dBm	$2,497 used
ADI	**4 GHz**	**Measured!** -155 dBm/Hz	-5 dBm 2nd mixer limited	**Much Less!**

(Thanks to Benjamin Sam for compiling commercial data!)







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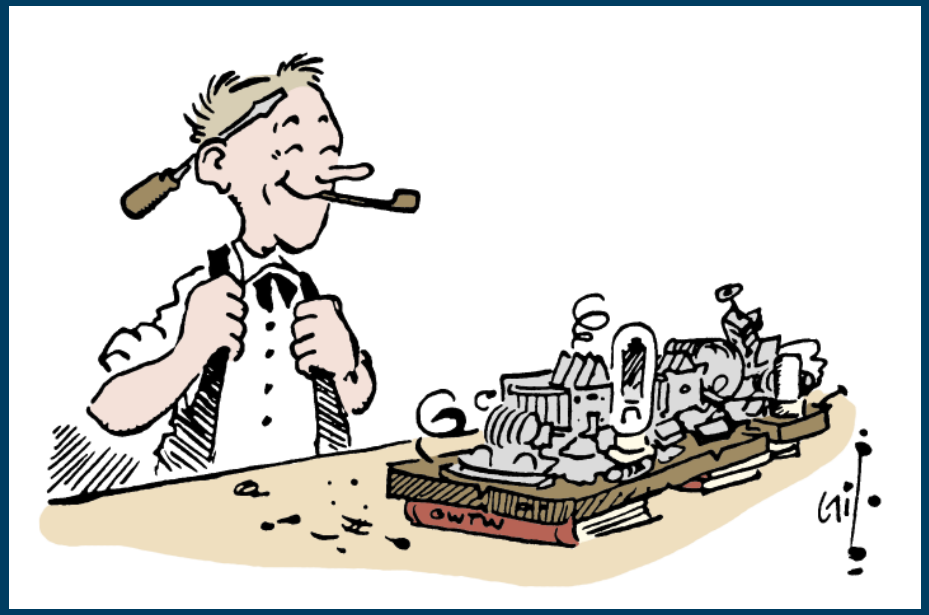
Where Do We Go From Here?



Next Steps

- Optimize synthesizer board
  - Substitute with **ADF5356** PLL/VCO
  - Explore active combiner for wider bandwidth and lower cost
- Debug final receiver board and integrate system
- Explore external LNA with bypass switch to decrease noise floor to better showcase **AD6676**'s dynamic range
- Use as material for trade show demo, article, CftLs, Circuit Notes @ www.analog.com
- ----------<

My acknowledgements go to the great engineers in the ADI Labs, who contributed to this challenging Signal Analyzer design with their knowledge and efforts and still improve it!