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High Bandwidth Data Acquisition (HBDQ) MTCA.4.1 Platform

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This presentation shows how the latest technology enhancements, new upcoming sub-standard MTCA.4.1 and more backplane interconnection create a new performance level of data acquisition.

NATIVE-R2 HBDQ platform doubles the bandwidth to each IO-Card and CPU card in its 6 AMC slots and quadruples the bandwidth to the aggregation processing nodes inside and outside the chassis.

The NATIVE-R2-HBDQ combines a 2U MTCA.4.1 chassis offering 8 PCIexpress lanes to each AMC slot with the NAT-MCH-PHYS80 offering 80 PCIexpress lanes, where two times 16 PCIexpress lanes (128 Gb/s) are routed to high performance aggregation and processing CPU inside and/or outside the chassis. It comes with the infrastructure for Timing Synchronisation solution based on NAMC-psTimer (compatible to x2-Timer) and/or White-Rabbit Clock module.

NATIVE-R2 HBDQ comes with pre-installed Linux operating system and driver and application software for plugged in timing and synchronisation hardware and for high performance DAQ boards.

Cascading the NATIVE-R2 HBDQ solution provides in an 8U frame space for 24 AMC (each with a bandwidth of 64 GT/s) and 24 µRTM slots.

Summary

This on the upcoming MTCA.4.1 sub-standard based platform solves the following requirements and limitations of existing MTCA.4 system:

- enough PCIe bandwidth to aggregate data of latest high performance data acquisition FPGA based cards
- full usage of all 8 PCIexpress lanes of High Performance AMC-CPUs, which until now could only use half of their available lanes in current MTCA.4 crates
- support for high accurate synchronisation of distributed systems over long distances without the need of a separate AMC slot
- debugging of multiple AMCs with FPGA via JTAG during runtime at the same time without the need of multiple or even without any JTAG probe
- out-of-the-box start, as operating system, drivers and timing configuration pre-installed
- small foot print of 2U, 19 inch.

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