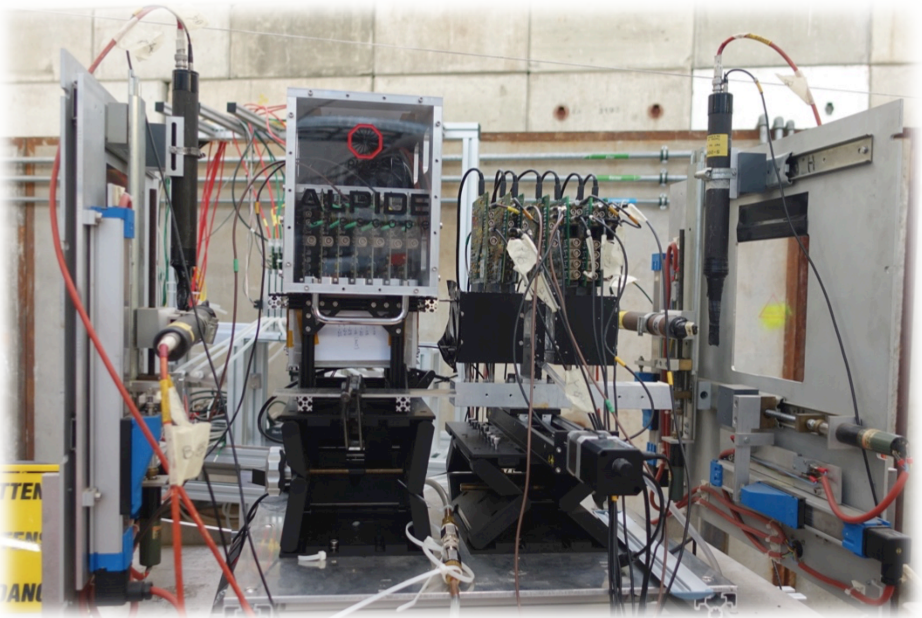
The ALPIDE telescope



J.W. van Hoorne - CERN

on behalf of the ALICE collaboration

Barcelona, January 26th, 2017

5th Beam Telescope and Test Beams Workshop 2017

Outline

1. Introduction
2. ALPIDE telescope
3. Selected results
4. Summary and future developments

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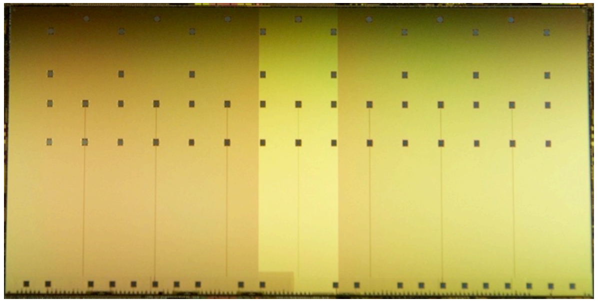
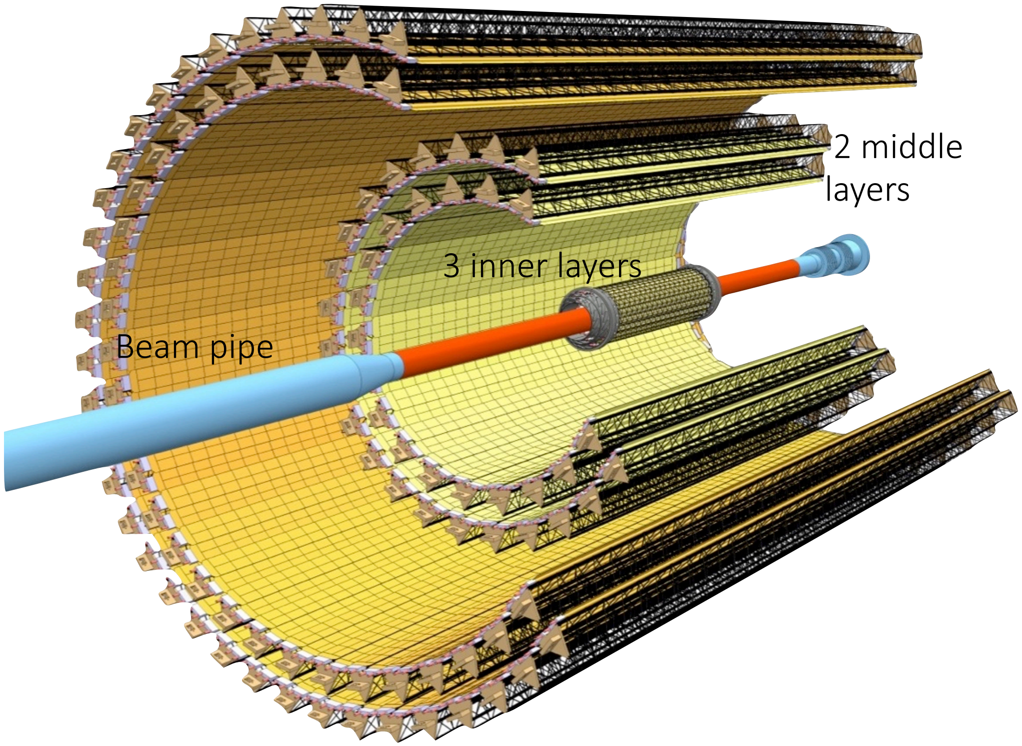
ALPIDE

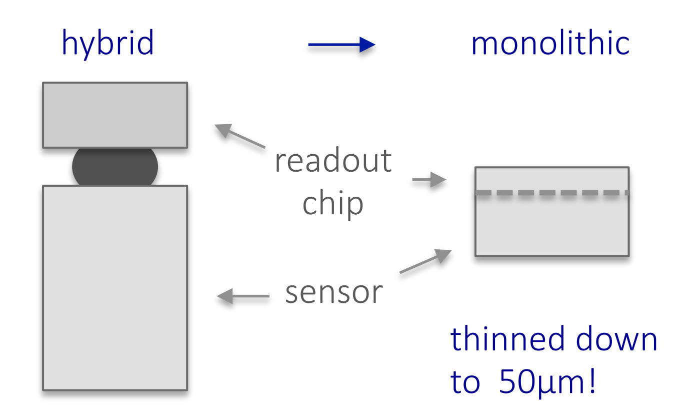


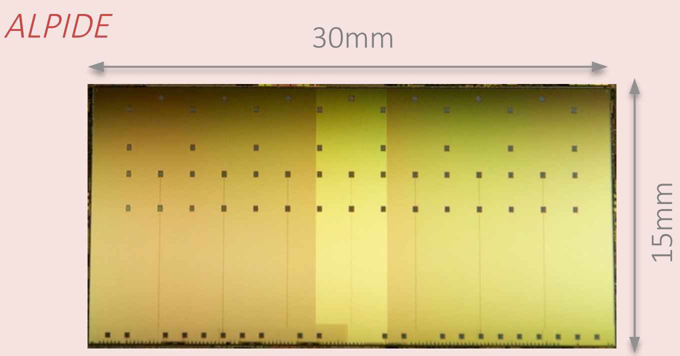


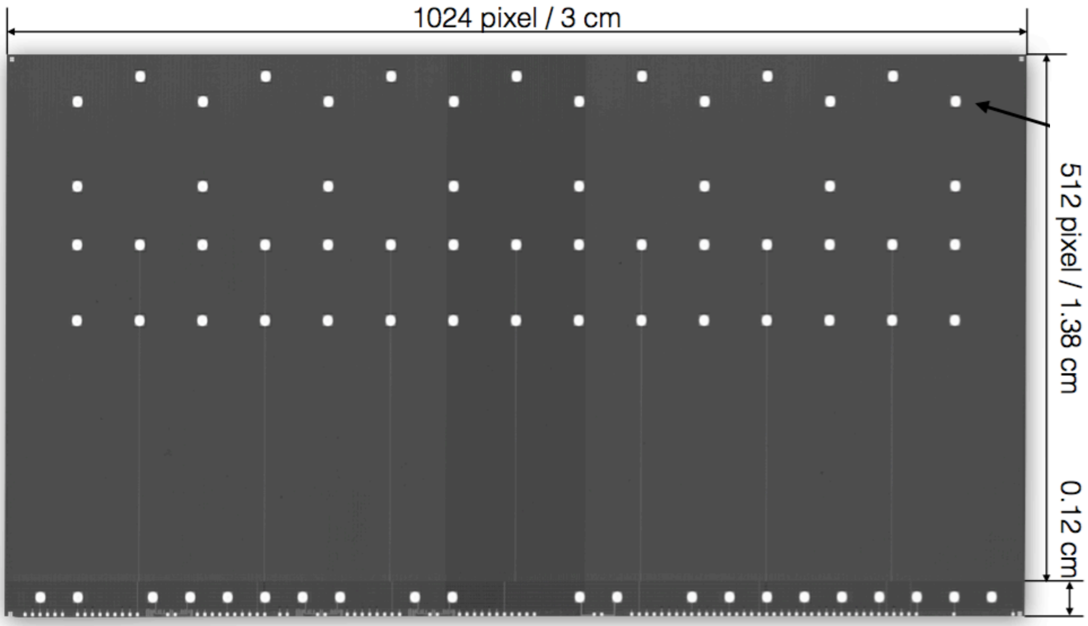
12.5 G-pixel camera:

- binary readout
- ~10 m^2 total area
- ~25000 chips

Fully equipped with Monolithic Active Pixel Sensors (MAPS)







- Produced in the TowerJazz 180nm CMOS Imaging Sensor (CIS) process
- 25µm epitaxial layer
- Full CMOS within pixel matrix

Key concepts:

- In-pixel amplification
- In-pixel hit discrimination
- In-pixel 3-level event memory
- In-matrix zero-suppression

Features:

- Dimension: 30mm x 15mm (1024 x 512 pixels)
- Pixel pitch: 29µm x 27µm
- Thinned to 50µm (0.05% x/X_0)
- Possibility to apply reverse bias voltage
- Event-time resolution 2-4 µs (charge collection time only 1-30ns, but not exploited)
- Very low power consumption (40mW/cm^2) no cooling needed in test beam setup
- Global shutter: triggered acquisition (up to 200kHz Pb-Pb or 1MHz pp <-> ~6MHz/cm^2 particle hit rate) or continuous (progr. integration time: 1µs – quasi ∞)
- Binary readout
- 1.2 Gbit/s serial link, can drive up to 5m of cable
- Two possible connection schemes: pads over the matrix and pads at the periphery

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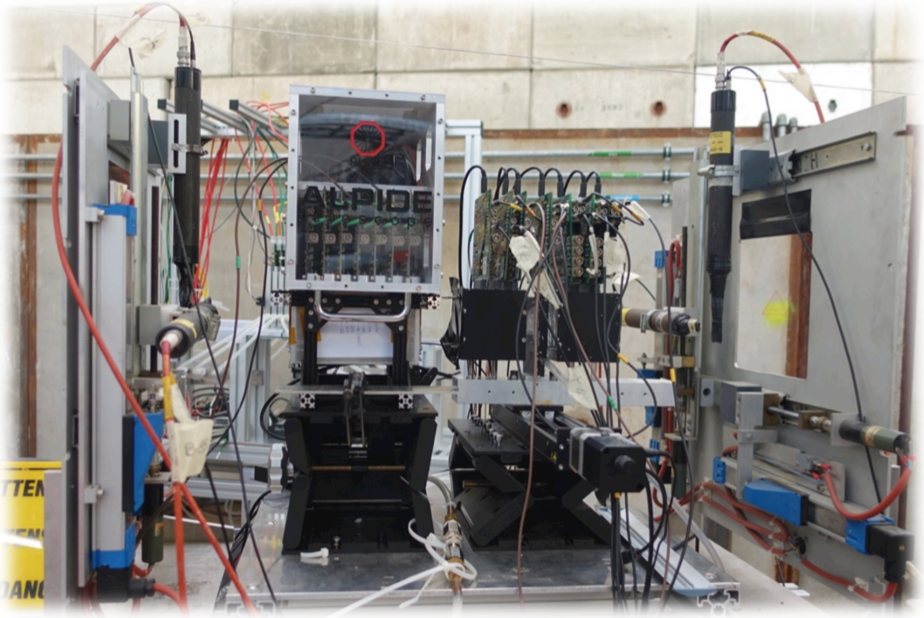
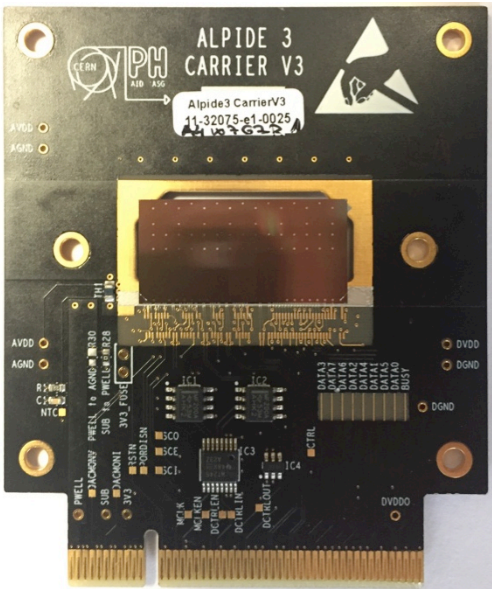
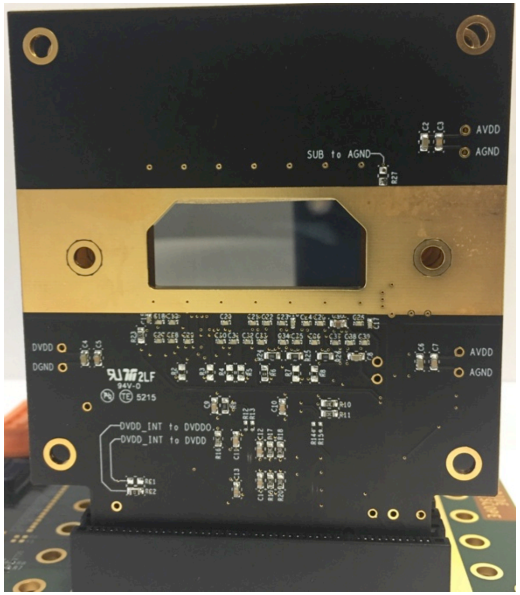


ALPIDE carrier card and DAQ board

2. ALPIDE telescope



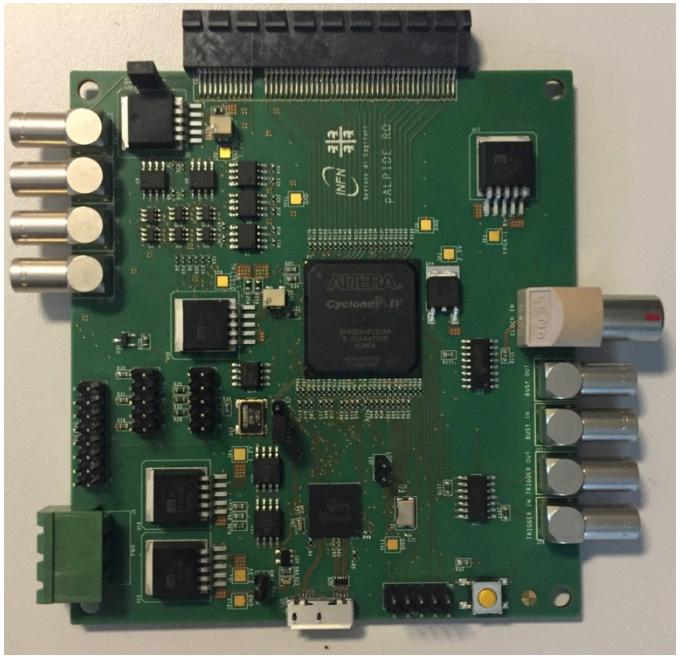


ALPIDE carrier card:

- Large opening underneath ALPIDE to reduce material budget
- PCIe connector used as mechanical and electrical interface (with custom electrical protocol)
- Small pads at periphery used for bonding

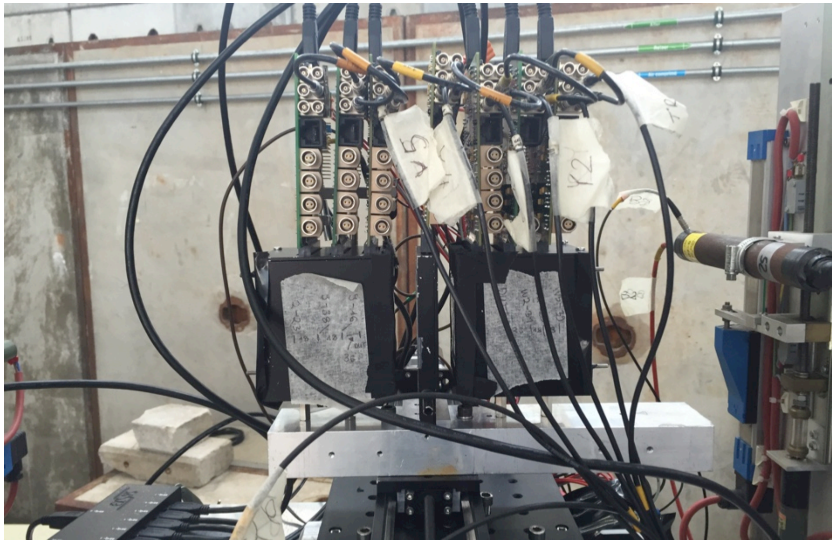
DAQ board:

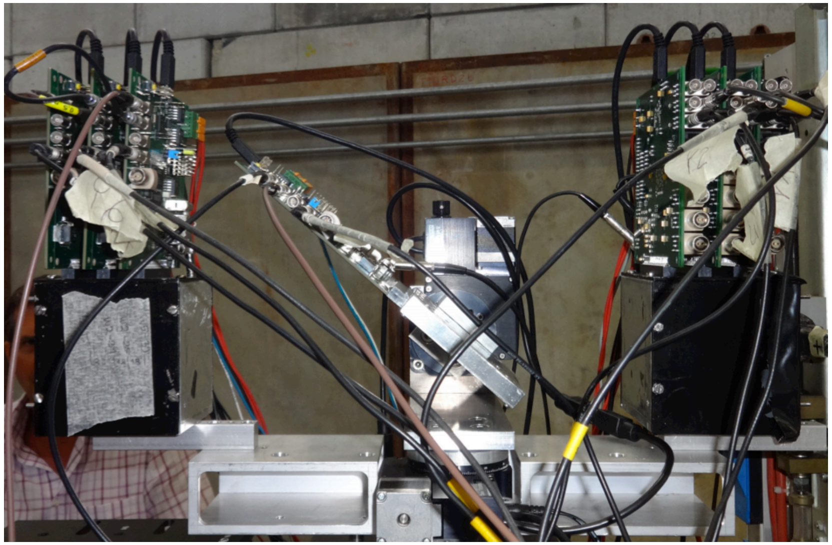
- USB-3.0 for connection to PC
- PCIe connector for carrier card
- Various GPIO connectors



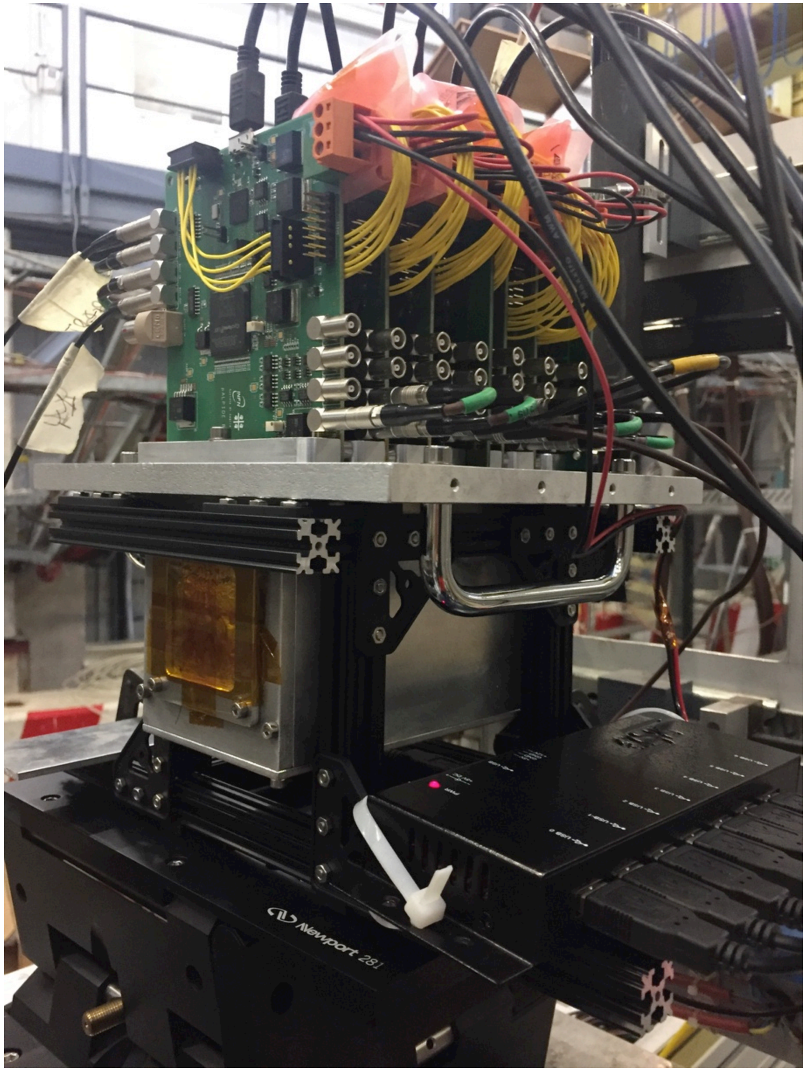
- ALPIDE telescopes typically consist of 7 planes, plane distance ~2cm
- Central chip is typically treated as Device Under Test (DUT)

Telescope 1



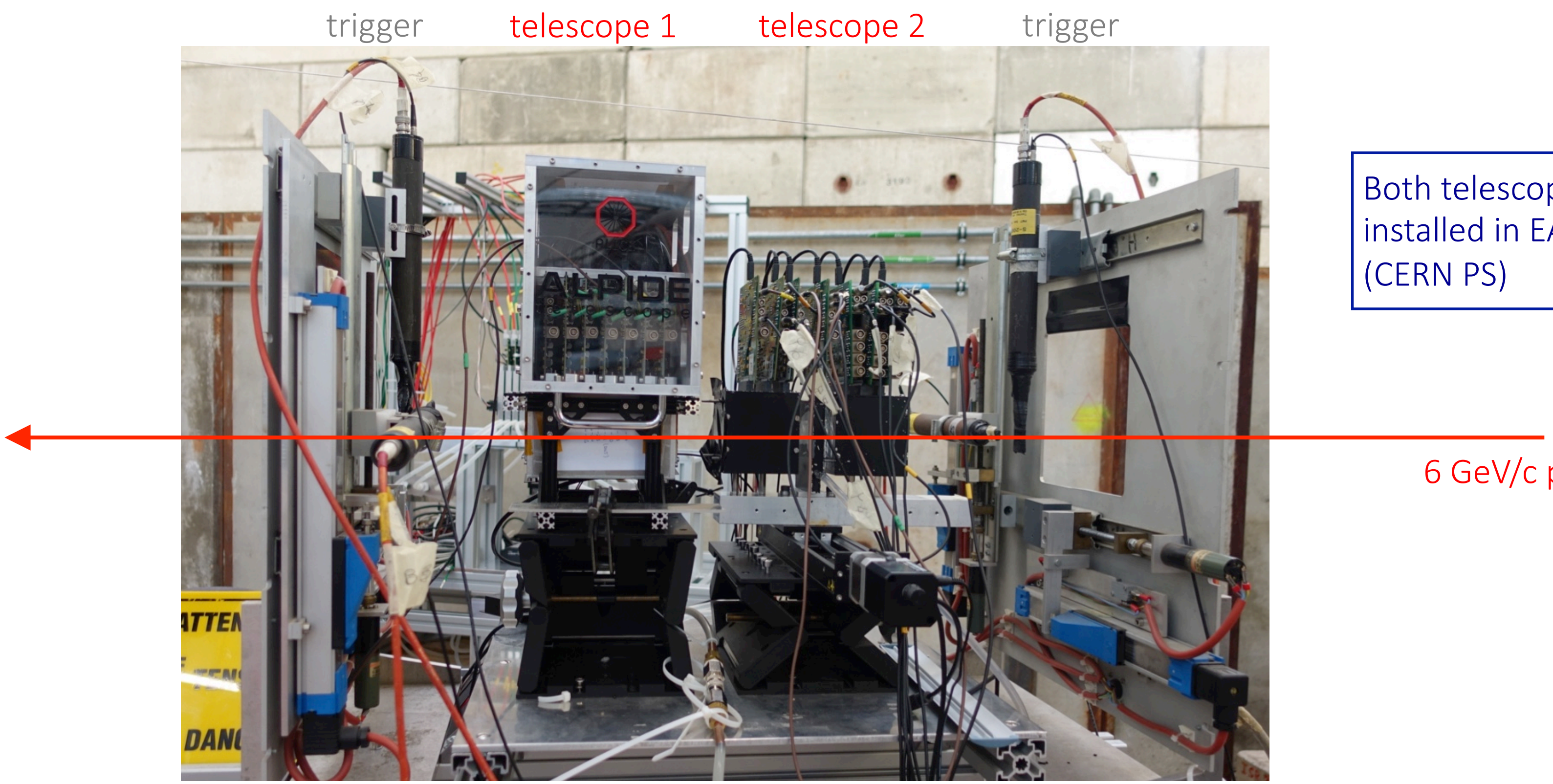


Telescope 2



ALPIDE Telescope

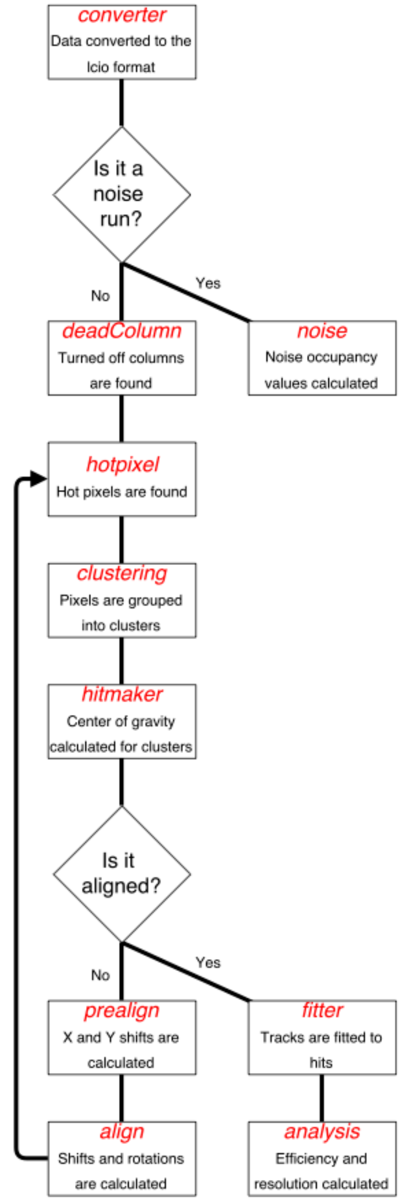
2. ALPIDE telescope



Both telescopes installed in EA T10 (CERN PS)

- ALPIDE telescopes successfully operated in various test beam facilities all over the world (CERN PS, DESY, BTF Frascati, Pohang/Korea, SLRI/Thailand)
- Simulated track resolution at DUT around 2-3µm with 6GeV/c pions
- Studied performance in terms of: detection efficiency, position resolution, cluster sizes and shapes

- DAQ using EUDAQ:
  - ALPIDE producer specialities:
    - Control of external equipment
    - Automatic reconfiguration for errors
    - Online data consistency checking (absolute and relative timestamps as well as trigger ids)
  - Automation:
    - Generation of configuration files
    - Changing configuration files after a certain number of events
    - Control of power supplies, pulser, linear and rotary stages
    - Watchdog sending texts and emails
      - Check EUDAQ control
      - Last event written
      - File size of current run
      - Out-of-sync
  - Like this about 1000 runs, each with a different setting (threshold, reverse bias, integration time, etc.), could be performed in 10 days without presence of shift crew
- Analysis using EUTelescope



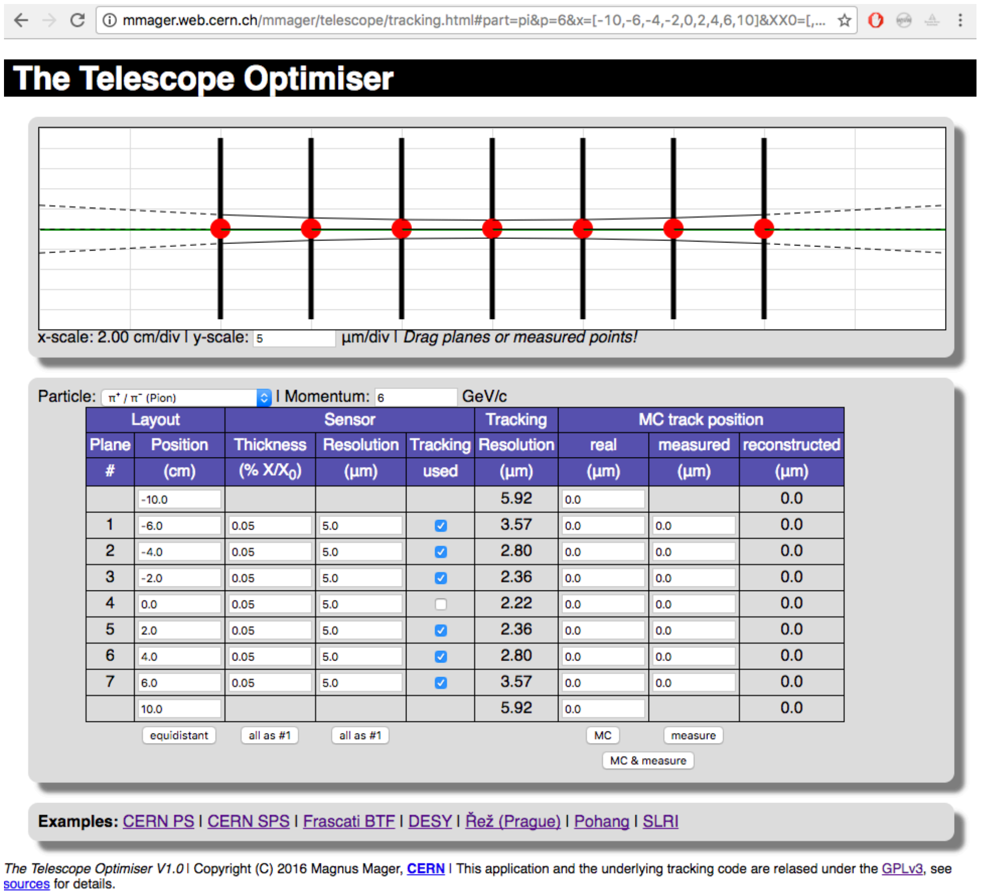
Nice online tool for optimizing telescope setup

- Variable parameters:
  - Plane position
  - Material budget per plane
  - Resolution per plane
  - Particle type and momentum

- Planes can be moved by mouse, results will be automatically updated
- Tracks and measured points in planes can be simulated

- One can also construct a setup by URL, see e.g. at bottom of this slide

- Page: http://mmager.web.cern.ch/mmager/telescope/tracking.html
- Source: https://gitlab.cern.ch/mmager/telescope-optimiser



Layout		Sensor			Tracking	MC track position		
Plane #	Position (cm)	Thickness (% X/X_0)	Resolution (µm)	Tracking used	Resolution (µm)	real (µm)	measured (µm)	reconstructed (µm)
	-10.0				5.92	0.0		0.0
1	-6.0	0.05	5.0	☑	3.57	0.0	0.0	0.0
2	-4.0	0.05	5.0	☑	2.80	0.0	0.0	0.0
3	-2.0	0.05	5.0	☑	2.36	0.0	0.0	0.0
4	0.0	0.05	5.0	☐	2.22	0.0	0.0	0.0
5	2.0	0.05	5.0	☑	2.36	0.0	0.0	0.0
6	4.0	0.05	5.0	☑	2.80	0.0	0.0	0.0
7	6.0	0.05	5.0	☑	3.57	0.0	0.0	0.0
	10.0				5.92	0.0		0.0

http://mmager.web.cern.ch/mmager/telescope/tracking.html#part=e&p=1&x=[-10,-6,-4,-2,0,2,4,6,10]&XX0=[,0.005,0.0005,0.0005,0.001,0.0005,0.0005,0.005,]&sy=[,0.0005,0.0005,0.0005,0.0005,0.0005,0.0005,0.0005,]&en=[0,1,1,1,0,1,1,1,0]&ymc=[0,0,0,0,0,0,0,0,0]&ym=[0,0,0,0,0,0,0,0,0]&scaley=0.0005

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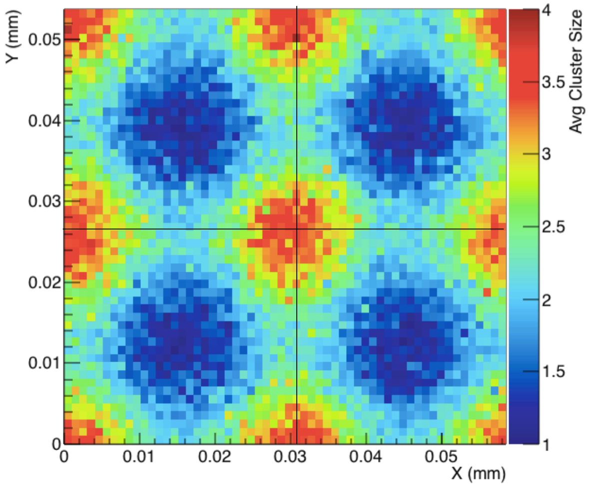
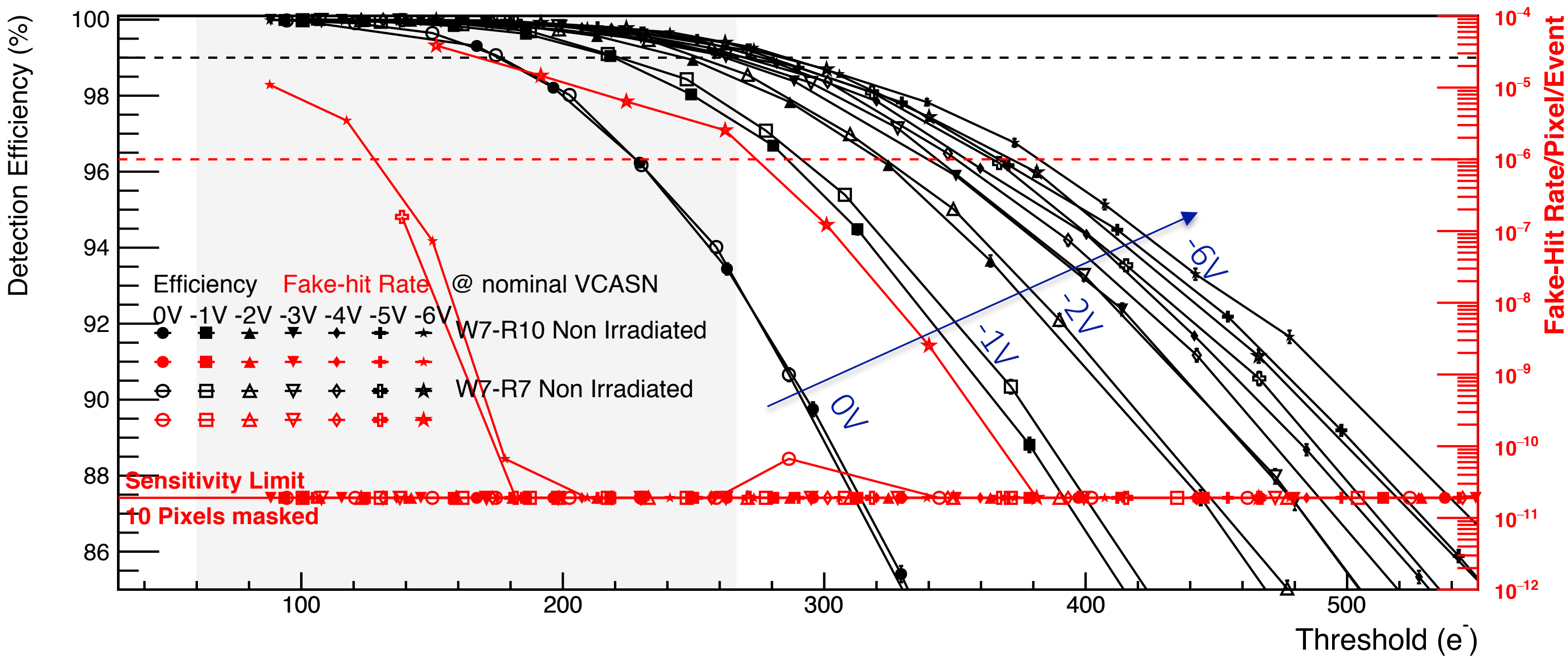


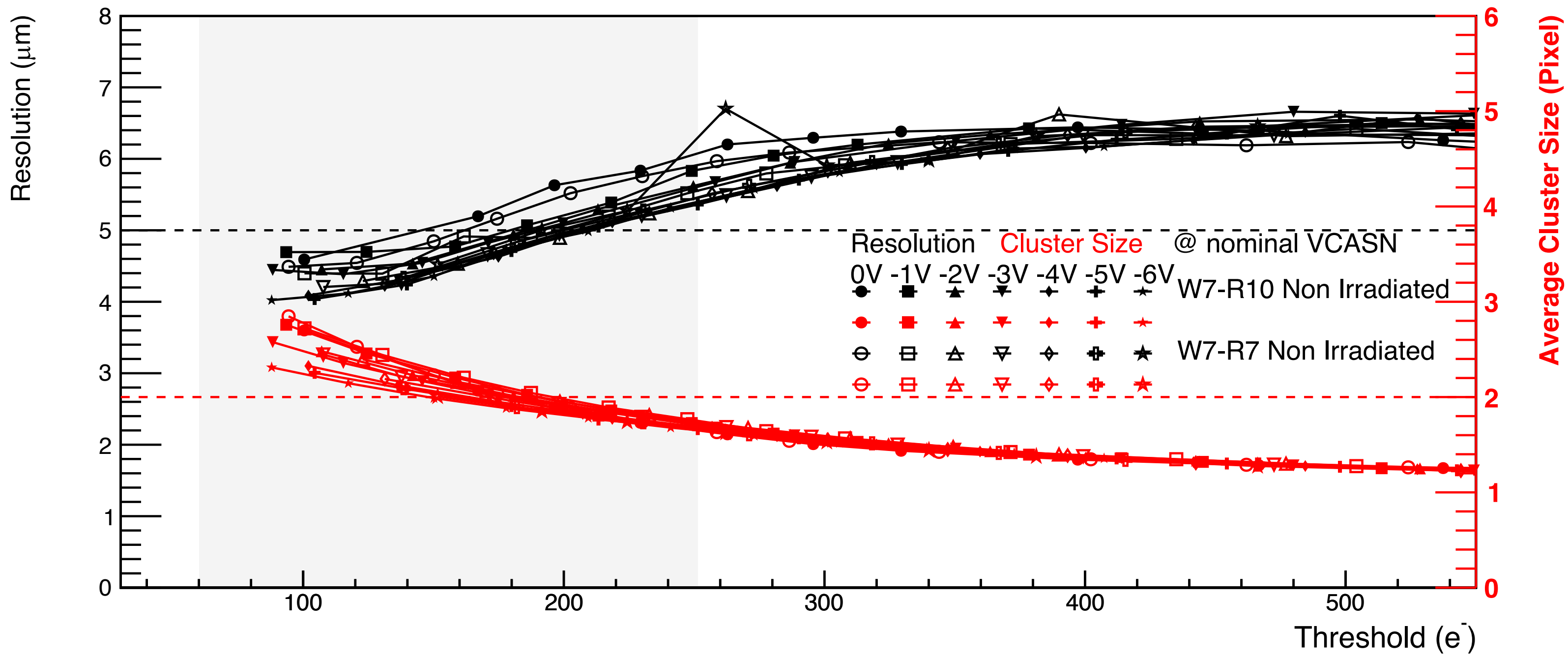
Detection efficiency and fake-hit rate

25µm epitaxial layer -> ~1600e⁻ produced produce by MIP (MPV)
-> then also charge sharing, Landau fluctuations to be considered..



- Detection efficiency stays at 100% - ε over wide range of thresholds
  - Chip-to-chip fluctuations negligible
- Clear ordering: increasing performance with larger reverse bias
  - Most significant improvement from 0V to -1V
- Extremely low fake-hit rate (Gaussian noise only 2-6 e^-)
  - Below measurement limit of 10^{-11}/pixel/event after masking 10 pixels (1/50 000), only increased for -6V

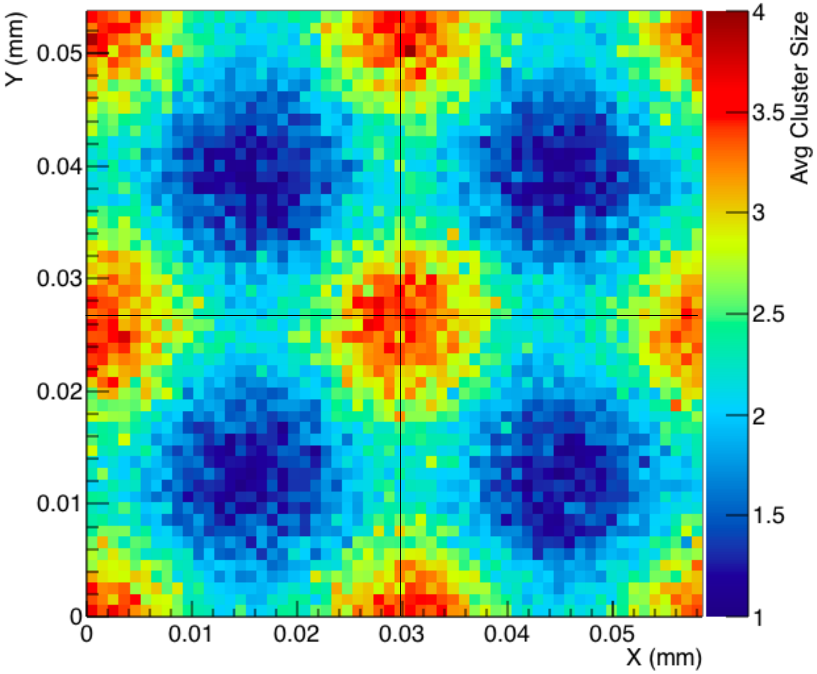
Position resolution and average cluster size

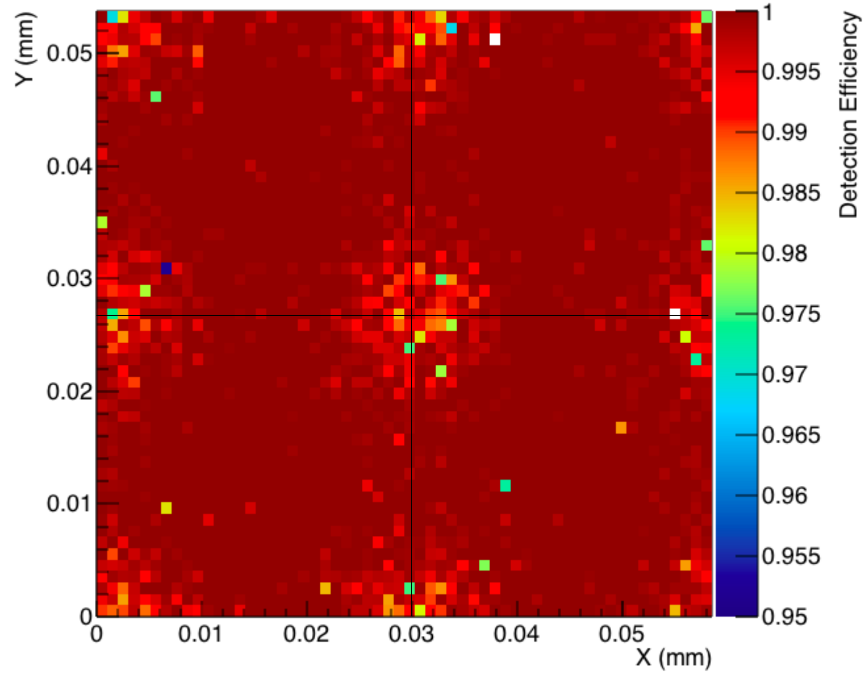


- Position resolution around desired 5μm in threshold range with detection efficiency > 99%
  - Biggest improvement from 0V to -1V
  - Little dependence on reverse bias from -2V to -6V
- Average cluster sizes vary between 1 and 3 pixels (for MIPs)

Cluster size and detection efficiency as function of the impinging point of the track within area of 2x2 pixels

- for reverse bias of -3V, threshold of ~180e$^-$ (high for ALPIDE!), 6GeV/c pions





- Cluster size strongly depending on impinging point: ~1 in pixel centers, ~4 in pixel corners
- At higher thresholds, detection efficiency first starts to drop in pixel corners <-> almost equal charge sharing between 4 pixels

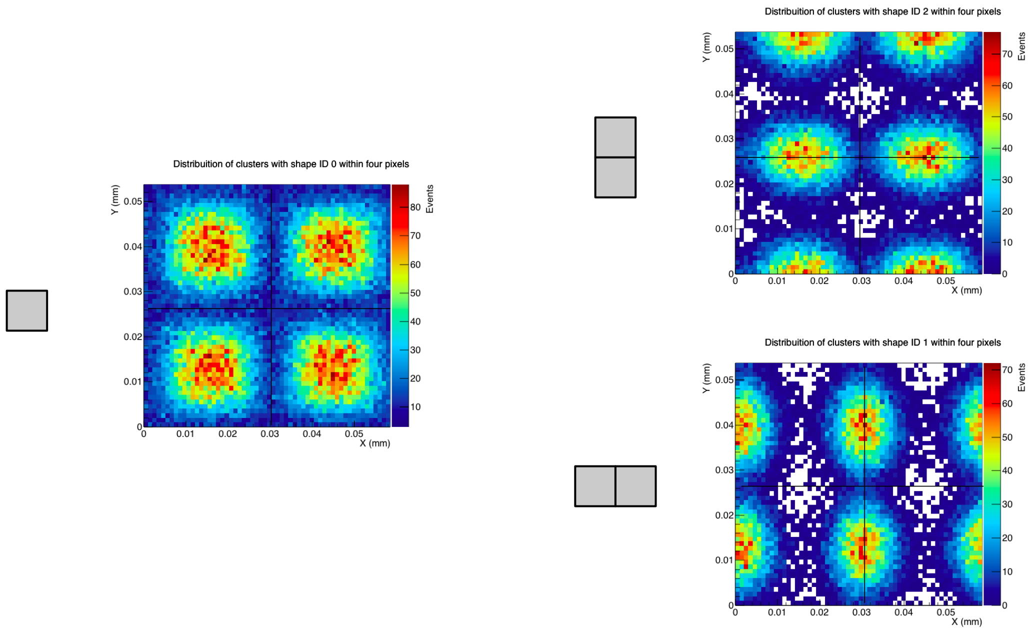
ALPIDE: Position-resolved results

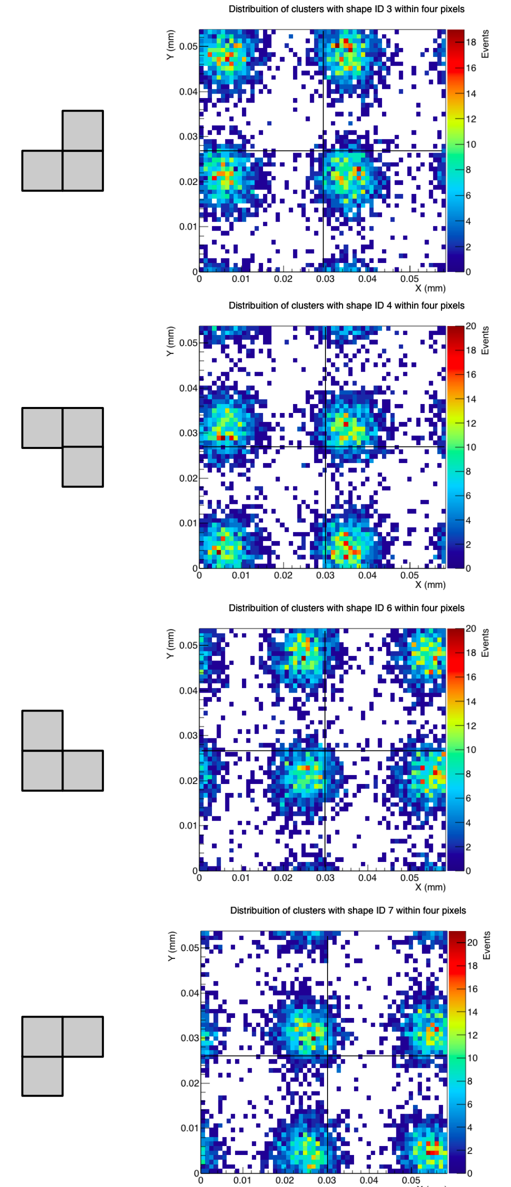
3. Selected results

Cluster shapes as function of the impinging point of the track within area of 2x2 pixels

- for reverse bias of -3V, threshold of ~180e[-] (high for ALPIDE!), 6GeV/c pions

Shape:





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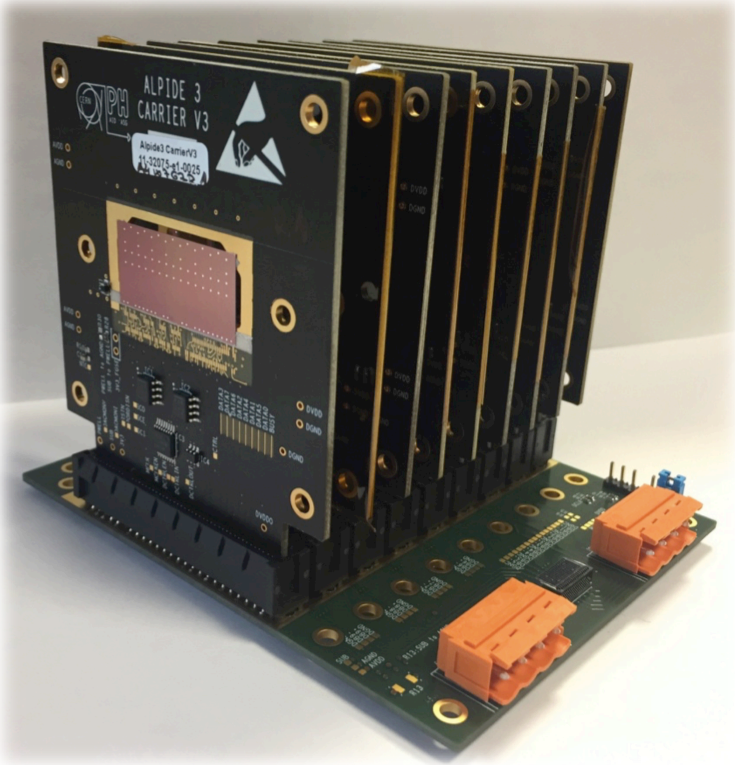


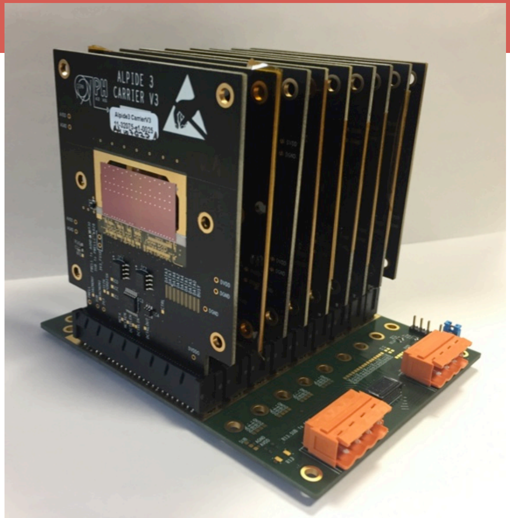
- Successfully designed and operated a 7-plane beam telescope fully consisting of ALPIDE chips
  - With 6GeV/c pions, a track resolution at the Device Under Test (DUT) of 2-3µm was reached
  - Setup highly automated: about 1000 runs, each with a different setting (threshold, reverse substrate bias, integration time, etc.), could be performed in 10 days without presence of a shift crew

- ALPIDE is very suitable chip for beam telescopes
  - Can be thinned down to only 50µm (0.05%x/X_0), making it suitable for high-resolution beam telescopes even at low beam energies
  - 3cm x 1.5cm in size
  - Spatial resolution of ~5µm
  - Event-time resolution of <4µs (a single additional plane with better timing resolution could easily be added to improve this)
  - Global shutter architecture

- Hardware:
  - 9-plane telescope with high-speed back plane
    - Plane distance of only 1cm
    - Using ITS Inner Barrel module readout topology with 9 1.2Gbit/s serial links
    - Connected via firefly cable (up to 5m) to ITS Readout Unit (RU) prototype
    - RU connected via USB-3.0 to PC
  - Test beam with ITS modules

- Software:
  - Generalise EUDAQ producer to
    - our other readout systems (including the Readout Unit)
    - cover both single chips and modules
  - Update our analysis code w.r.t. general EUTelescope developments

- High precision measurements with different angles of beam incidence
  - First tries with summer student last summer, but desired track resolution not yet achieved
  - Setup (plane distances) to be optimized, go to SPS to reduce multiple scattering
  - Analysis software



BACKUP

ALICE ITS pixel chip requirements
2. ALPIDE

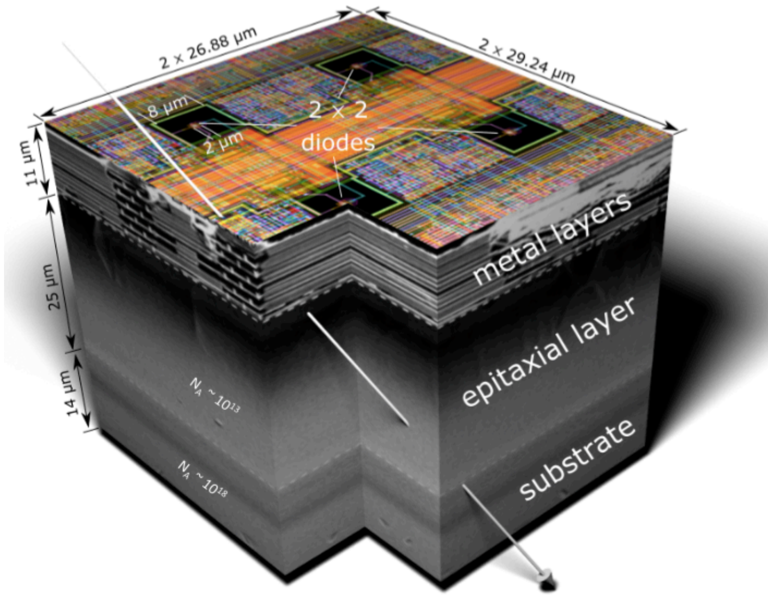
Parameter	Inner Barrel	Outer Barrel	ALPIDE
Silicon thickness	50µm		✔
Spatial resolution	5µm	10µm	~5µm
Chip dimension	15mm x 30mm		✔
Power density	< 300mW/cm^2	< 100mW/cm^2	< 40mW/cm^2
Event time resolution	< 30µs		~2µs
Detection efficiency	> 99%		✔
Fake hit rate	< 10^{-5}/event/pixel		<<< 10^{-6}/event/pixel
NIEL tolerance	1.7x10^{12} 1MeV n_{eq}/cm^2	10^{11} 1MeV n_{eq}/cm^2	>1.7x10^{13} 1MeV n_{eq}/cm^2
TID tolerance	270krad	10krad	>500krad

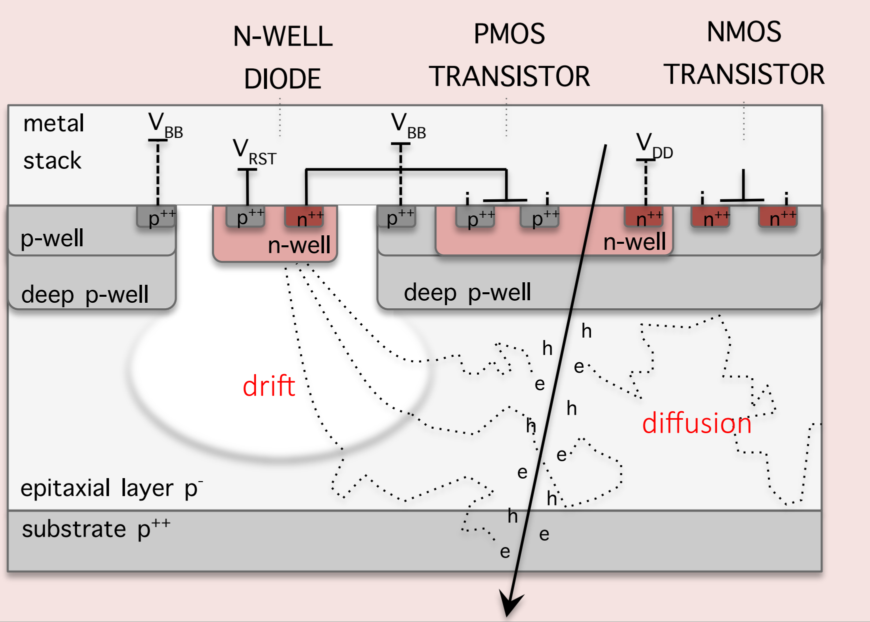
- ALPIDE fulfills or surpasses pixel-chip requirements of the ALICE ITS upgrade
- ALPIDE development represents significant advancement of MAPS regarding power density, fake-hit rate, readout speed, and radiation hardness

TowerJazz 180nm CMOS imaging sensor process:

- High-resistivity (>1kΩcm) p-type epitaxial layer (18μm-40μm) on p-type substrate (~10Ωcm)
- Deep p-well for full CMOS circuitry within the matrix
- Feature size 180nm and 6 metal layers ➔ dense circuitry

Sensor only partially depleted ➔ application of moderate reverse bias V_{BB} (<6V) possible via the substrate





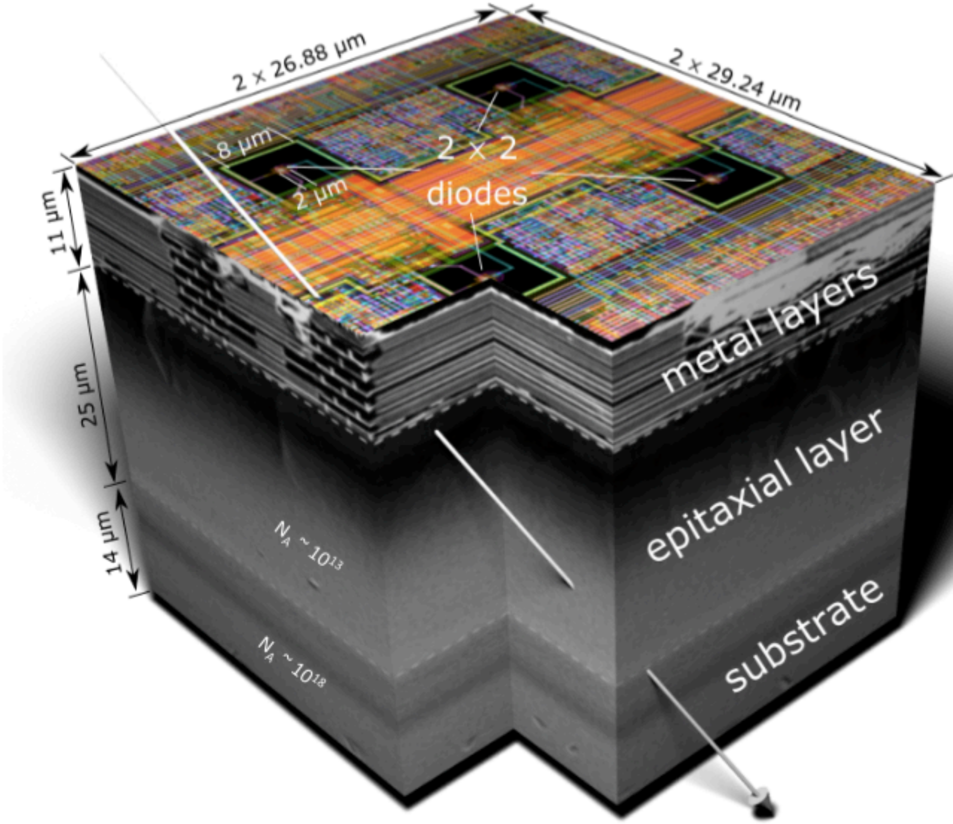
Signal from collection diode: ΔV ~ Q/C

- particular focus put on low pixel-input capacitance C
- ➔ values as low as 2fF achieved (signal of 80mV for 1000e$^-$)

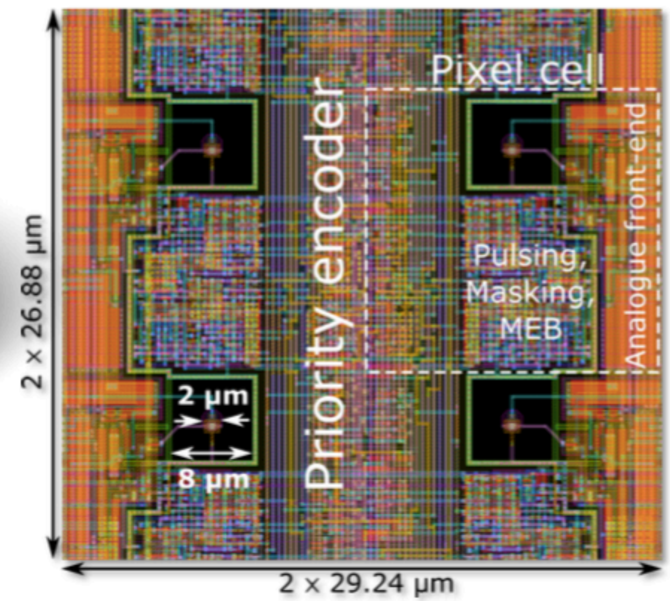
Charge collection time: ~1-30ns

- depending on size of depletion zone (reverse substrate bias, collection diode geometry)

3D and 2D view of 2x2 pixels



full CMOS circuitry within pixel matrix



ALPIDE in-pixel circuitry

- Front-end: continuously active, power consumption 40nW (9 transistors, full custom)
- Multi-event memory: 3 stages (62 transistors, full-custom)
- Configuration: masking and pulsing registers (31 transistors, full-custom)
- Testing: analog and digital test pulse circuitry (17 transistors, full-custom)
- Matrix read-out: priority encoder, asynchronous, hit-driven

Q/C ratio and sensor design parameters

2. ALPIDE

Sensor performance mainly determined by:

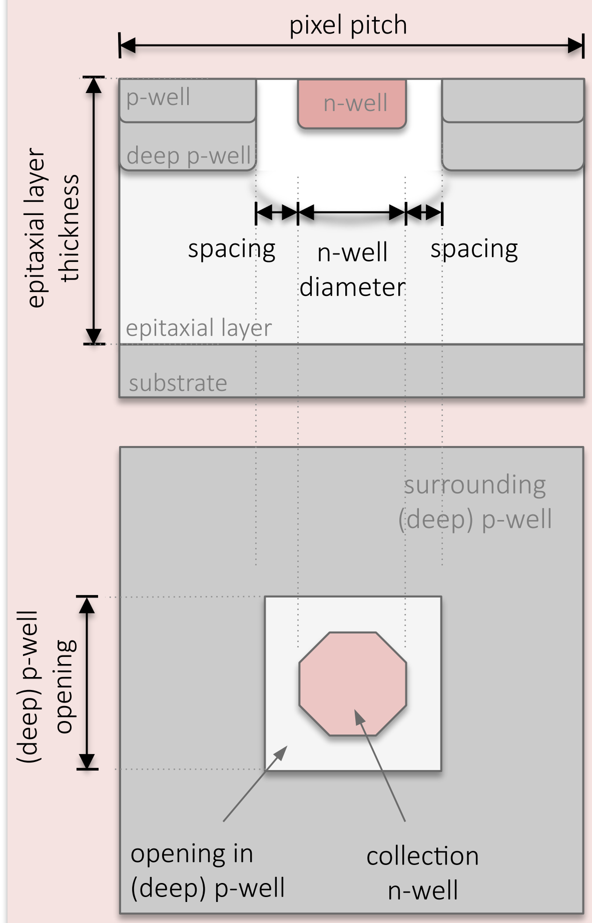
- Pixel pitch
- Collection n-well size
- Spacing between the collection n-well and surrounding(deep) p-well
- Epitaxial layer thickness and resistivity
- Reverse bias voltage V_{BB} on the collection diode

- Sensor optimization studies mainly by small-scale prototypes with analog readout
- During design of ALPIDE, particular focus put on low pixel-input capacitance C
  - ➔ values as low as 2fF achieved (signal of 80mV for 1000e$^-$)

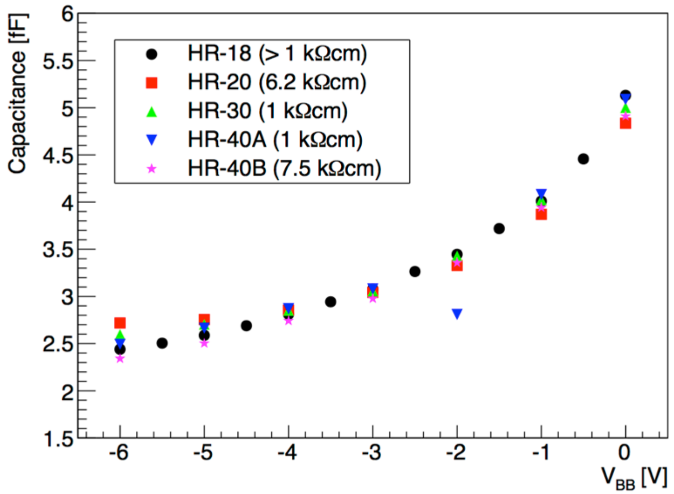
Parameters selected for ALPIDE (29µm x 27µm pixel size):

- 25µm epitaxial layer
- 2µm n-well diameter, 3µm spacing
  - ➢ 88% of pixel surface can be used for circuitry

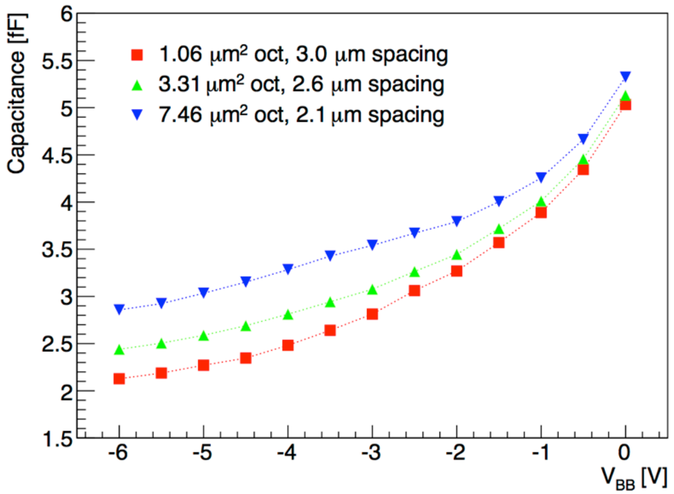
Pixel and collection electrode geometry (not to scale):

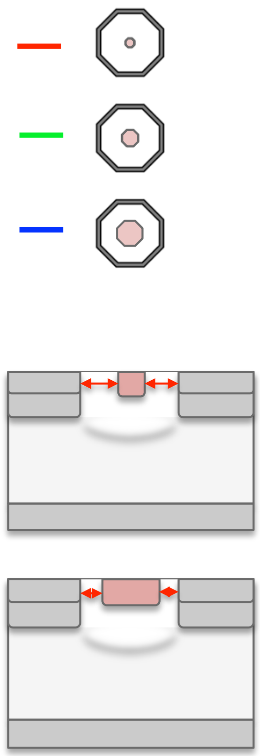


Epitaxial layer resistivity



Collection diode geometries:





Pixel input capacitance significantly decreased with increasing $|V_{BB}|$

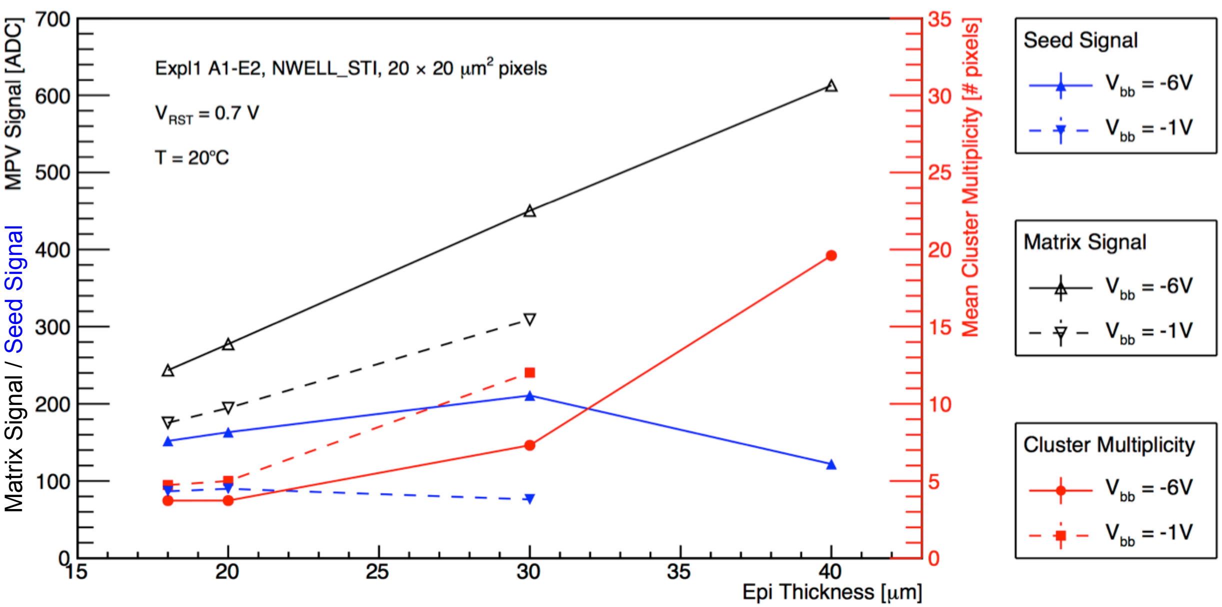
- ~5fF for V_{BB}=0V ➔ ~2.5fF for V_{BB}=-6V

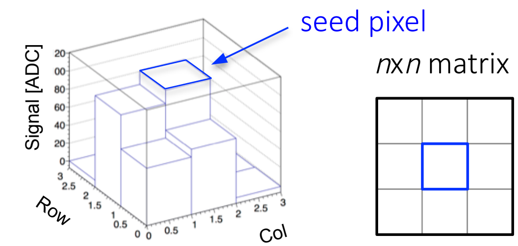
Epitaxial layer resistivity

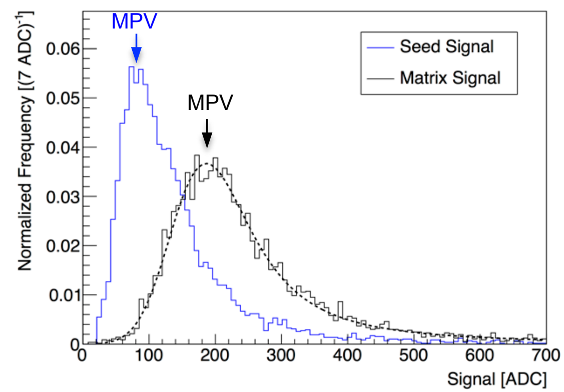
- No influence in range between 1kΩcm and 7.5kΩcm with current pixel layout

Collection diode geometry

- smaller collection n-well, larger spacing ➔ smaller pixel input capacitance at large V_{BB}







Prototypes produced on wafer with different epitaxial layer thickness and resistivity

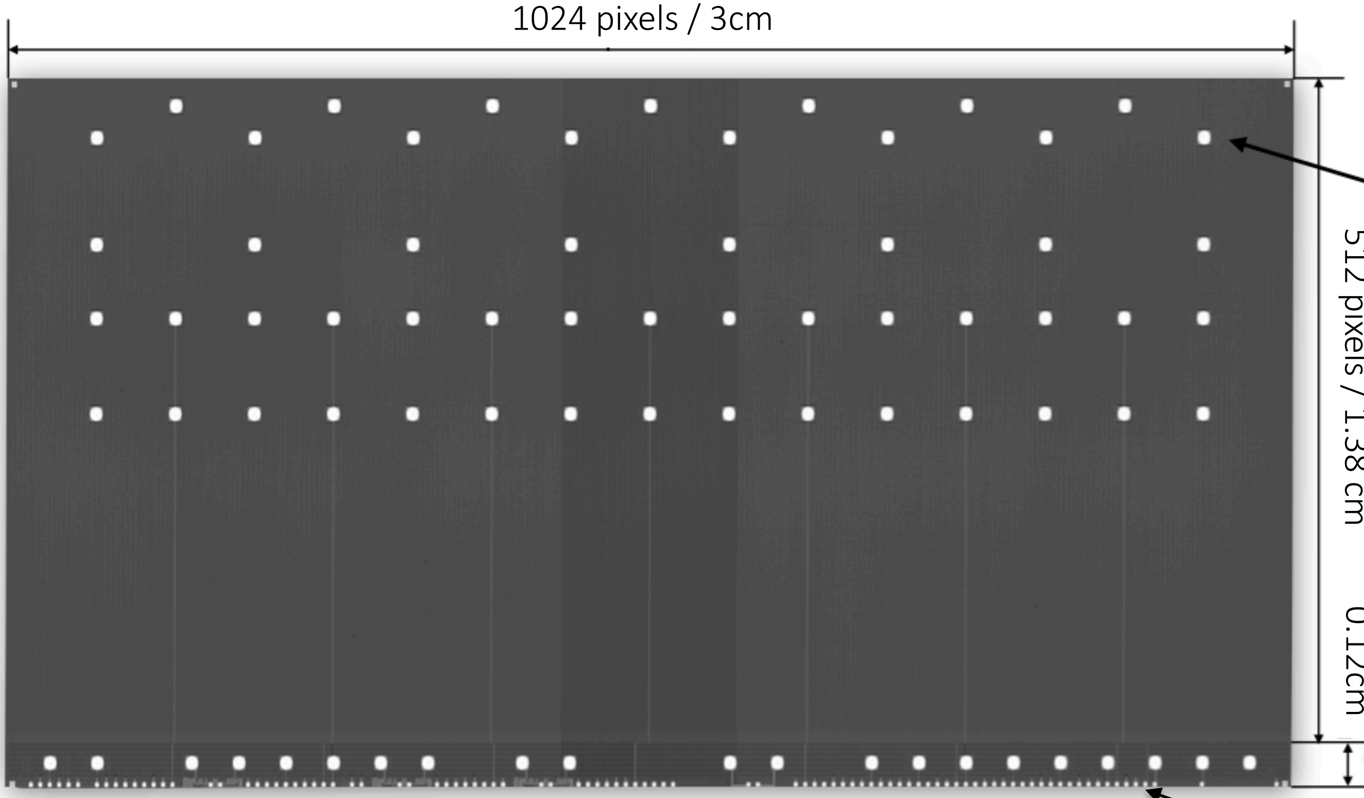
- increasing epitaxial layer thickness:
  - generated charge (matrix signal) increases linearly
  - cluster size increases non-linearly

Optimum epitaxial layer thickness depending on achievable depletion volume

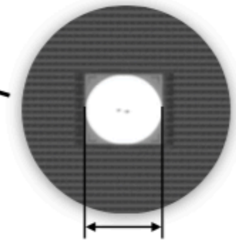
➔ depending on V_{BB} and geometry

Parameters selected for ALPIDE: 25μm epitaxial layer, 2μm n-well diameter, 3μm spacing

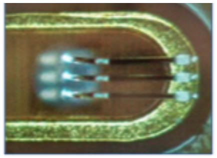
ALPIDE: Floor plan



interface pads over matrix



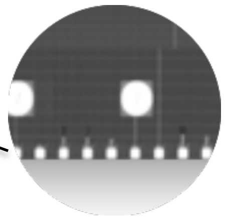
used for wire bonding on modules



pixel matrix

analogue biasing and digital interface circuitry

interface pads at periphery



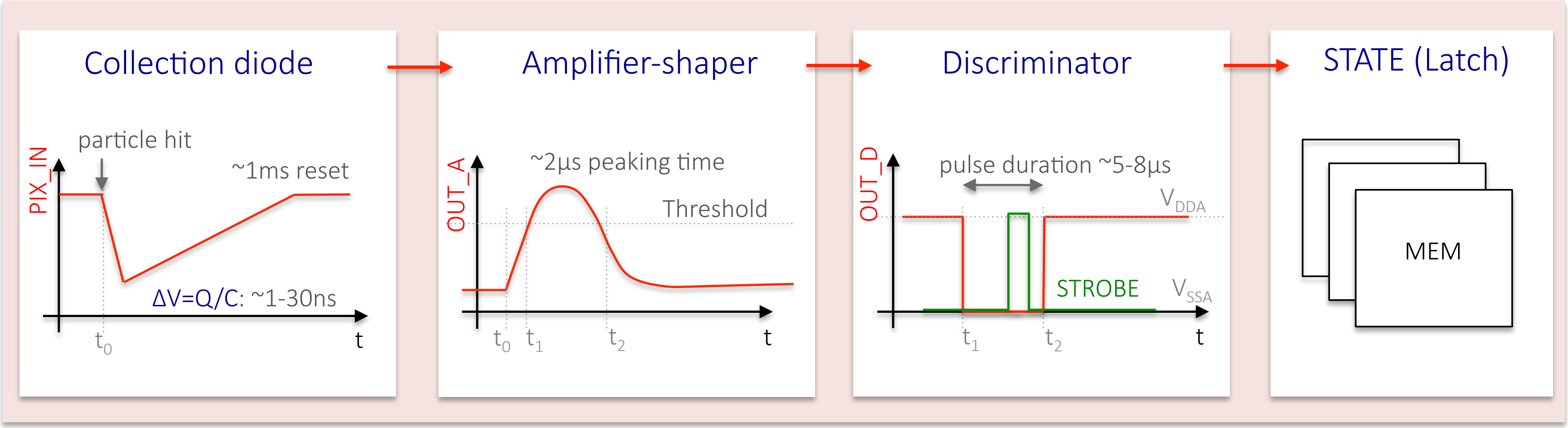
used for wire bonding carrier cards

Features:

- Dimension: 30mm x 15mm (1024 x 512 pixels)
- Pixel pitch: 29µm x 27µm
- Thinned to 50µm or 100µm
- Global shutter: triggered acquisition (up to 200 kHz Pb-Pb, 1MHz pp) or continuous (progr. integration time: 1µs - ∞)

Concepts:

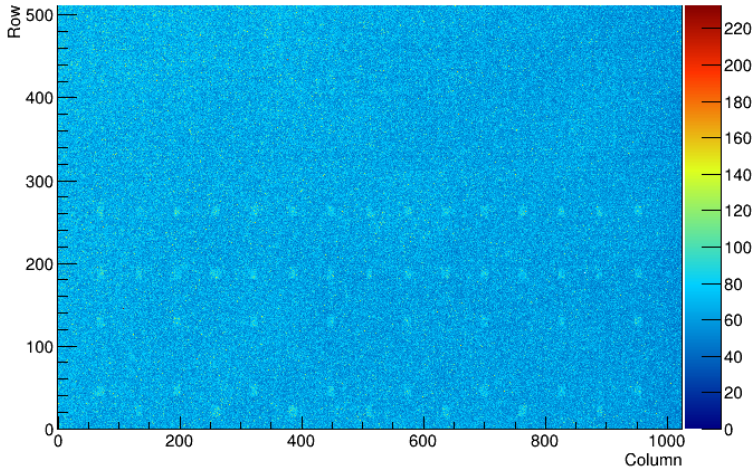
- In-pixel amplification
- In-pixel hit discrimination
- In-pixel 3-level event memory
- In-matrix zero-suppression

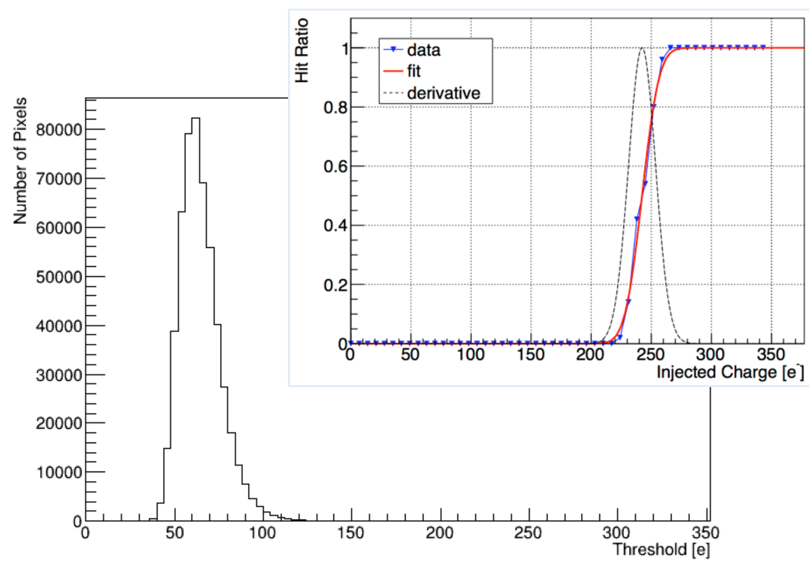


Front-end acts as delay line

- Sensor and front-end continuously active
- Upon particle hit front-end forms a pulse with peaking time of 2-4µs (<-> time walk)
  - charge collection time < 30ns! -> long pulse duration a choice made for ALICE ITS: functioning as delay line and reduce power consumption (40nW/pixel) <-> material budget
- Threshold is applied to form a binary pulse
  - globally set by front-end bias DACs
- Hit is latched into memory if STROBE is applied during binary pulse
  - Global shutter: triggered (up to 200 kHz Pb-Pb, 1MHz pp) or continuous (progr. integration time: 1µs - ∞)

- Threshold globally adjustable via on-chip DACs
- Good threshold uniformity
  - Threshold RMS 10-15% of average threshold
- Very low noise values
  - 5-6e$^-$ without reverse substrate bias, 2-3e$^-$ with
- Large threshold-to-noise ratio
  - Fake-hits due to Gaussian noise extremely rare
- Large operational margin
  - MIPs release in order of 1600e- (MPV) in sensitive layer (Landau fluctuations, charge sharing also to be considered..)

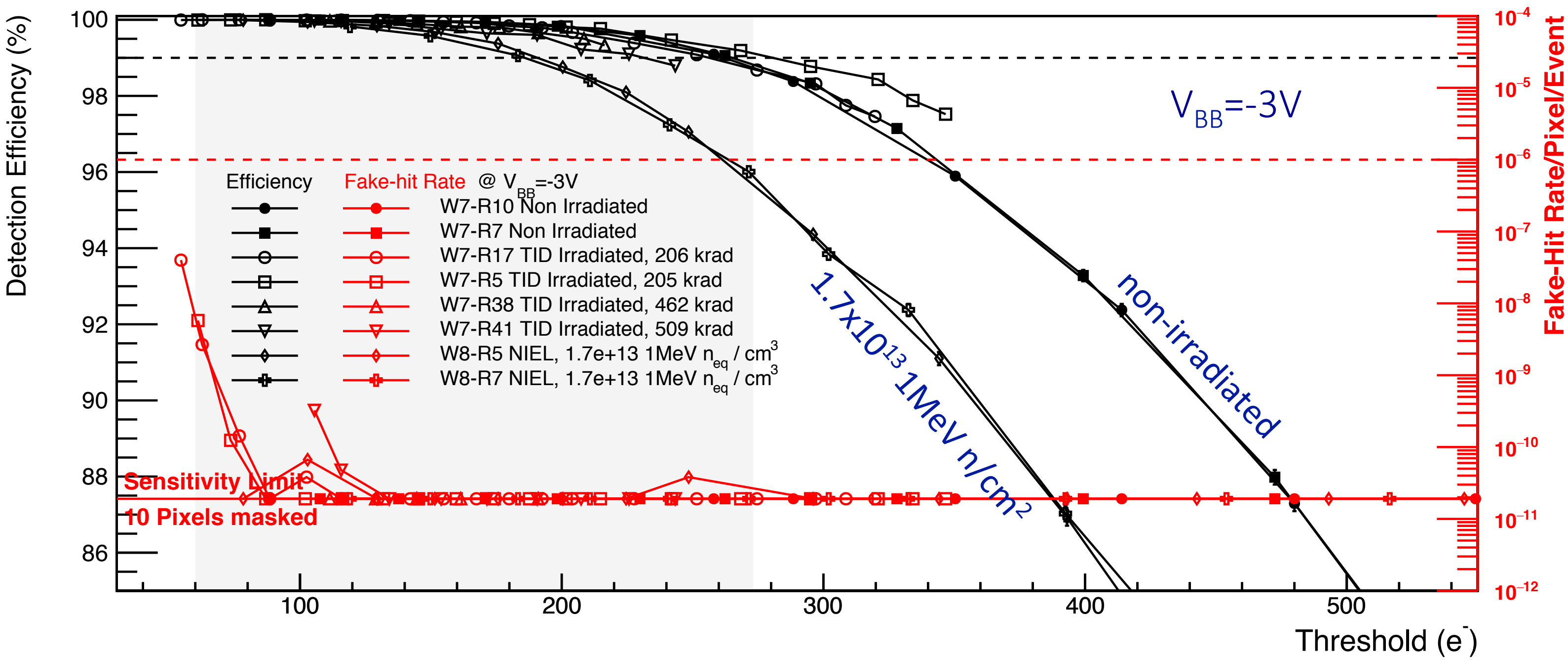




Performance after NIEL and TID irradiation

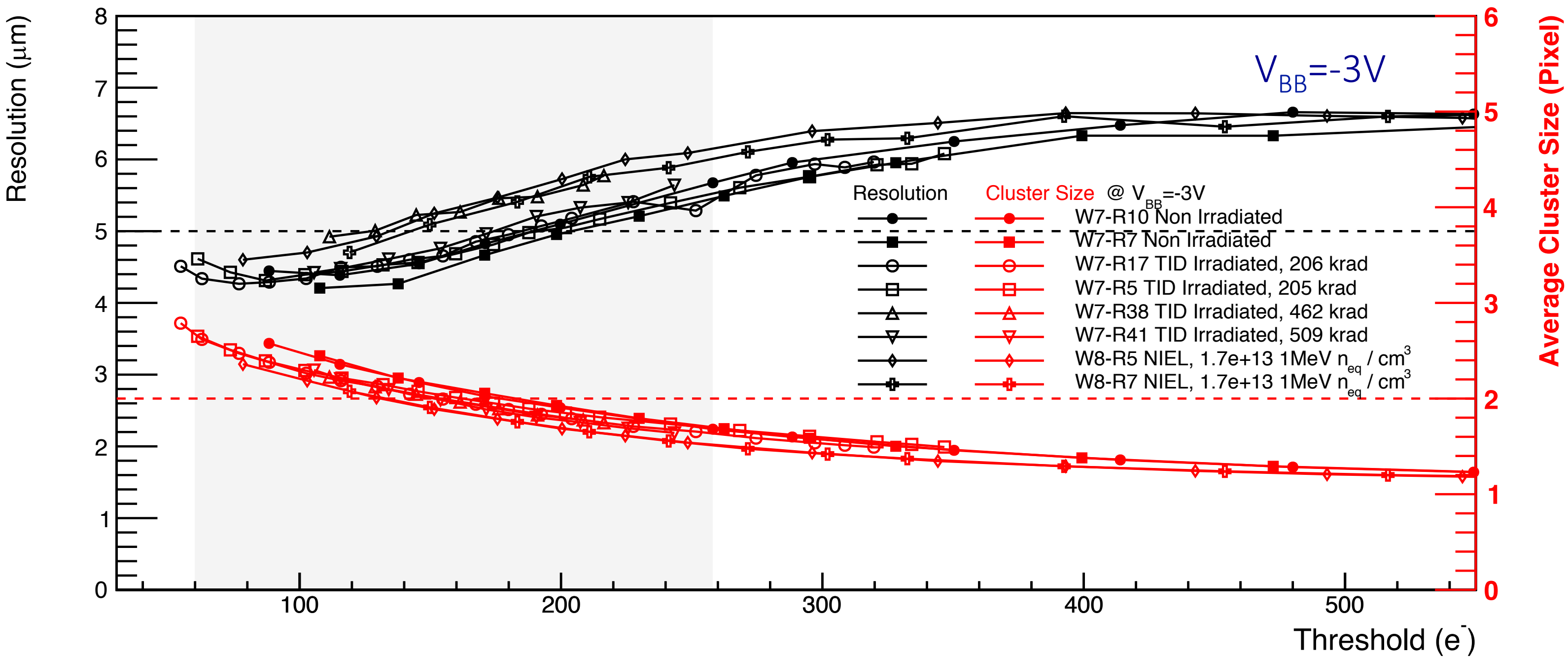
2. ALPIDE

Detection efficiency and fake-hit rate

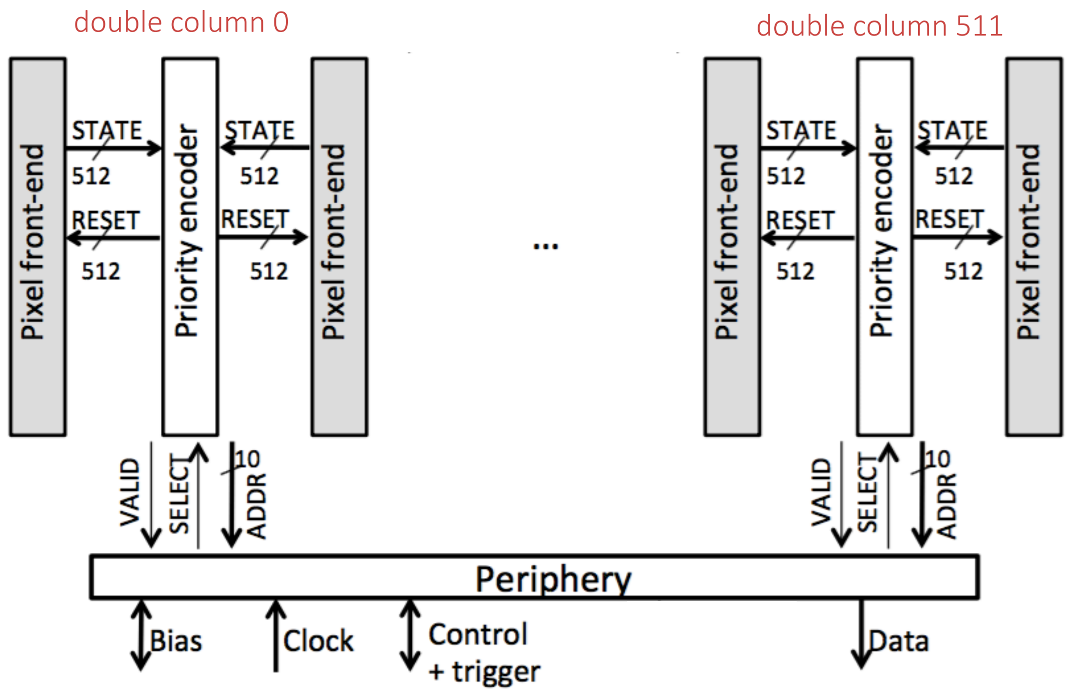


- Sufficient operational margin after $1.7\text{x}10^{13}$ 1MeV n/cm^2 (10 times life time dose of upgraded ITS)

Position resolution and cluster size



- Cluster sizes and position resolution slightly reduced after 1.7×10^{13} 1MeV n/cm^2 (10 times life time dose of upgraded ITS)
  - Resolution remains around desired 5μm in threshold range with detection efficiency > 99%



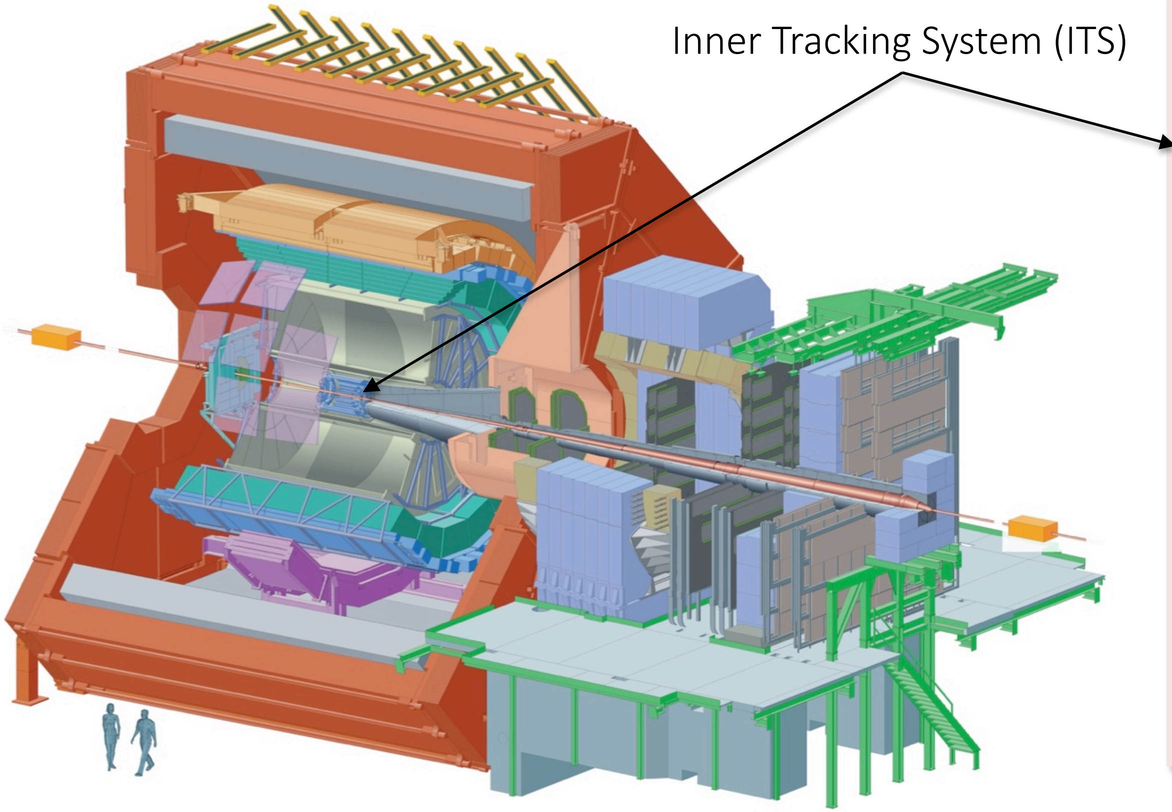
Matrix readout by hit-driven asynchronous circuit (priority encoder) in double-columns:

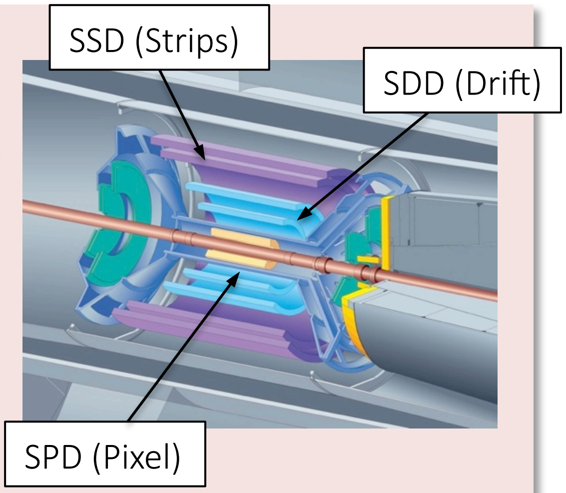
- sequentially provides addresses only of hit pixels ➔ in-matrix zero suppression, fast
- no activity if not hit (no free running clock) ➔ low-power matrix readout (~2mW)

- Readout time: 1 clk cycle (20MHz) for one hit
- Minimum event size: chip header (16bit), region header (8bit), short data(16bit), trailer (8bit) -> 48 bit

- ALICE prepares major upgrade of experimental setup in LS2 of LHC in 2019/2020
- Targets:
  - Large sample of recorded events: 10 nb^{-1} Pb-Pb plus pp and p-Pb data -> gain factor 100 in statistics over originally approved program
  - Significant improvement of tracking and vertexing capabilities at low p_T

➔ also present ITS needs to be upgraded!



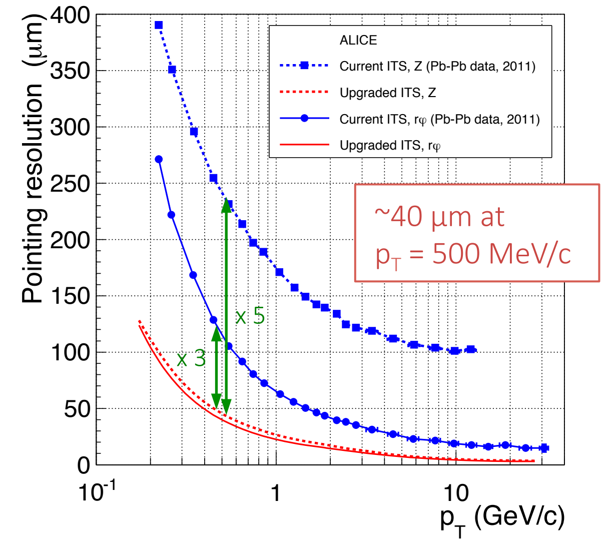


6 layers:

- 2 layers silicon pixel (SPD)
- 2 layers silicon drift (SDD)
- 2 layers silicon strips (SSD)

Improve pointing resolution by a factor ~3 in r-ϕ and ~5 in z at p_T=500MeV/c (~40 μm at p_T = 500 MeV/c)

- reduce beam pipe radius: 29mm ➔ 19mm
- get closer to IP: 39mm ➔ 22mm (innermost layer)
- reduce material budget: ~1.14% x/X_0 ➔ ~0.3% x/X_0 (inner layers)
  ➔ less material ➔ reduce power consumption
- reduce pixel size: 50x425μm² ➔ O(30x30μm²)

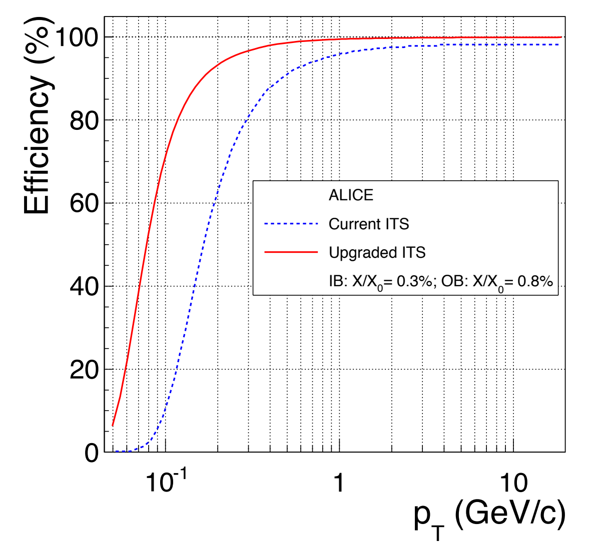


Improve tracking efficiency and p_T-resolution at low p_T

- increase granularity: 6 layers ➔ 7 layers, only pixel sensors

Fast readout

- readout of Pb-Pb at up to 100 kHz (presently 1kHz) and 400kHz for pp



Fast insertion/removal of detector modules

- possibility to replace non-functioning detector modules during yearly shutdown

➔ Decision to fully replace present ITS

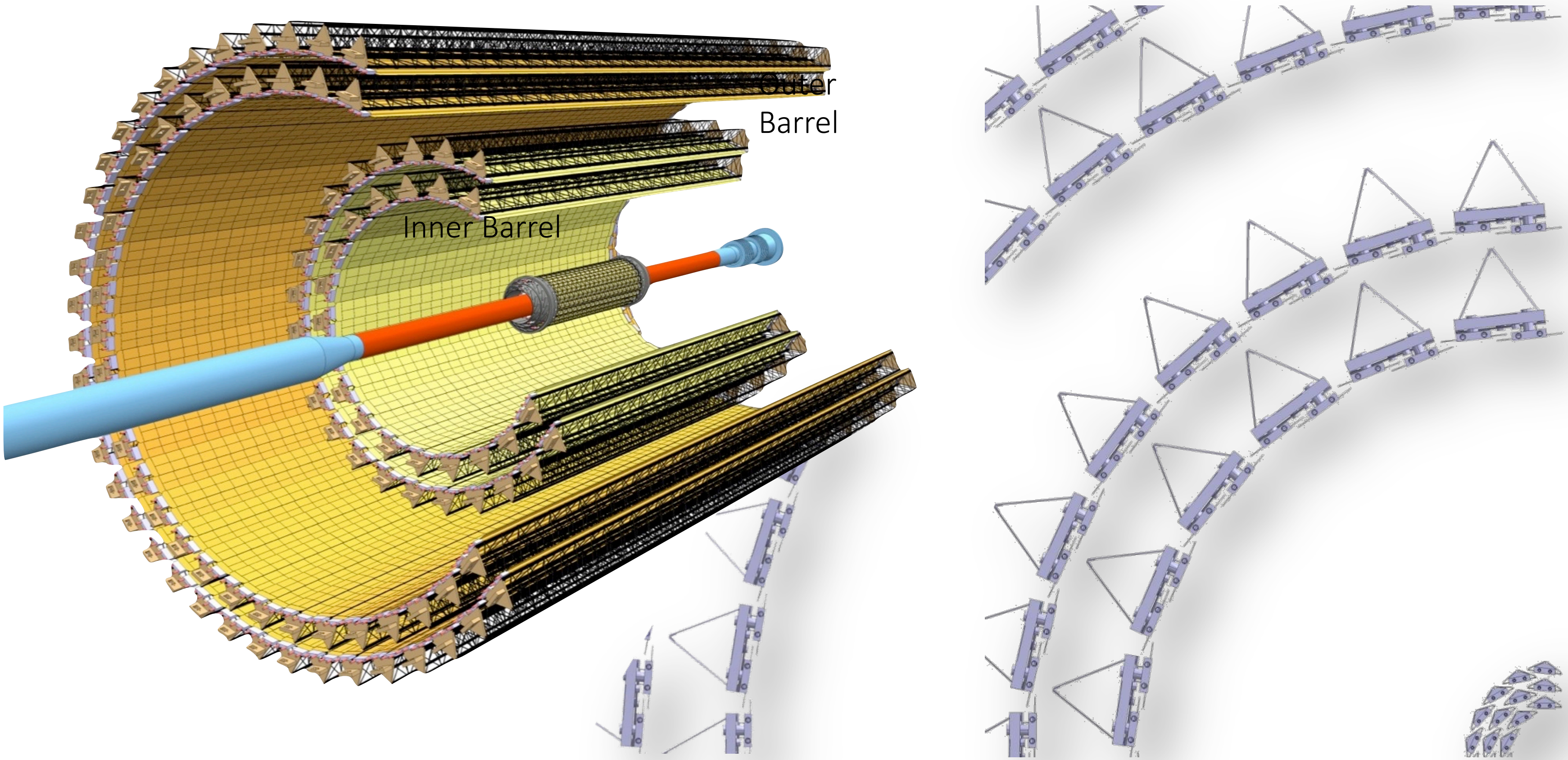
Layout of new ALICE Inner Tracking System

1. Introduction

7-layer geometry:

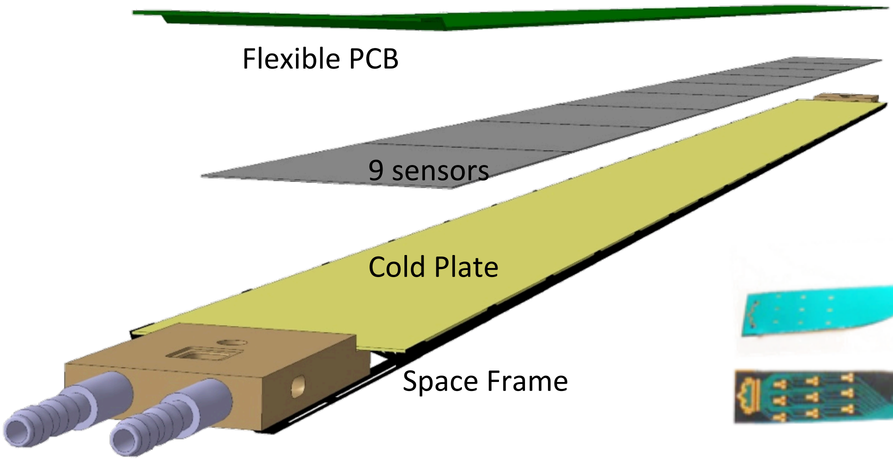
- r-coverage: 23 mm - 400 mm
- η-coverage: |η|≤ 1.22 for tracks from 90% luminous region

- 3 Inner Barrel layers: 0.3% x/X_0 per layer
- 4 Outer Barrel layers: 1% x/X_0 per layer



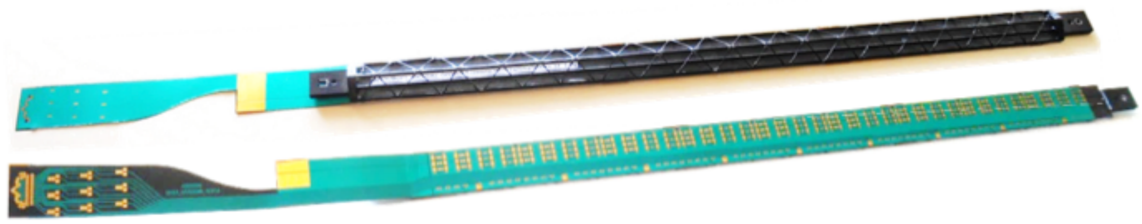
Layer n.	6	5	4	3	2	1	0
N. of staves	48	42	30	24	20	16	12
Stave length	1500 mm		900 mm		290mm		

Inner Barrel stave

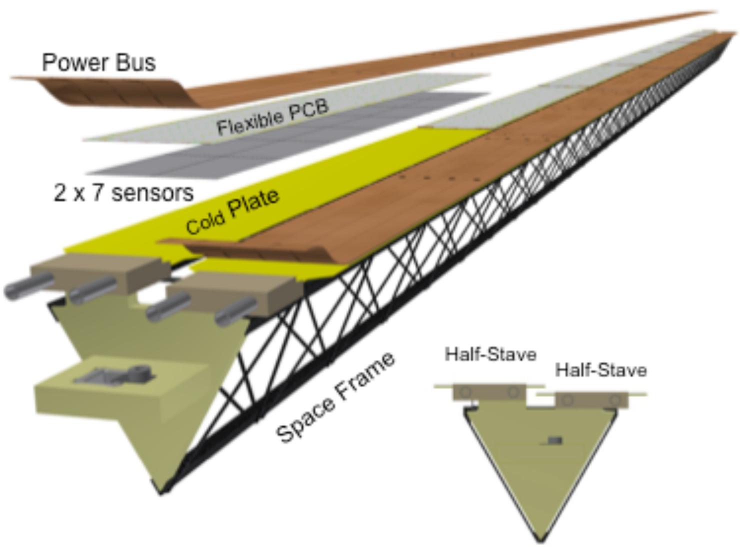


Inner barrel module (x48):

- 9 chips, each read out using 1.2 Gb/s link

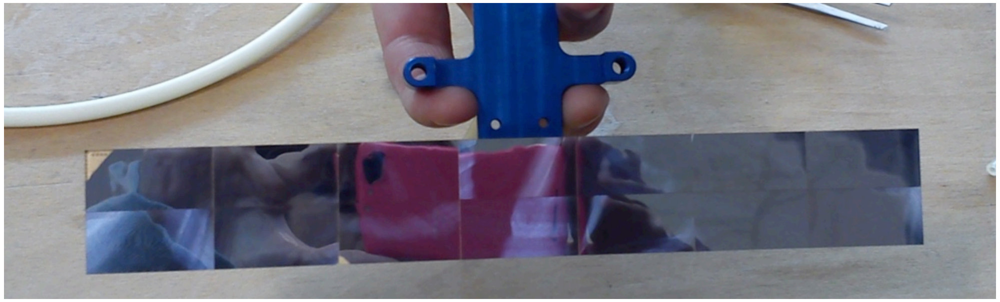


Outer Barrel



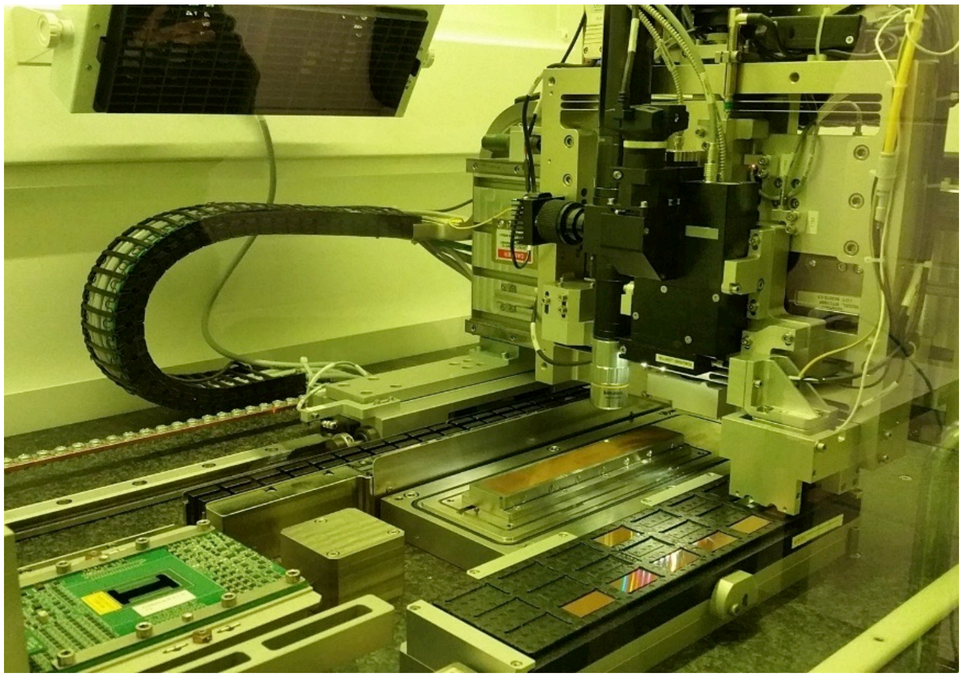
Outer barrel module (x1800)

- 2×7 chips (1 master, 6 slaves), locally interconnected, read out using 2×400 Mb/s links



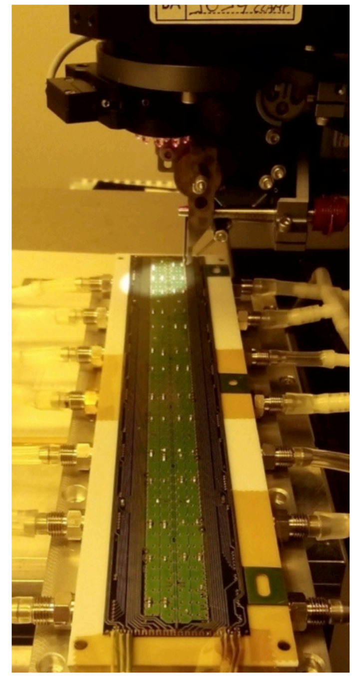
Module (HIC – hybrid integrated circuit): chips glued and wire-bonded to flexible PCB

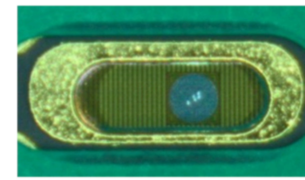
Chip placement + gluing to flexible PCB

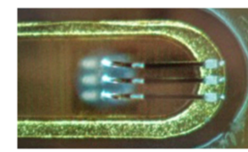


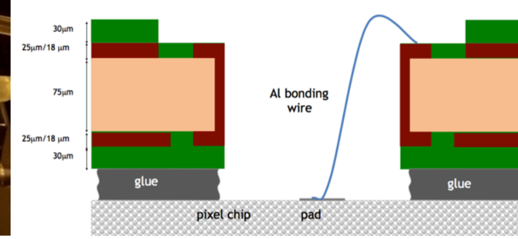
- Placement is handled by automated custom-made machine (distributed to 6 assembly sites worldwide)
- Flexible PCB is glued to chips

Wire bonding



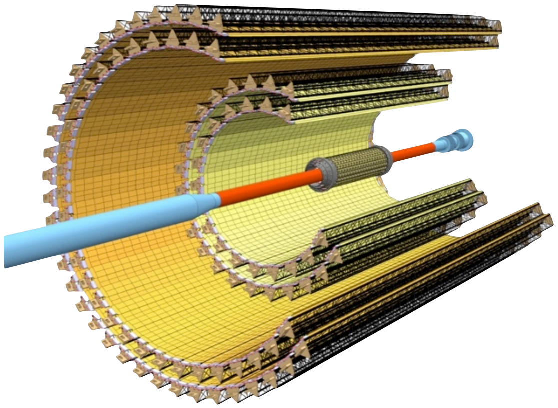






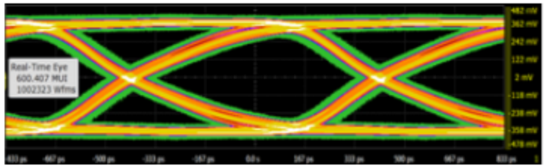
- Chips are wire bonded through vias in the FPCB distributed over full chip surface

Detector



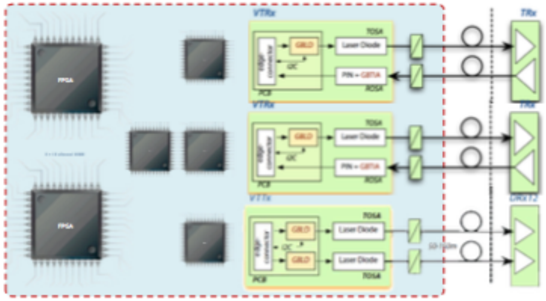
- Readout logic fully integrated into ALPIDE
- ALPIDE can directly drive 5m cables using integrated high-speed transmitters (up to 1.2 Gb/s)
- No further electronics on detector

5m cable

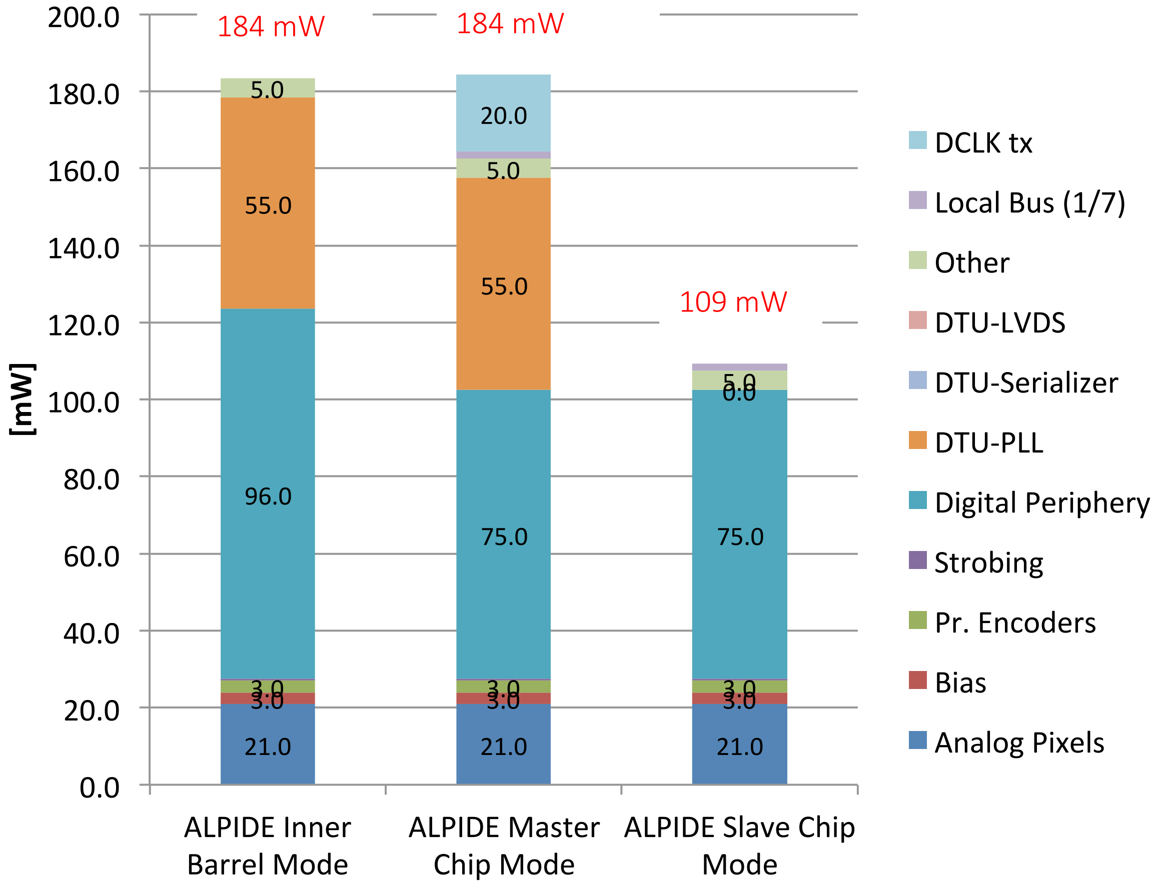


- 1.2 Gb/s (data IB)
- 400 Mb/s (data OB)
- 80 Mb/s (ctrl IB/OB)
- Clock
- Power

Readout units



- Total: 192 Readout Units
- Distribute trigger and control signals
- Interface data links to ALICE DAQ
- Control power supplies of chips



Inner Barrel: 41 mW/cm^2

Outer Barrel: 27 mW/cm^2

Data: combination of available measurements and simulations

Values scaled for readout at 100 kHz rates and max occupancies

Clock gating enabled

Test chip: INVESTIGATOR

3. Future developments

- INVESTIGATOR: dedicated test chip developed within ALPIDE R&D phase, designed for systematic studies on influence of design parameters on sensor characteristics

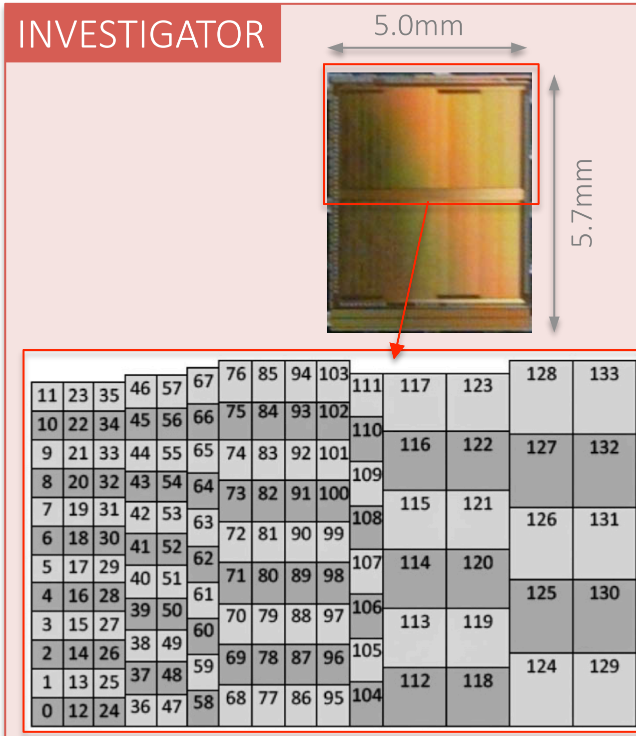
- Consists of 134 matrices of 8x8 pixels ("mini-matrices", MM)
  - Various pixel sizes (20x20µm^2 to 50x50µm^2) and collection electrode designs (n-well size, spacing)

- Each of the mini-matrices can be selected and connected to a set of 64 output buffers (~10ns rise time)
  - All 64 pixels of a mini-matrix can be read out in parallel, allowing for continuous parallel signal sampling
  - Possibility of measuring evolution of a cluster, i.e. charge collection time in each pixel
  - Dedicated 64-channel readout system developed, sampling at 65MHz

✓ Chips produced on different wafers with epi-layer thickness between 18µm and 30µm, and in different process variants (std, mod)

  ✓ Samples tested up to 10^{15} 1MeV n_{eq}/cm^2 and 1Mrad

INVESTIGATOR



MM address	Pixel pitch [µm]	Number of MM (per pitch)
0 - 35	20	36
36 - 57	22	22
58 - 67	25	10
68 - 103	28	36
104 - 111	30	8
112 – 123	40	12
123 - 134	50	10

Charge-collection time

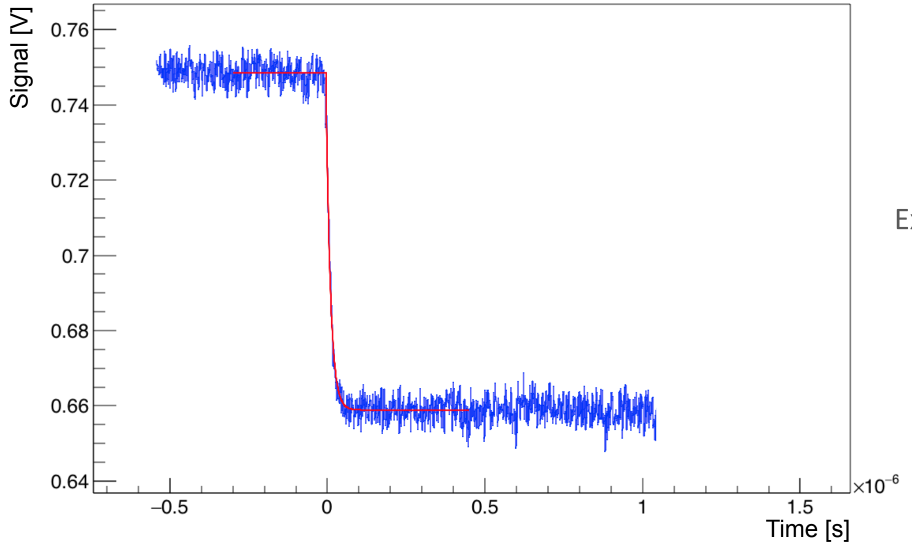
3. Future developments

- Precise charge-collection time measurements performed using differential probe and fast scope on single pixel

- Fit of waveforms with function:

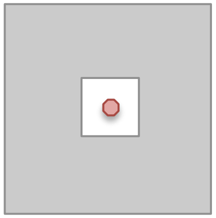
$$t \le t_0 \qquad f = a + m \cdot (t - t_0)$$

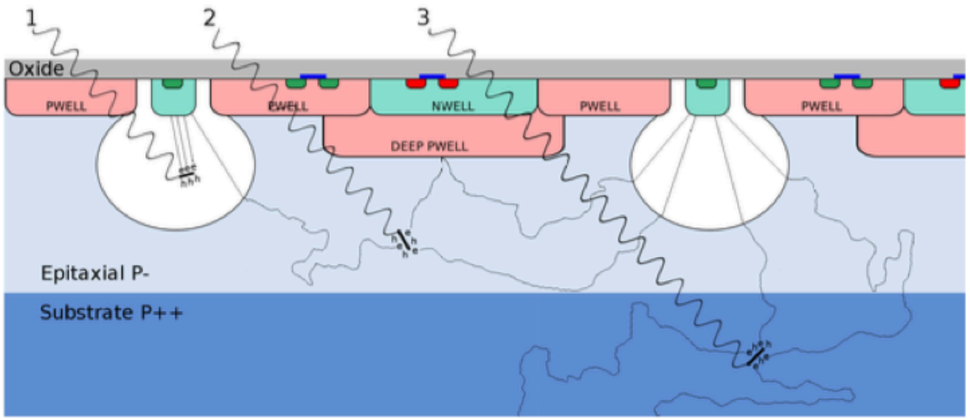
$$t > t_0 \qquad f = a + m \cdot (t - t_0) - b \cdot (e^{-\frac{t-t_0}{\tau}} - 1)$$



Example waveform and fit

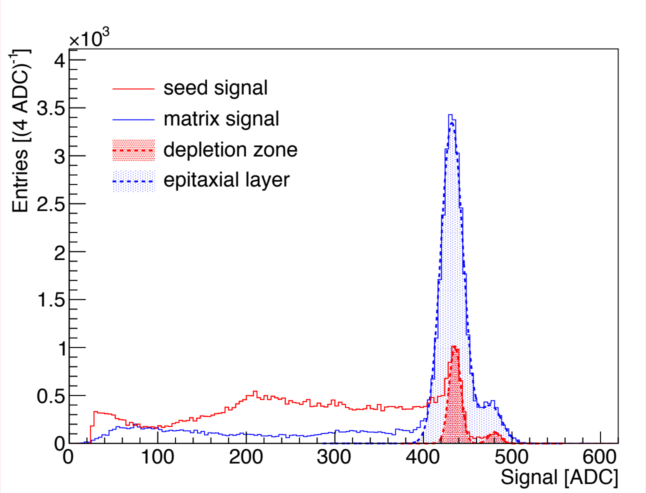
- ALPIDE-like pixel studied: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi
- Measurements performed with ^{55}Fe

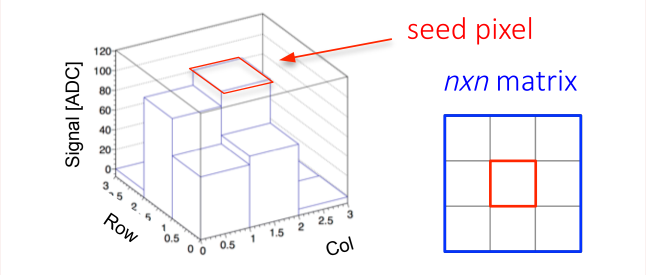




^{55}Fe: two X-Ray emission modes:

1. K-α: 5.9keV (1640e/h in Si), relative frequency: 89.5%
   attenuation length in Si: 29µm
2. K-β: 6.5keV (1800e/h in Si), relative frequency: 10.5%
   attenuation length in Si: 37µm





For X-Ray absorption in sensor fabricated with the std process three cases can be defined:

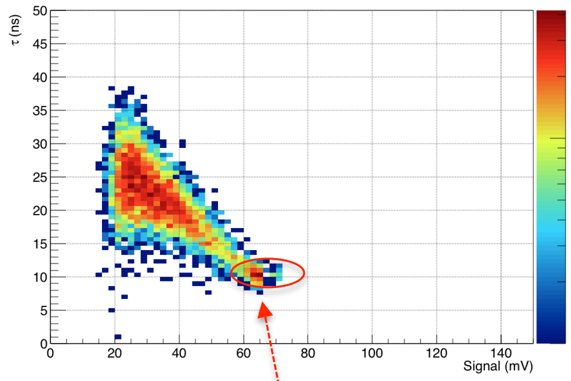
1. Absorption in depletion volume: charge collected by drift, no charge sharing, single pixel clusters
   - Events of this case populate the calibration (K-α) peak in signal histogram
   - Charge collection time expected to be ≈ 1ns
2. Absorption in epitaxial layer: charge partially collected by diffusion and then drift, charge sharing between pixels depending on position of X-Ray absorption
   - Charge collection time expected to be dependent on distance of the X-Ray absorption from a depletion volume, and longer than for events of case 1
3. Absorption in substrate:
   - contribution depending on depth of X-Ray absorption position within substrate, and charge carrier lifetime within substrate

Charge-collection time - Standard process

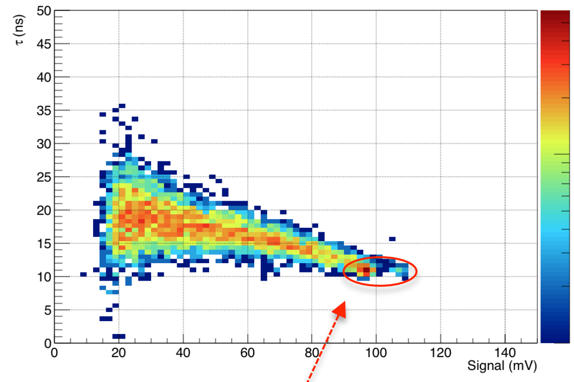
3. Future developments

MM75: 28µm pitch, 2um n-well diameter, 3µm spacing, 25µm epi

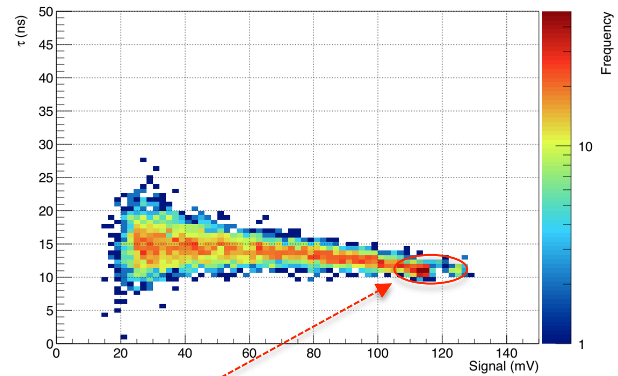
V_{BB} = -1V



V_{BB} = -3V



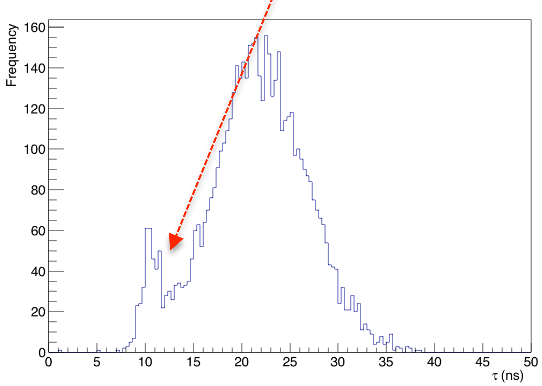
V_{BB} = -6V

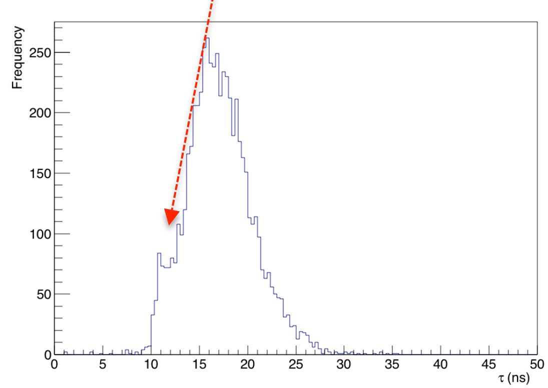


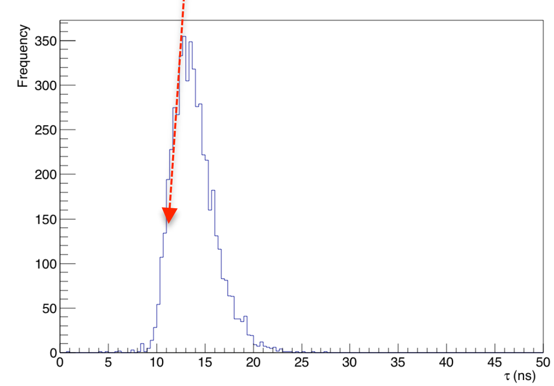
Calibration (drift) peak: no charge sharing, signal collected by drift (in <= 1ns)

- Rise time about equal for all all values of $V_{BB,}$ moreover about equal to buffer rise time
- Drift peak clearly visible in low-V_{BB} rise time histograms, for larger V_{BB} it overlaps with diffusion-drift peak

Rise time (τ):





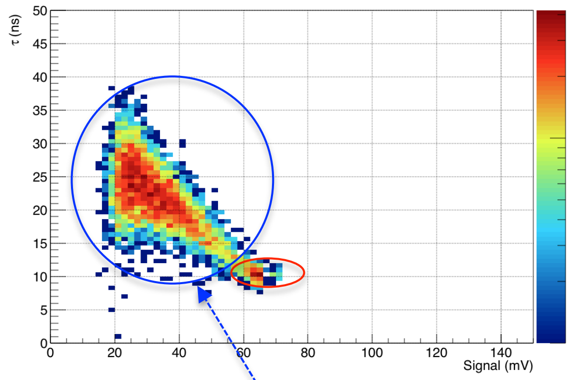


Charge-collection time - Standard process

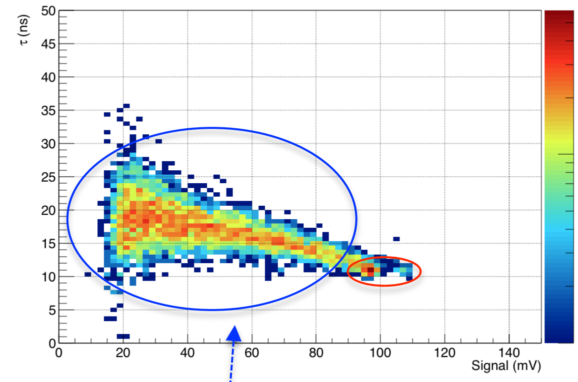
3. Future developments

MM75: 28μm pitch, 2um n-well diameter, 3μm spacing, 25μm epi

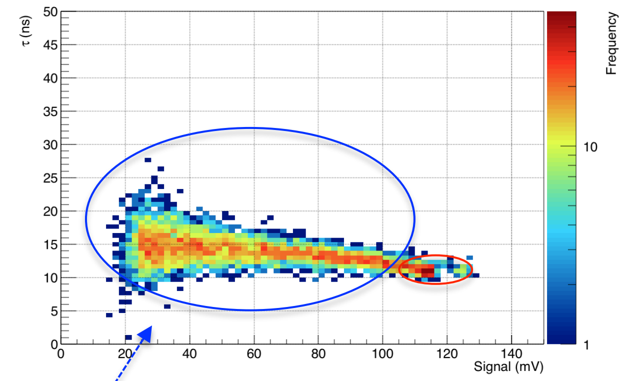
V_{BB} = -1V



V_{BB} = -3V



V_{BB} = -6V



Charge sharing – signal collected partly by diffusion and then drift

- Larger rise times with decreasing signal clearly visible in low-V_{BB} measurements
- Less clear in high-V_{BB} measurements (larger depletion volumes)

Rise time (τ):