First beam test of a monolithic matrix of the H35Demo chip

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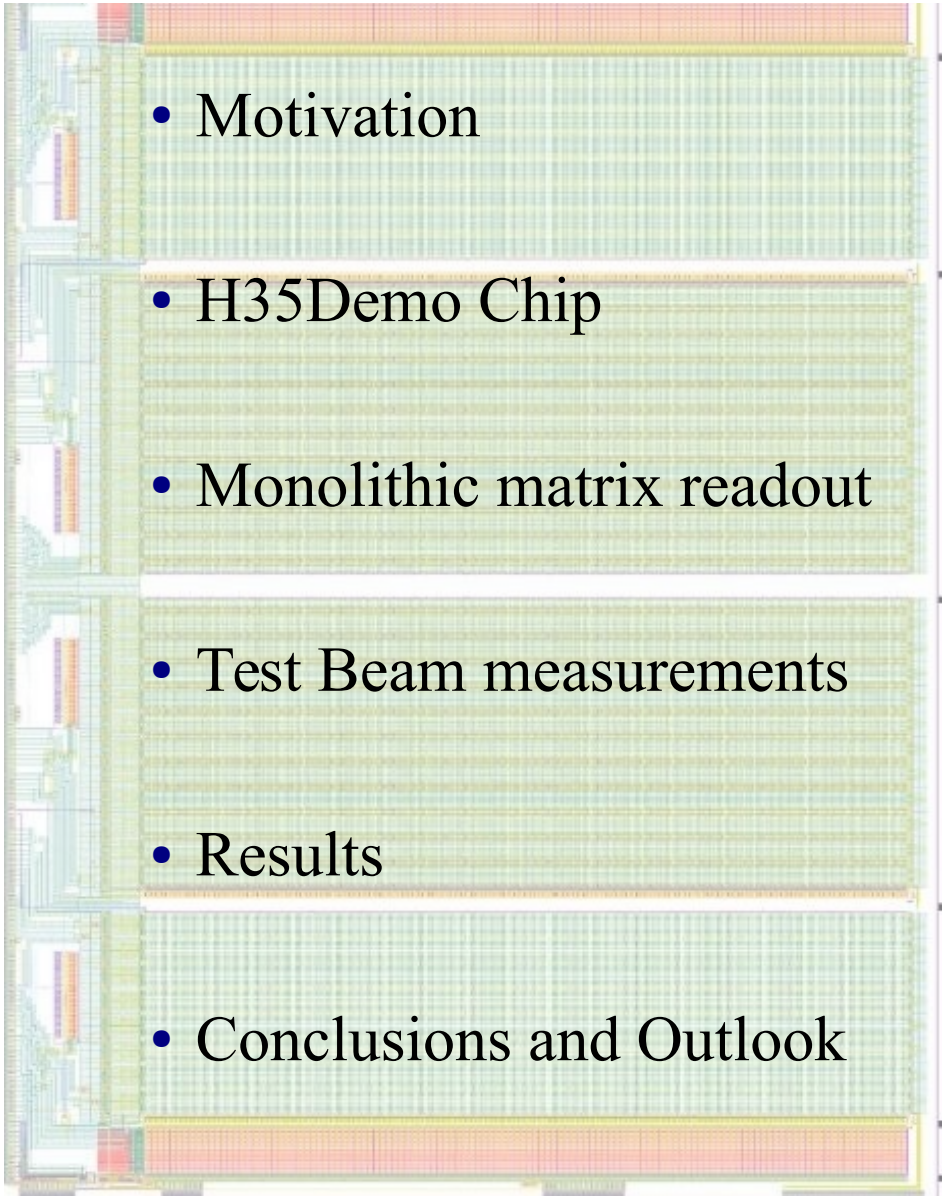
5th Beam Telescopes and Test Beams Workshop
24-27 January 2017

Outline



- Motivation
- H35Demo Chip
- Monolithic matrix readout
- Test Beam measurements
- Results
- Conclusions and Outlook

Motivation

Depleted CMOS for the ATLAS upgrade

LHC upgrade to High Luminosity LHC scheduled for beginning 2024
Plan to increase the luminosity by an order of magnitude up to 10^{35} $cm^{-2}s^{-1}$

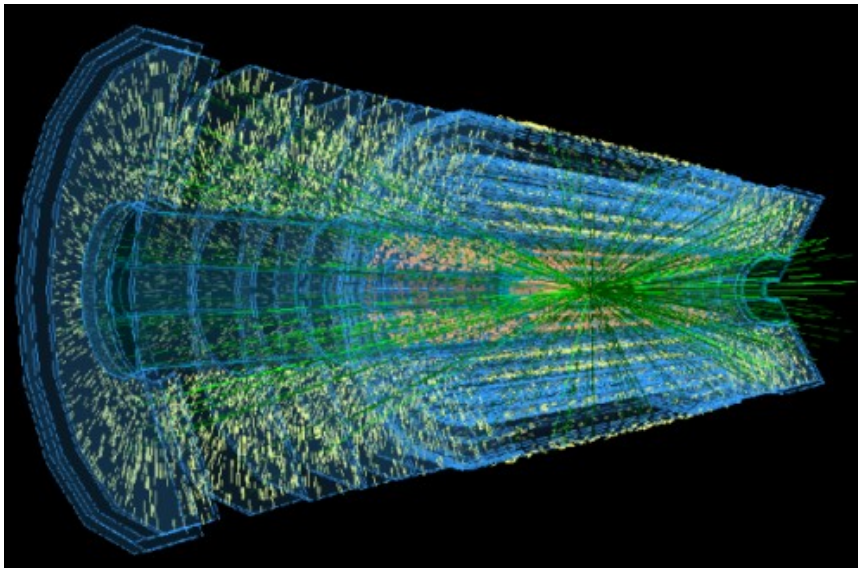
Detector challenges:
particle multiplicity - pileup rejection
radiation hardness

ATLAS ITk - tracker upgrade for HL-LHC

- 5 layers Pixel detector
- 4 layers Strip detector

A total area of **~10 m^2 of pixel detectors** will be installed

The **innermost pixel layer** will be required
to stand up to a fluence of **$2 \cdot 10^{16}$ n_{eq}/cm^2**
the **outermost layer ~ 10^{15} n_{eq}/cm^2**



Sketch of an event in ATLAS at HL-LHC

Depleted CMOS technologies being investigated in ATLAS as an option for the HL-LHC upgrade

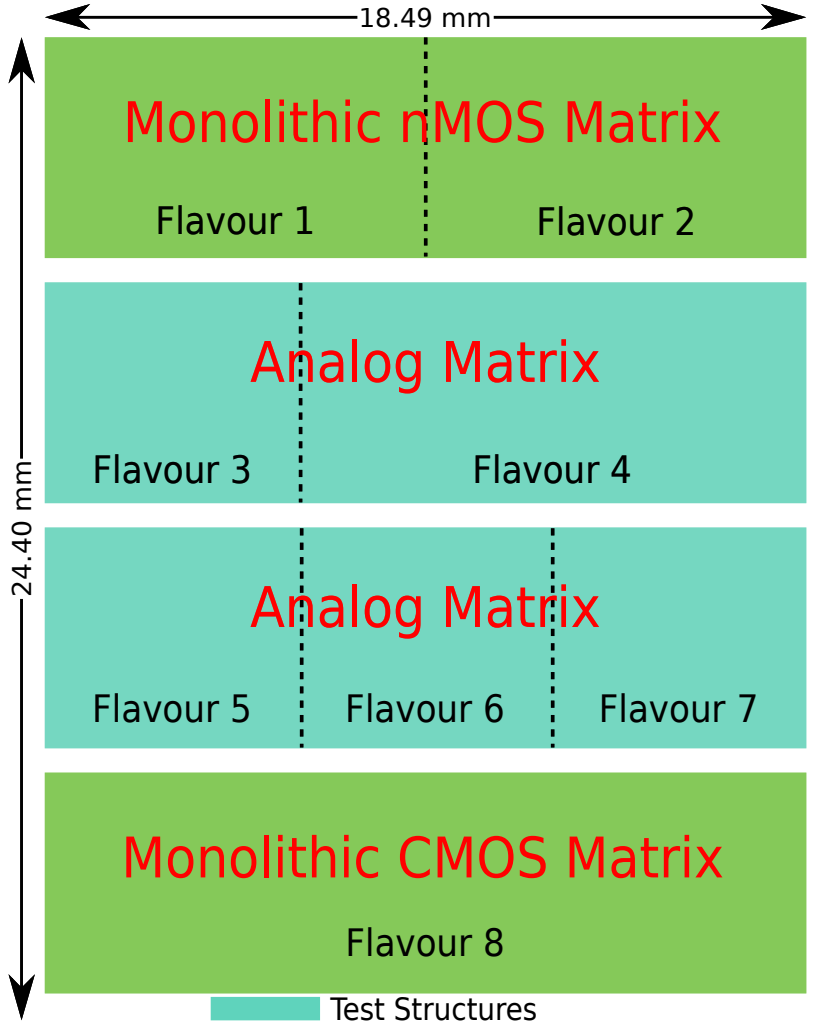
ATLAS groups are investigating the performances of:

- Devices from different foundries
- Different approaches:
  CC coupled – monolithic

H35Demo Chip

A large area demonstrator chip in the AMS 0.35µm HV-CMOS technology produced on wafers of different resistivity 20 Ωcm (standard), 80 Ωcm, **200 Ωcm**, 1 kΩcm

Designed by KIT, IFAE and University of Liverpool



Eight different pixel matrix flavors:

- Monolithic **nMOS** matrix
  - Digital pixels with in pixel nMOS comparator
  - Two flavors: w/ Time Walk compensation and w/o TW compensation
- **Analog** matrix (2 arrays)
  - Different flavors in terms of gain and speed
  - To be capacitative coupled to FE-I4 readout chips
- Monolithic **CMOS** matrix
  - Analog pixels with off pixel CMOS comparator
  - In the readout cells:
  - - 1 discriminator for the left half
  - - 2 discriminators for the right half

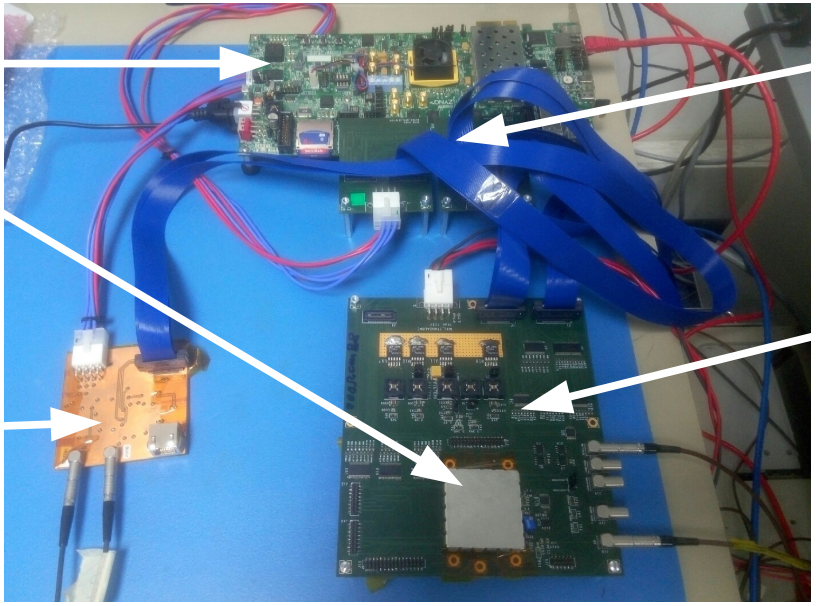
Monolithic matrix readout

Readout of the monolithic matrices developed at IFAE, both hardware and software
Still work in progress at the time of the beam test, not all the features implemented

Xilinx ZC706 FPGA board

H35Demo chip
- Both CMOS and nMOS matrices wirebonded

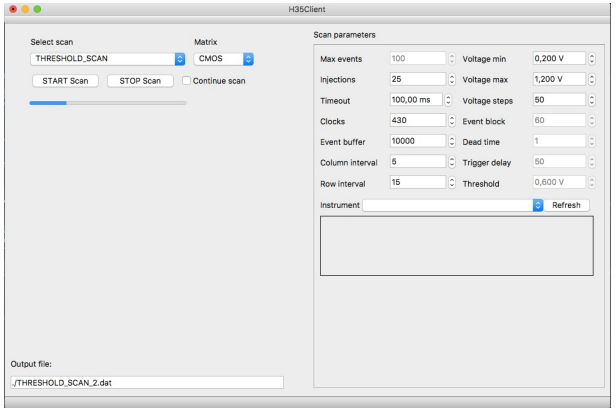
Trigger board
- Trigger in
- Busy out



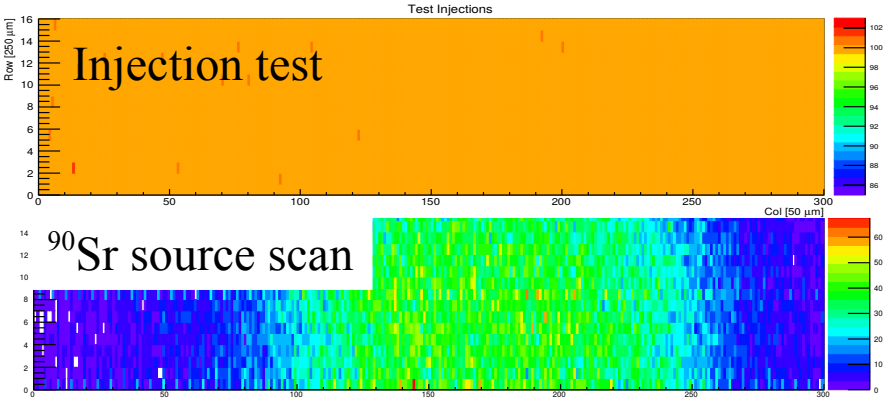
PCB adapters
1x H35 PCB
1x test signal
1x Trigger PCB

H35Demo PCB
- Low voltage regulators
- Sensor bias
- Test pulse input
- Analog signal output

Steering software



First laboratory results



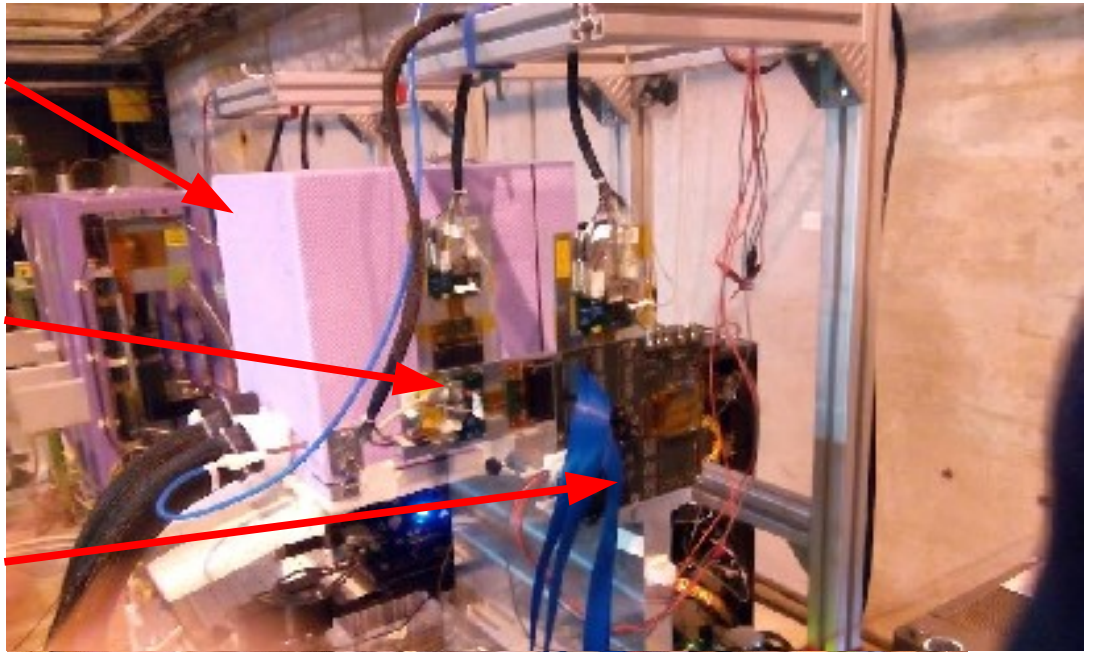
Test beam at CERN SpS

First beam test of the H35Demo monolithic CMOS matrix in November 2016
Collaboration between UniGe (Telescope support) and IFAE (data taking and data analysis)

UniGe Cooling box
- H35Demo CC to FEI4

UniGe Telescope
- 6 x FEI4 planes
- 2 planes rotated 90º
- RCE readout

IFAE H35Demo PCB
- CMOS matrix aligned to the beam



Integration with the Geneva FEI4 telescope (Trigger – busy scheme)

- Triggers from the telescope reach the Xilinx FPGA board
- Busy signal from the FPGA is risen to stop the DAQ until H35 is ready again
- Events are written separately and sequentially by each DAQ system
- System running at 25 ns with ~2 kHz trigger rate

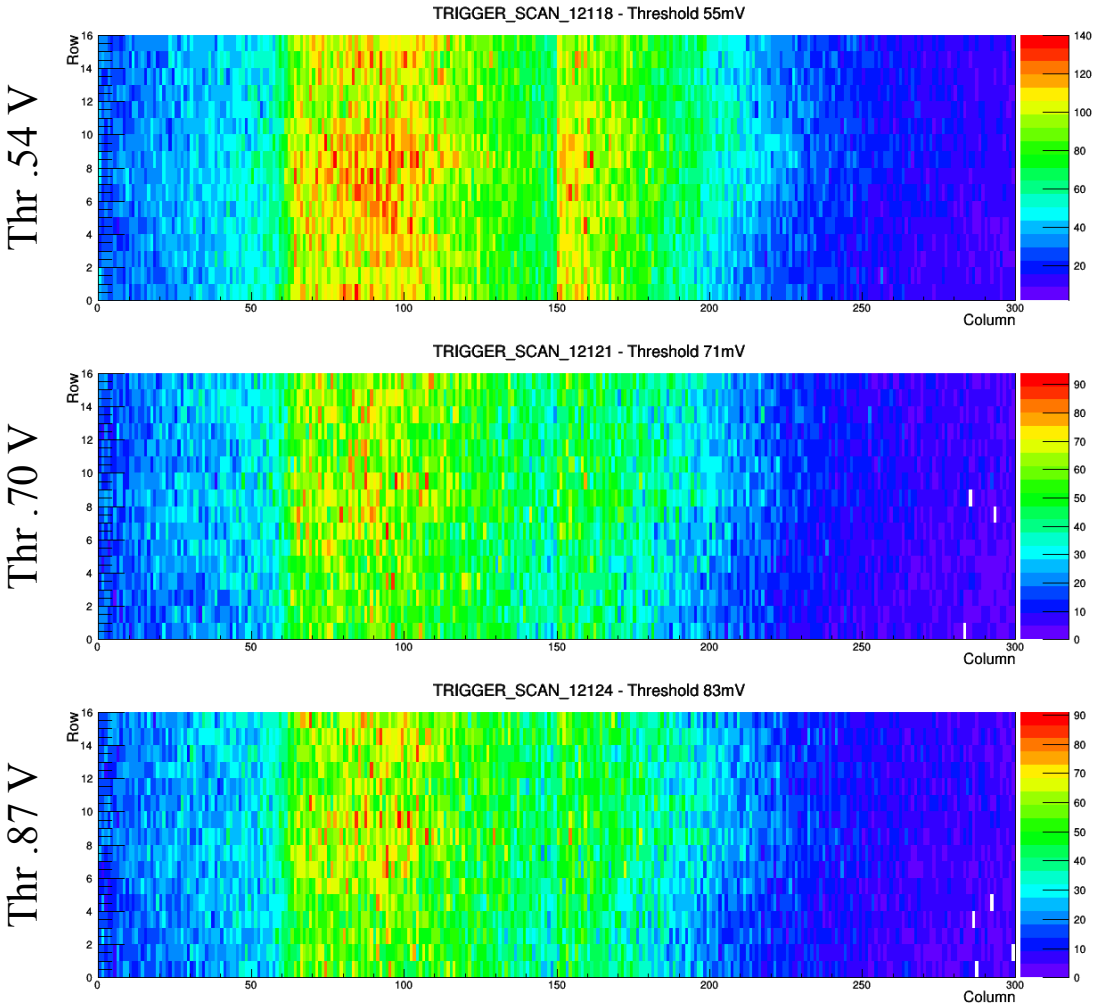
'On-line' data analysis

Measurements set:

3 different **bias voltages**
→ 50 V – 100V – 120V

3 different **thresholds**
→ 0.54 V – 0.70 V – 0.87 V

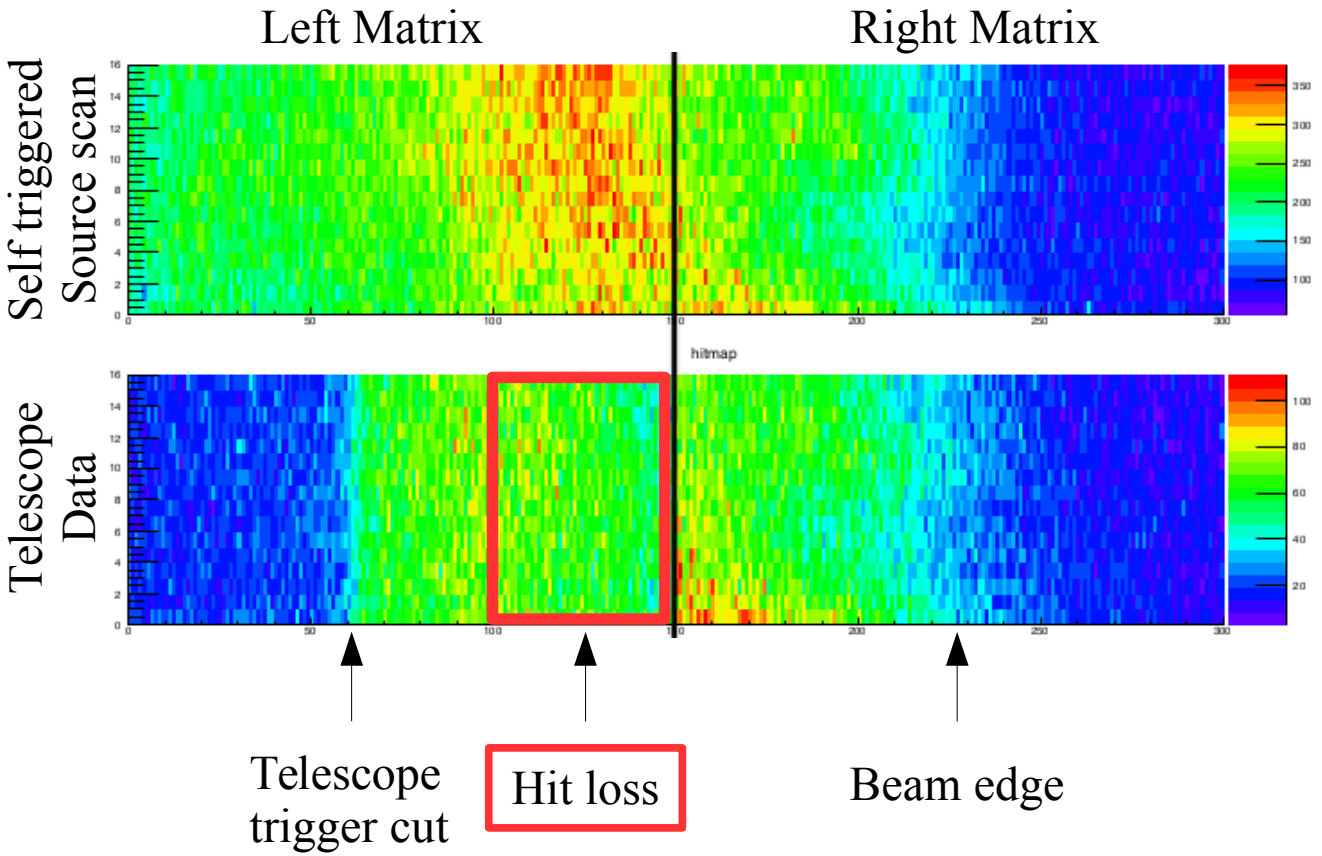
Hit maps not compatible with the beam shape
→ Region of low occupancy in the center of the matrix



V_{bias} = 120V

'On-line' data analysis

External trigger and self trigger give two different hit maps:



The beam spot structure is clearly visible with self triggered scans

A region with lost hits is present in when the readout is triggered with an external trigger

- Same pixel flavor in left and right matrix
- Different readout lines
  - Different timing properties

→ Hits out of time are lost

Synchronization

The Telescope – DUT events synchronization is based on a Trigger – Busy scheme:

- FEI4 telescope trigger fires
- Trigger signal is sent to the telescope DAQ and to the H35 FPGA
- H35 FPGA rises a busy signal
  - FEI4 telescope cannot send trigger while the Busy signal is up
  - Busy pulled down when the H35Demo DAQ ready to receive a new Trigger

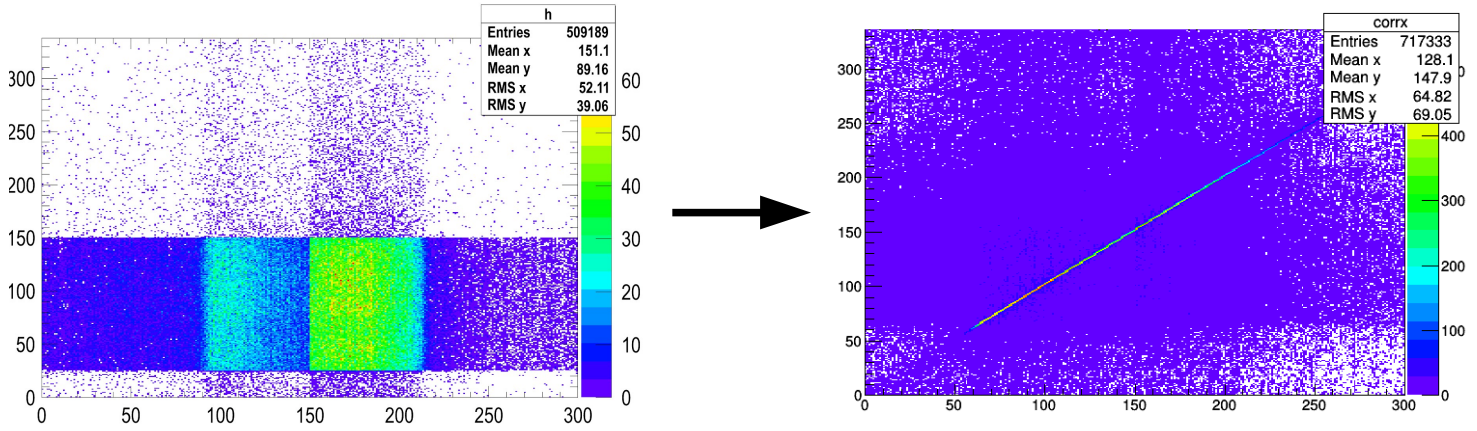
Problem:

The H35Demo FPGA sometimes did not react to a Trigger → Events de-synchronization

Off-line solution:

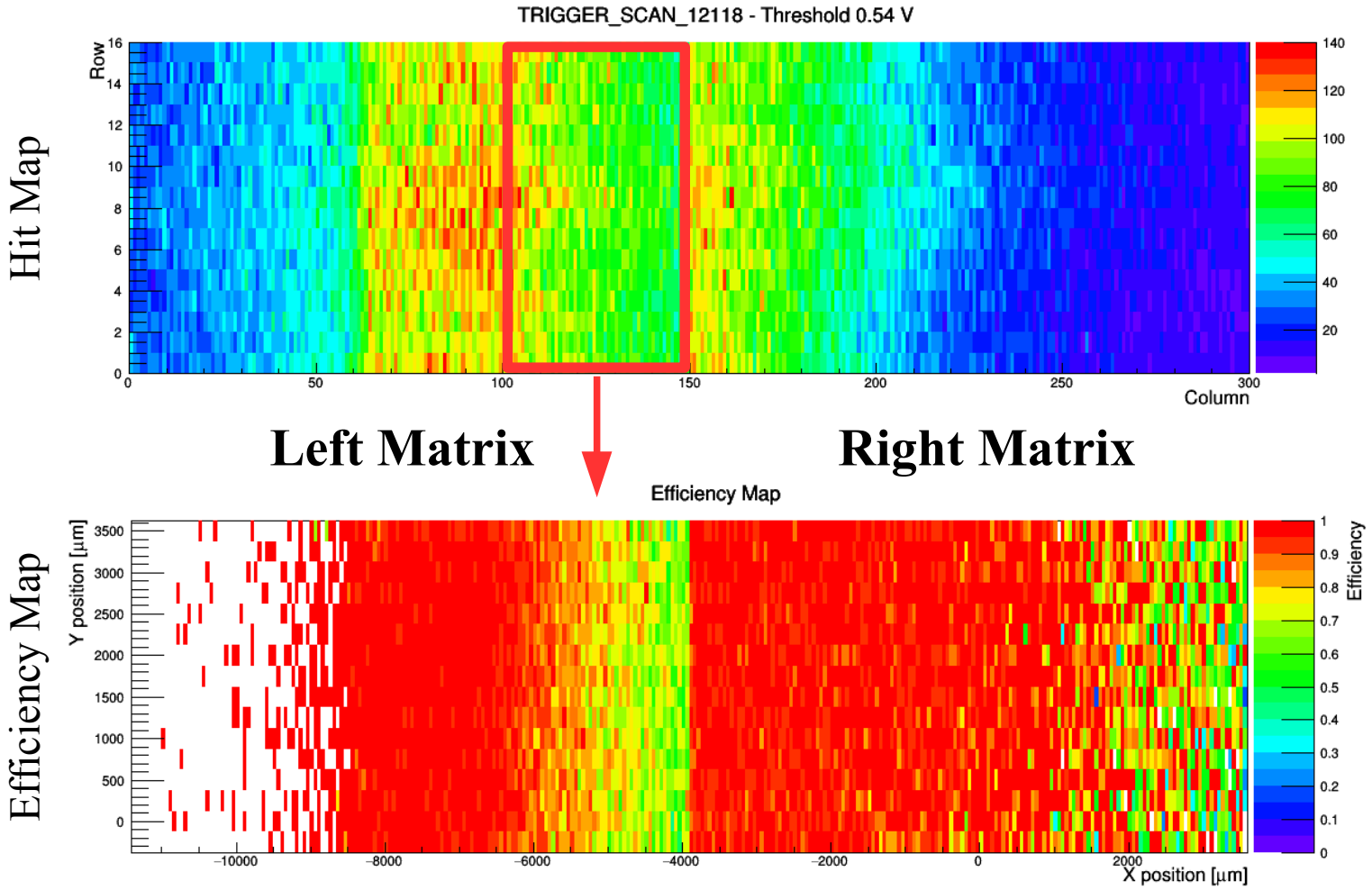
Both the FEI4 Telescope and the H35Demo DAQs have a trigger time-stamp

- The time-stamp is not the same in the two systems
- The time difference between consecutive triggers is ~ the same (not shared clock)
- Triggers seen by both DAQs are re-synchronized
- Most of the runs re-synchronized and analyzed



Efficiency

The area with lost hits of the hit map converts into an area of lower efficiency

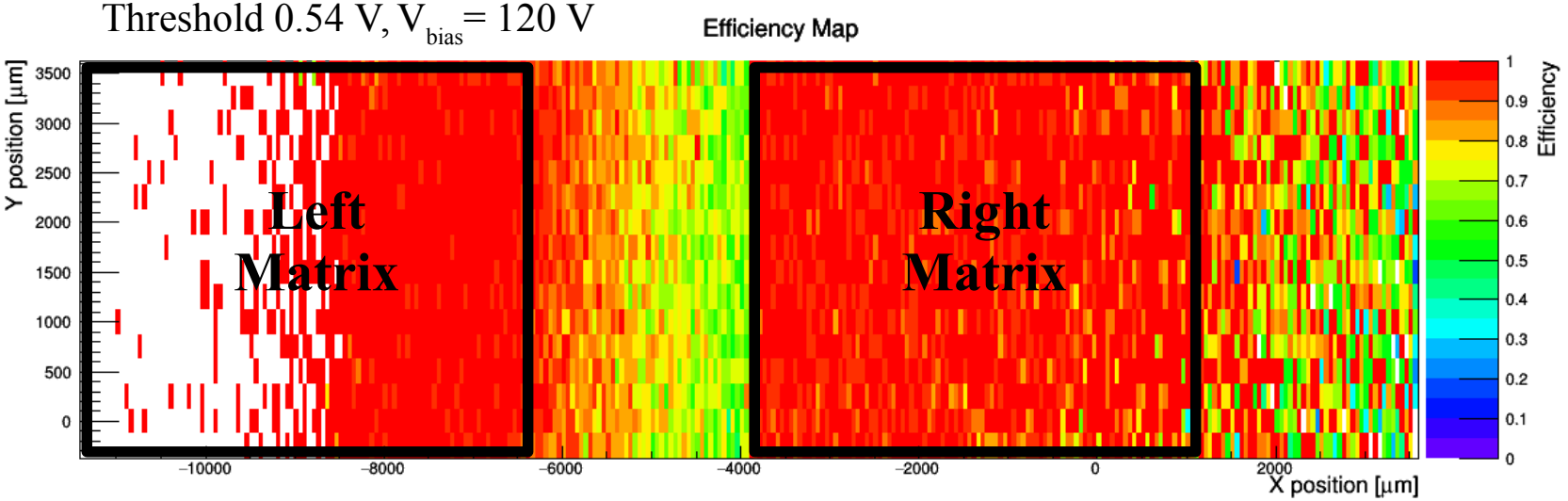


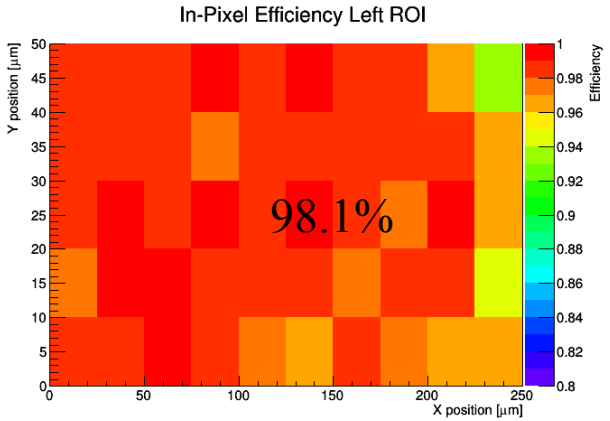
The efficiency map shows a region of lower efficiency also on the right matrix but the low statistics do not allow to make strong conclusions

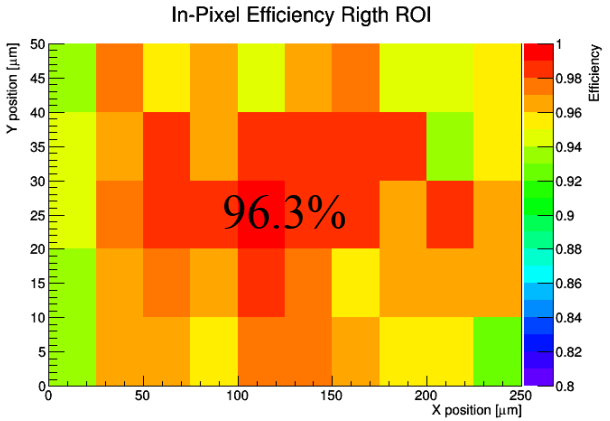
Efficiency

Track reconstruction and data analysis performed with Judith software
Two regions of interest are selected for the right and left matrices excluding the columns with lost hits

Threshold 0.54 V, V_{bias} = 120 V







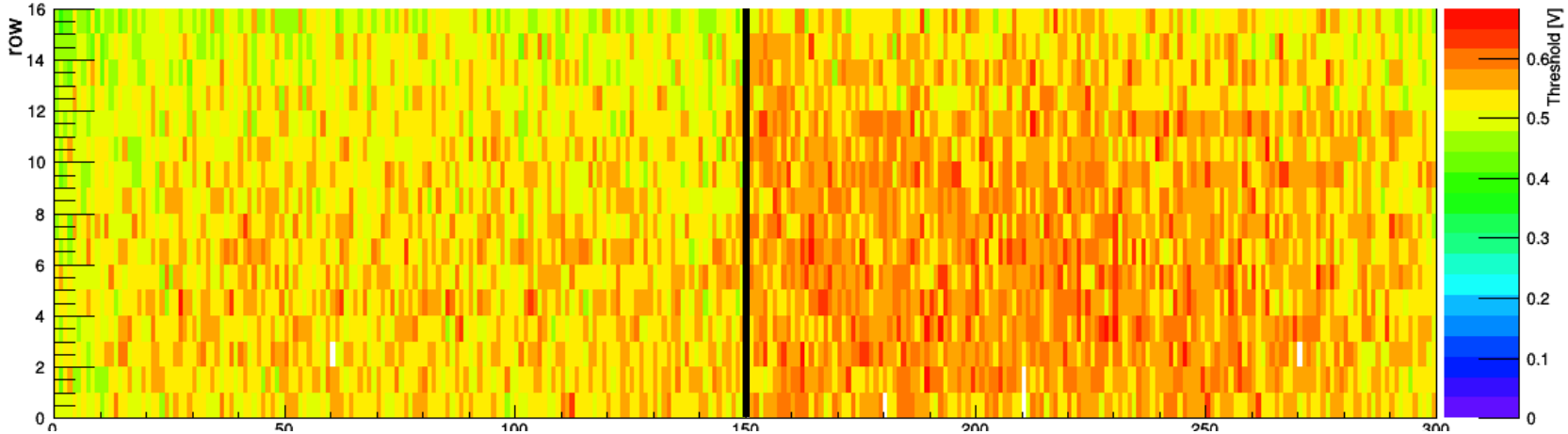
The Left matrix has a systematically higher efficiency than the Right one

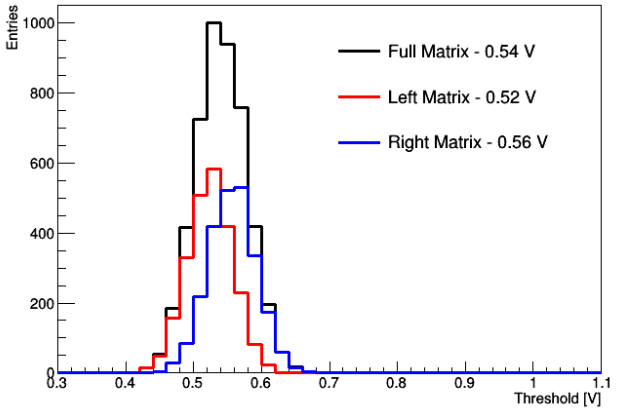
Threshold distribution

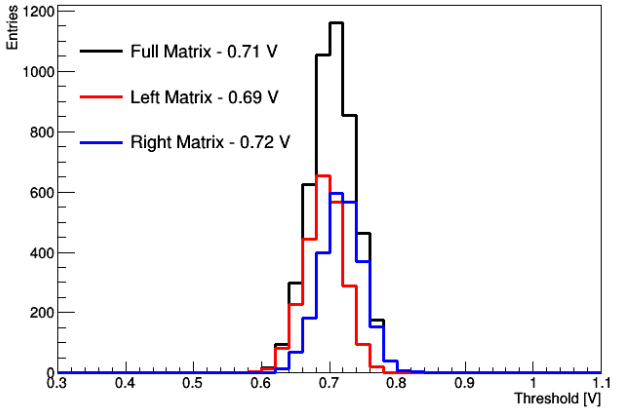
Pixel tuning was not yet implemented in the monolithic read-out system

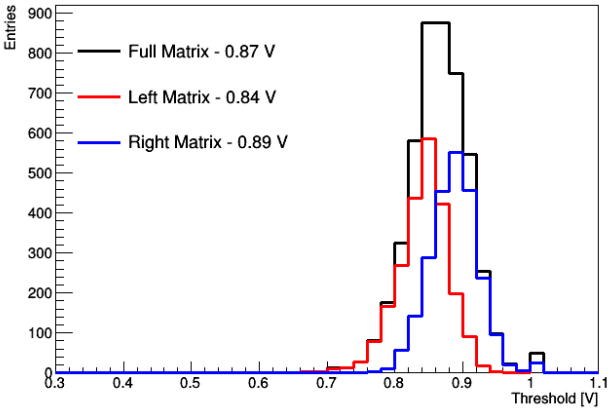
- Only global value is set for the threshold

Threshold map at a threshold = 0.54 V





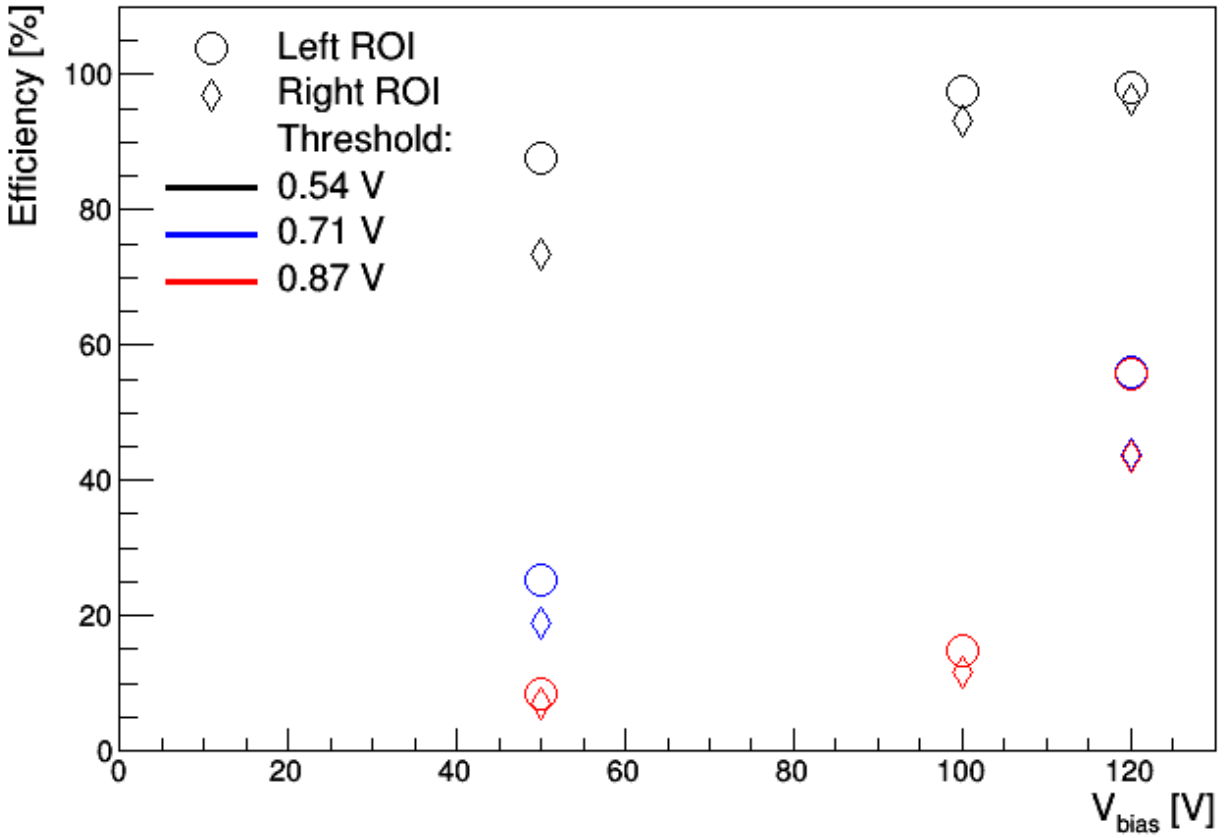




The average threshold of the right matrix is larger than the one on the left matrix

Efficiency

- Left matrix always more efficient than the right one
- L/R threshold asymmetry affects efficiency considerably
  → up to ~10%
- Efficiency larger than 96% at 120V and Thr = 0.54V
  → 98% for the Left matrix



Conclusions

- The first beam test of a monolithic matrix of the H35Demo chip performed integrating the IFAE readout system with the UniGe FE-I4 telescope
- Data synchronization to the telescope achieved
- Good efficiency at the very first test of the H35Demo chip
  - Efficiency up to 98% in the ROIs

Outlook

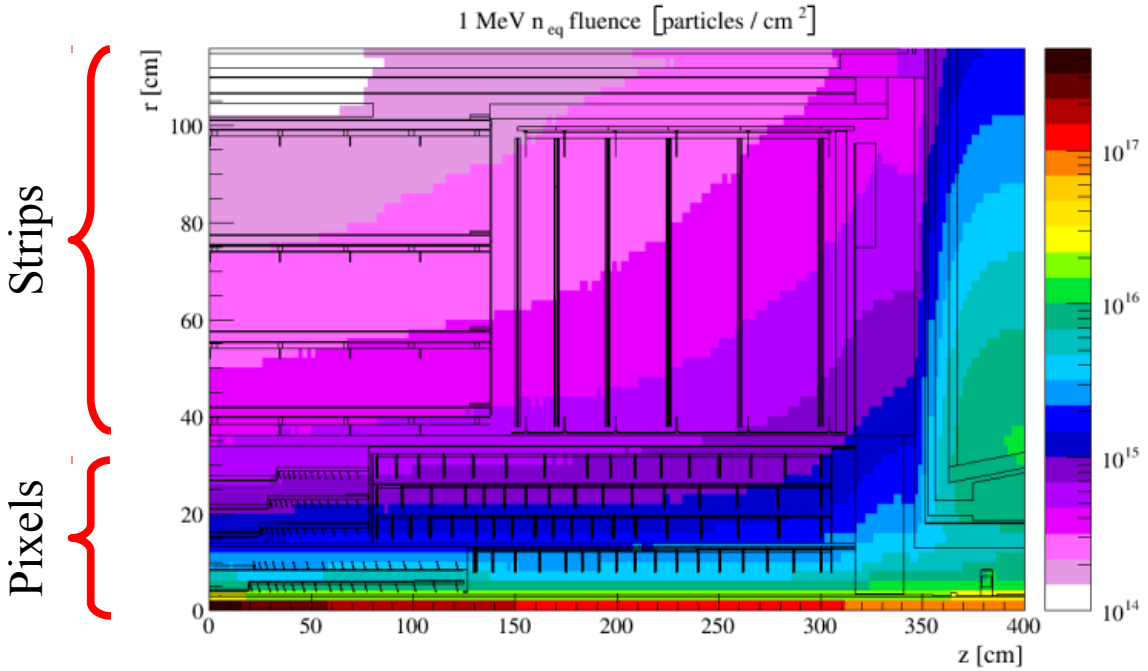
- Update the H35 readout
  - Lost trigger → Solved
  - Pixel tuning → To be implemented
  - Timing behavior → Under investigation
- Go back to test beam soon

Thanks

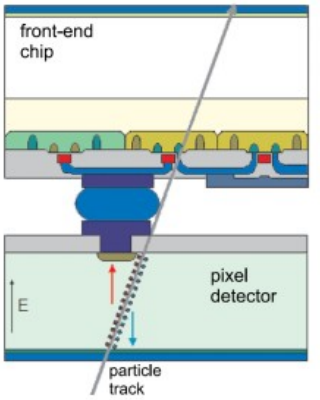
Backup

Backup

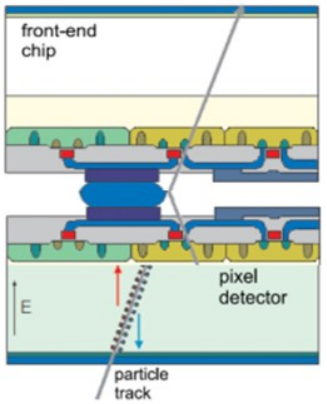
Requirements for inner and outer layers of the ATLAS ITK differ by orders of magnitude in terms of radiation tolerance, occupancy, ...



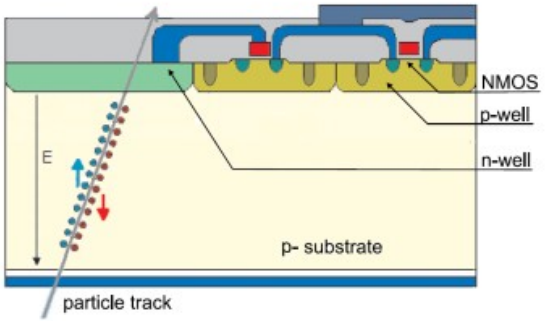
Different options:



Hybrid



Capacitive coupled (CCPD)



Monolithic

Possible solution:

Hybrid solution for the **inner layers**

CMOS monolithic or CCPD for the **outer layers**

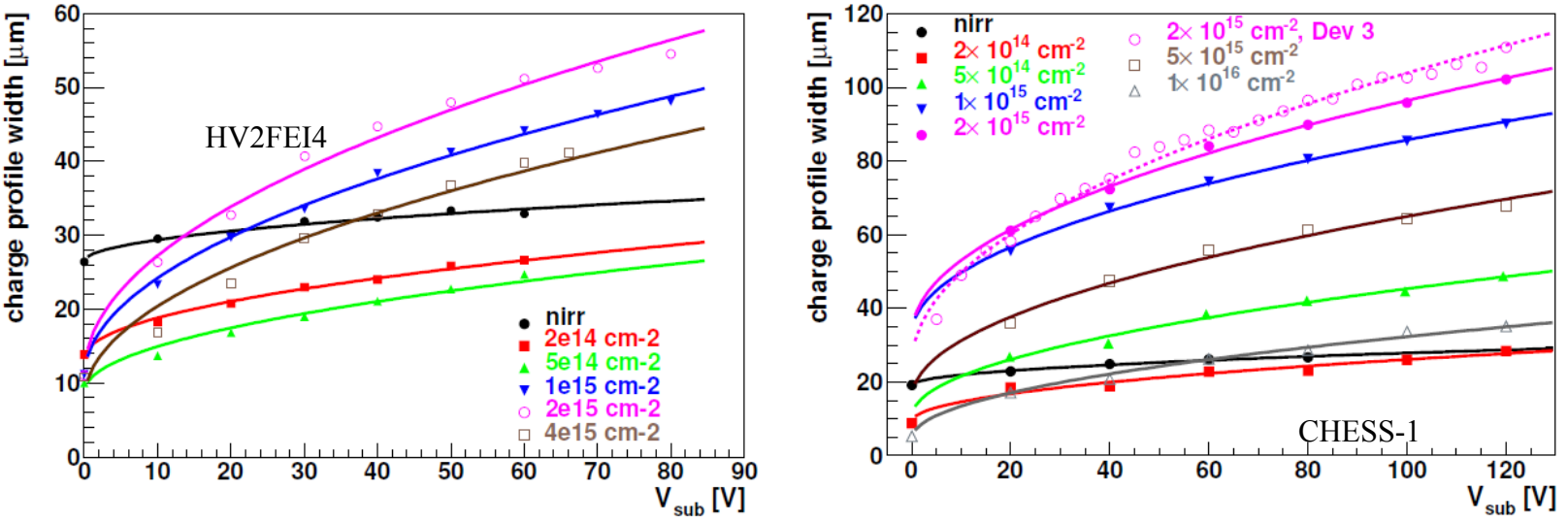
CCPD and monolithic could be more cost effective and meet radiation hardness requirements for the outer layers

HV-CMOS for HEP

Several productions from different foundries have been made
Each with its production technology and wafer resistivity:

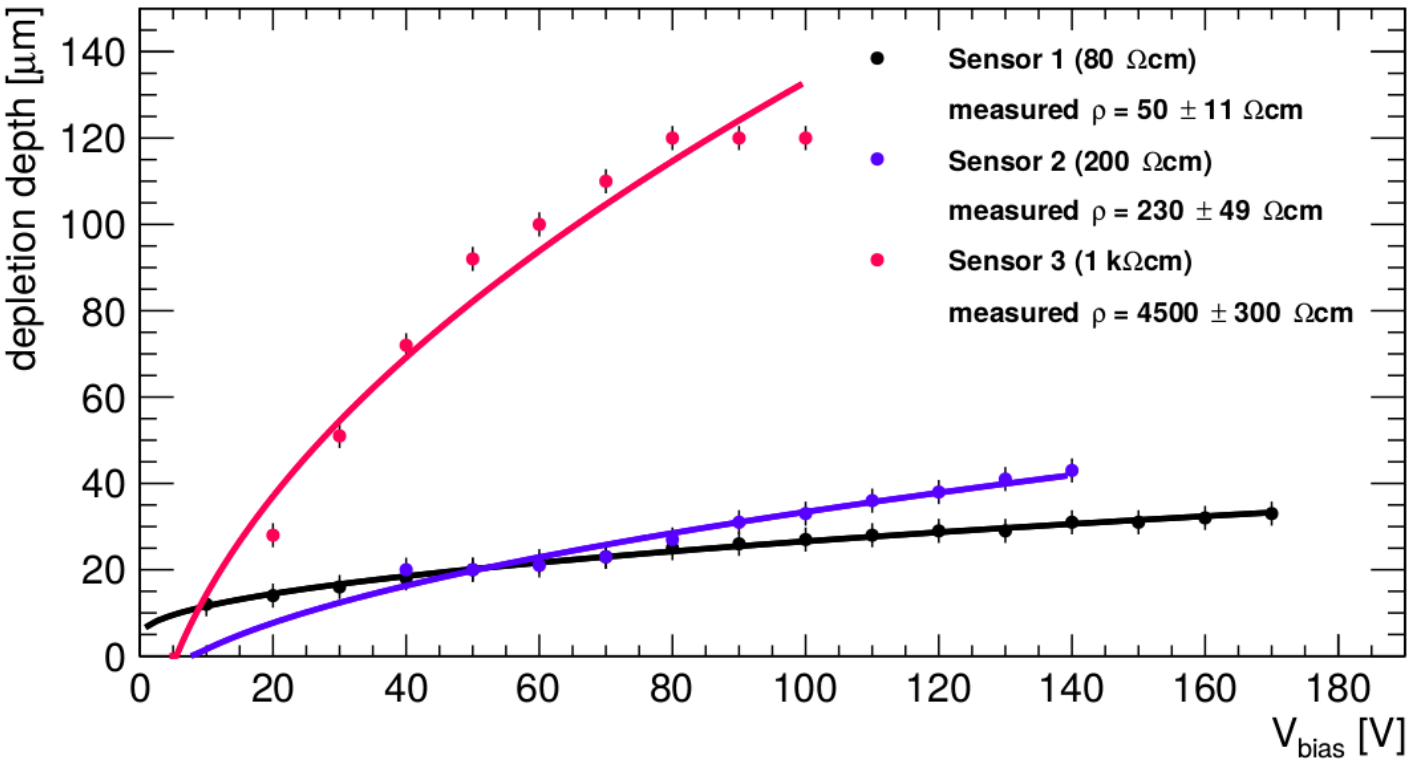
- AMS 350nm, ρ = 20Ω·cm (CHESS-1)
- AMS 180nm, ρ = 10Ω·cm (HV2FEI4)
- LFoundry 150nm, ρ = 2kΩ·cm
- X-FAB 180 nm, ρ = 100Ω·cm

Interesting results have been obtained but it is hard to compare devices from different foundries because of different technologies, substrate doping and well properties



G Kramberger, 27th RD50 Workshop

Depletion depth



Depletion depth measured with edge-TCT on a scanning TCT set-up

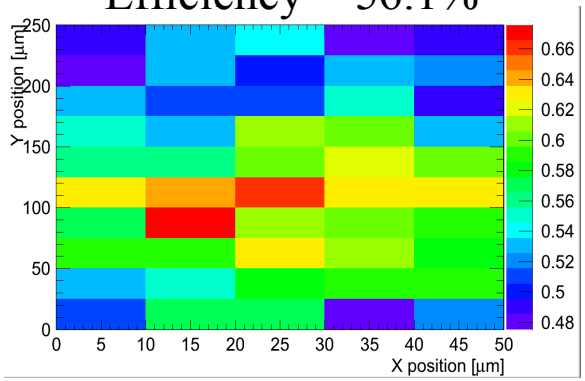
In-pixel efficiency

Threshold dependence

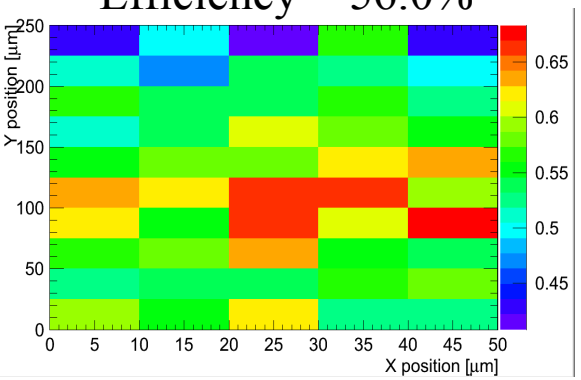
Threshold = 0.87 V | **Threshold = 0.71 V** | **Threshold = 0.54 V**

Left

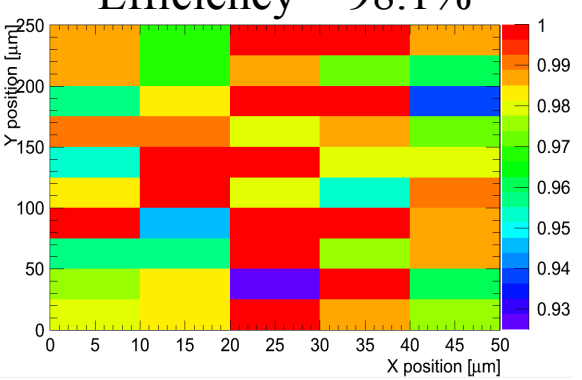
Efficiency = 56.1%



Efficiency = 56.0%

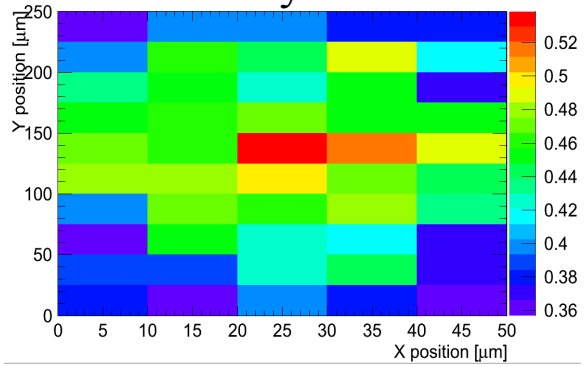


Efficiency = 98.1%

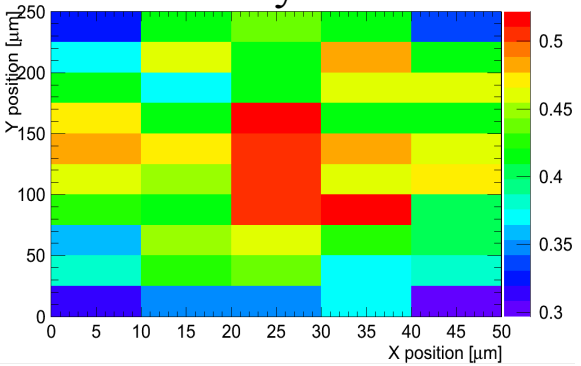


Right

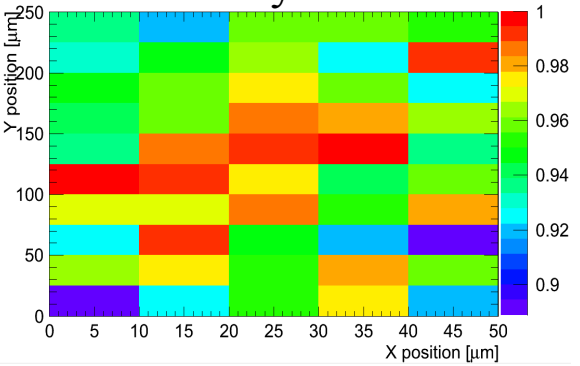
Efficiency = 42.9%



Efficiency = 42.3%



Efficiency = 96.3%



V_{bias} = -120 V

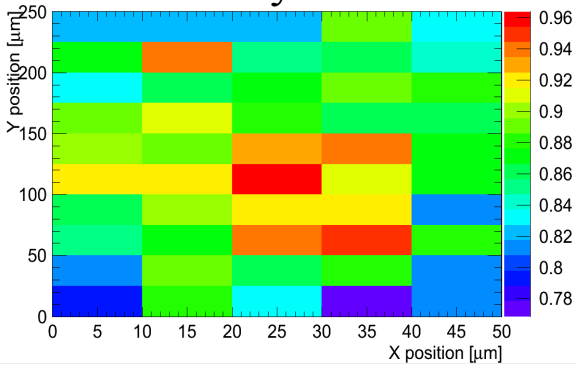
In-pixel efficiency

Bias voltage dependence

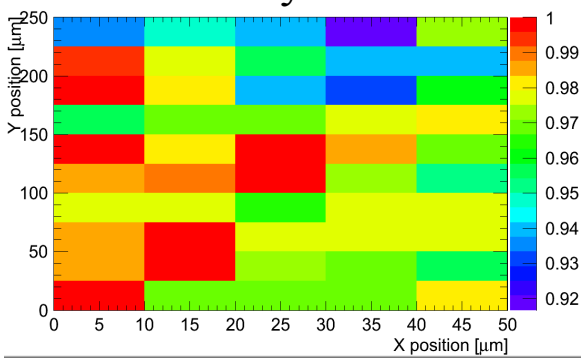
V_{bias} = 50 V **V_{bias} = 100 V** **V_{bias} = 120 V**

Left

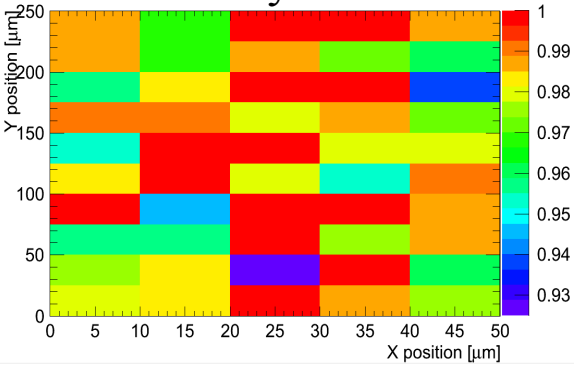
Efficiency = 87.1%



Efficiency = 97.2%

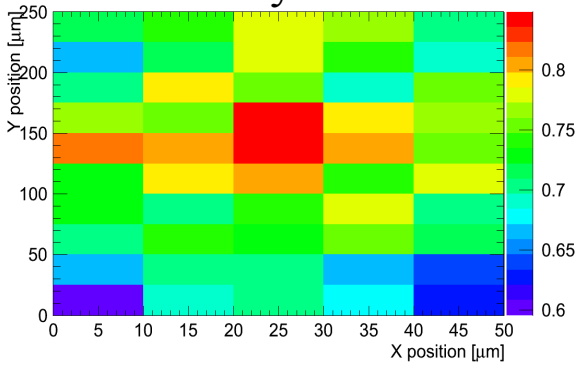


Efficiency = 98.1%

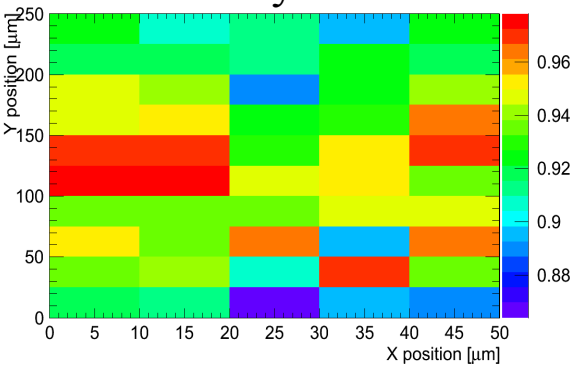


Right

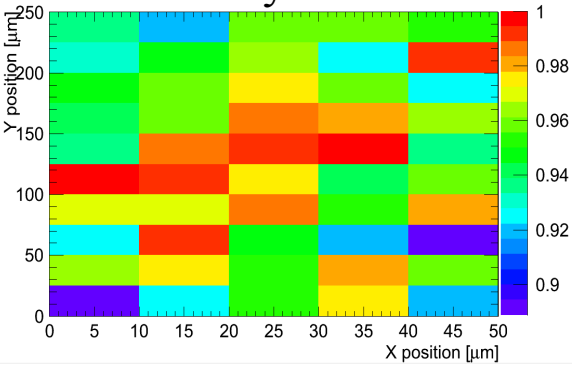
Efficiency = 73.5%



Efficiency = 93.4%



Efficiency = 96.3%



Threshold = 0.54 V