CHESS2 Digital Test Boards

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Digital Test Daughter Boards

- First panel of 10 PCBs at SLAC
- Preparing vendor wire bonding. 200+ bonds and not so regular pad patterns
- Somewhat trickier layout (10 layers) and more expensive than original expectation due to many fine pitched wire bond pads.

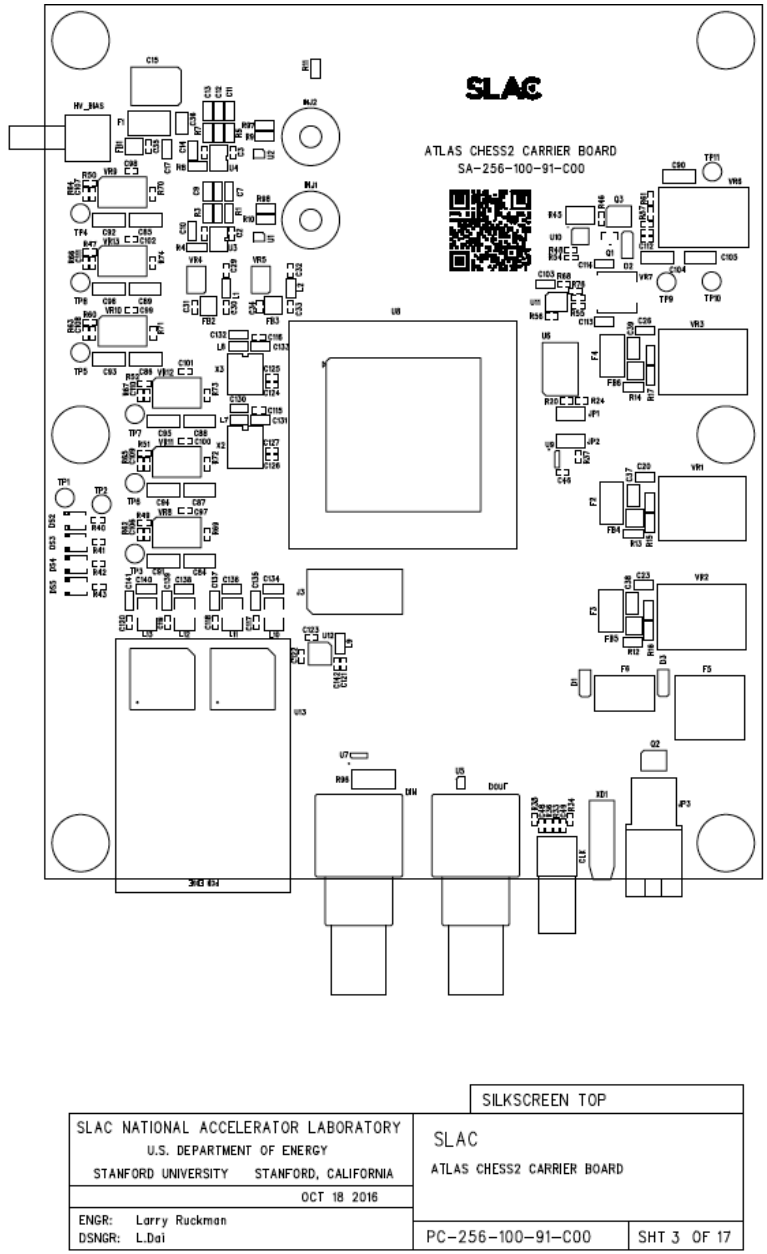
Design details for daughter + carrier are documented at:
https://confluence.slac.stanford.edu/display/AIRTRACK/ATLAS%3A+CHESS2

What chip(s) to load ?

- SLAC received 10 chips of the types:
  2x(20,50-100,200-300)
  4x(600-2000)
- Probably will load 1 high-res chip to start with to check wire bonding procedure and any possible gross issues
- If Ok, then the rest 4 or all 9 ? Or anyone else wants to try wire bond daughter boards ?

Digital Carrier Board

- PO for 20 PCB in processing to go out this week and back in one week.
- More “conventional” 10-layer digital PCB.
- Initial version of firmware exists.
- Software interface and backend HSIO2 code starting (Martin)
- Load 5 first when PCB returns to check for gross issues.
- Small number of loaded daughter boards and carrier boards for distribution at AUW ?
- If no issues, the bulk distribution can follow within a month.
- Round-2 HSIO2 production in progress.



Bulk Assemblies

- How many daughter boards to produce ?
- Always load full chips ? Digital sections useless on analog cards so only makes sense to load 1+1 on analog cards ? The digital pair half still takes a full daughter board.
- How many analog / digital daughter boards to irradiate with what and how much does ?
- Test beams ?