RD53A pixel ASIC

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on behalf of RD53 Collaboration

Outline

- Introduction on RD53 Collaboration
- RD53A chip specifications
- Floorplan
- Analog front-end
- Analog chip bottom
- Digital architecture
- Serial powering
- Padframe
- Verifications

RD53 Collaboration

RD53 is a collaboration among **ATLAS-CMS** communities for the development of **LARGE scale Pixel chips for Atlas/CMS phase 2 upgrades**

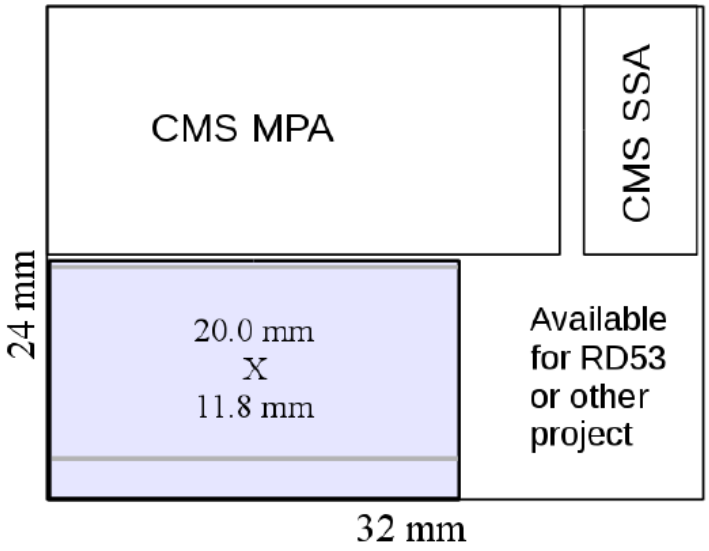
- 19 Institutions from Europe and US
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, RAL, Seville, Torino, UC Santa Cruz.

- **65 nm CMOS** is the chosen technology
- RD53 Goals:
  - Detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness
  - Development of **tools and methodology** to efficiently design large complex mixed signal chips
  - Design of a **shared rad-hard IPs library**
  - Design and characterization of **full sized pixel array chip**

RD53A

– RD53A specifications approved at the end of 2015 by ATLAS, CMS and RD53 collaborations: **http://cds.cern.ch/record/2113263**

– Fabricated on an engineering run shared with CMS MPA chip for cost sharing



– RD53A size: 20x11.8 mm^2 → 400 col. x 192 rows of 50x50 μm^2 pixels

Submission: 31 May 2017

RD53A specifications

Technology	65nm CMOS
Pixel size	50x50 um^2
Pixels	192x400 = 76800 (50% of production chip)
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	<600e-
In -time threshold	<1200e-
Noise hits	< 10^{-6}
Hit rate	< 3GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	Max 1MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤ 1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	500Mrad at -15°C
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1W/cm^2 including SLDO losses
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

RD53A additional features

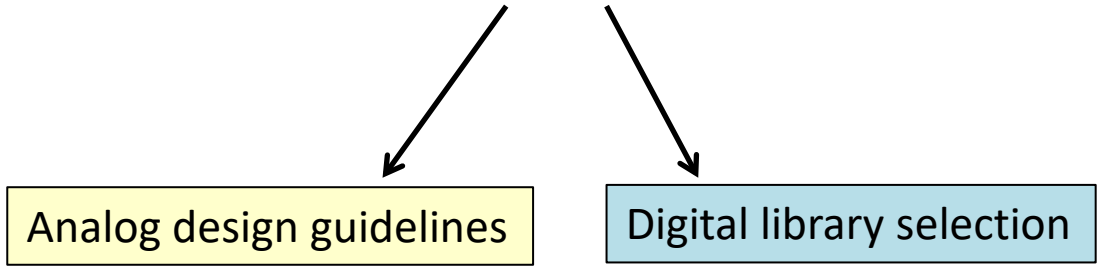
RD53A is not intended to be a production chip

- will contain design variations for testing purposes
- some additional features included **ONLY** after RD53A v1.x is fully verified and in case of time/manpower availability

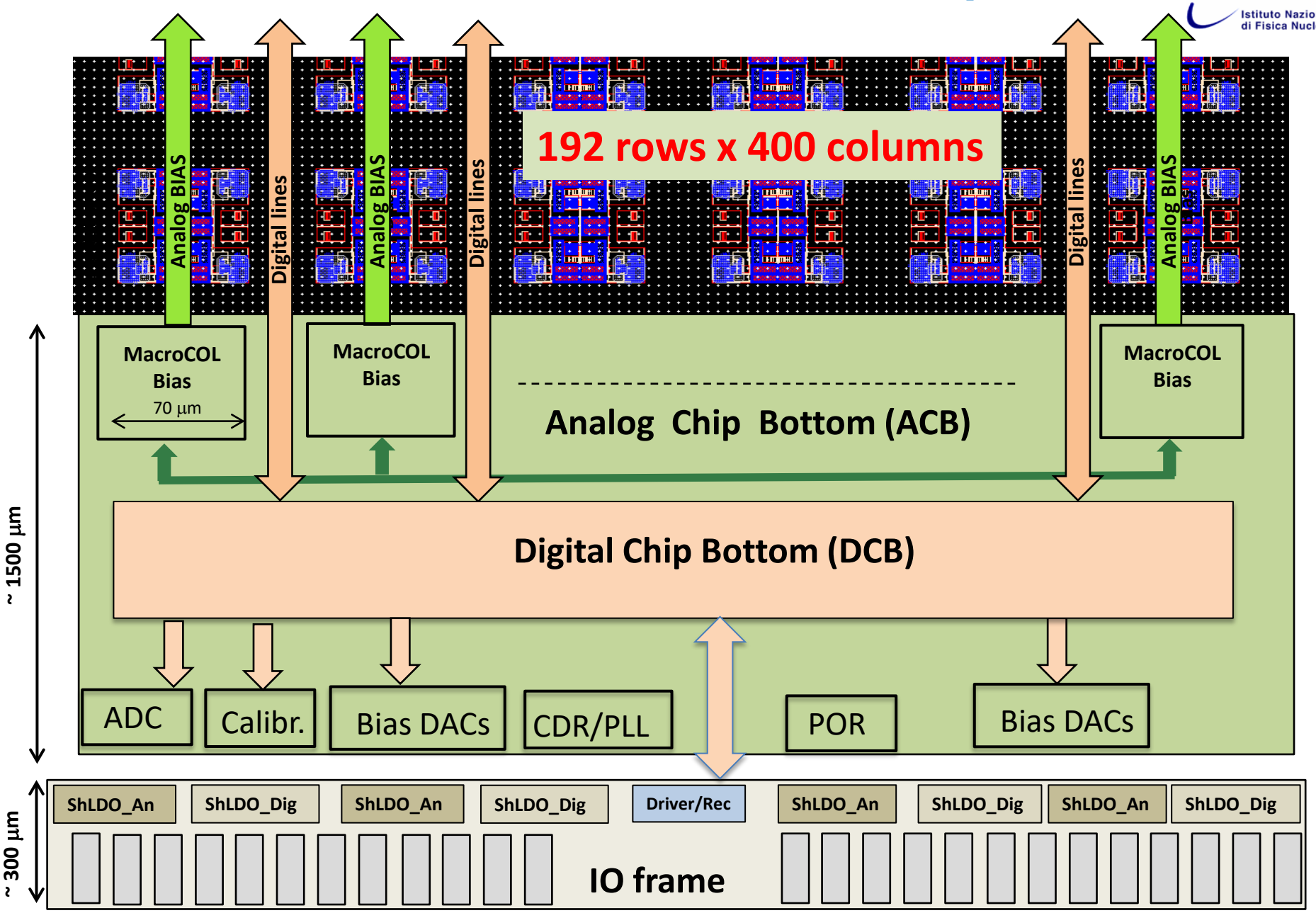
- High resolution (> 4 bit) mode /Non linear TOT encoding / 80 MHz counting
- On-chip data compression
- Data merging from several pixel chips into one link
- ….

Radiation tolerance

- RD53A should be capable to operate at least up to 500 Mrad
- Extensive irradiation campaign in past 3 years to qualify the technology
- Significant radiation damage above 100 Mrad:
  - Analog: transconductance, Vt shift
  - Digital: speed degradation
- 200 Mrad and 500 Mrad simulation models were developed to “predict” the circuit behaviour during design phase



RD53A functional floorplan



Analog Front-Ends

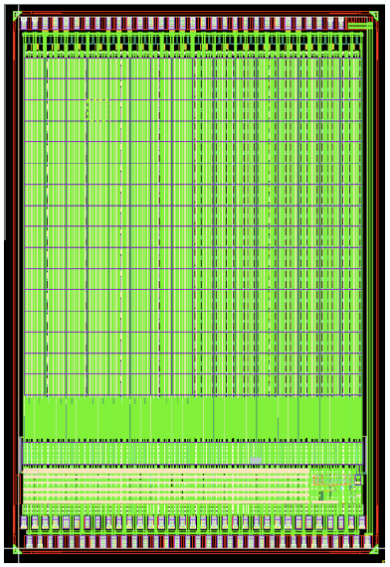
3 different AFEs designs

FE_SYNC	FE_LIN	FE_DIFF
Single stage with SAR-like ToT counter using synchronous comparator	Single stage with current comparator and ToT counter	Continuous reset integrator first stage + DC-coupled pre-comparator stage
128 columns (16x8)	136 columns (17x8)	136 columns (17x8)
0-127	128-263	264-399

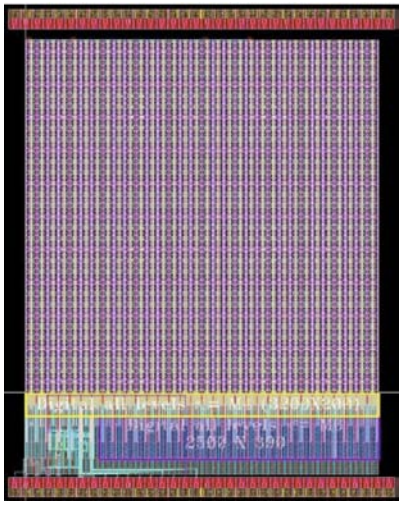
- Common calibration injection circuit scheme implemented
  - Based on 3 levels: CAL_HI, CAL_ME and GNDA
  - The levels (pulse amplitude) are set by 12-bit DACs → LSB ~ 50 e^-
  - Allows to inject in the same pixel two consecutive pulses with different amplitudes
  - Allows to inject pulses with different amplitudes in two adjacent pixels

Small scale demonstrators

- **FE_SYNC** and **FE_LIN** included in the **CHIPIX65 demonstrator** (64x64) submitted at end of June 2016 and currently under test

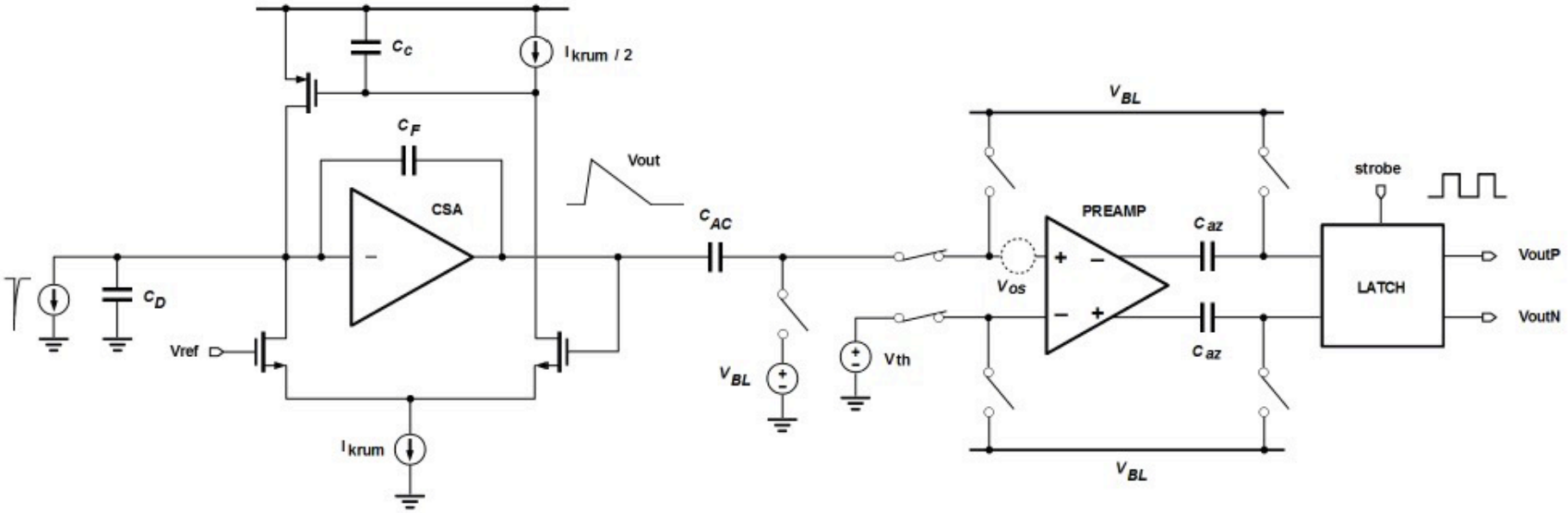


- **FE_DIFF** is included in the **FE65-P2 demonstrator** (64x64), currently under test

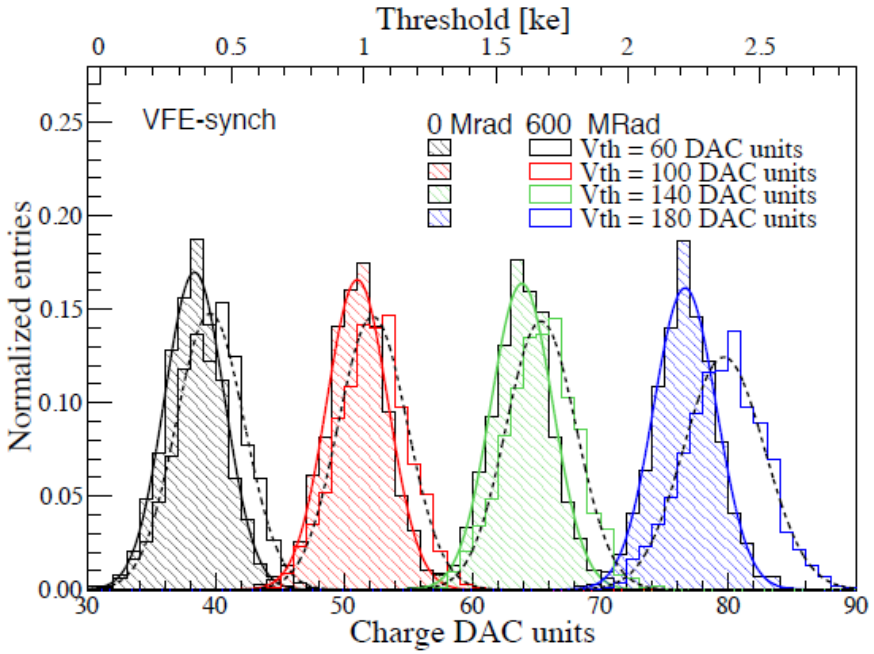


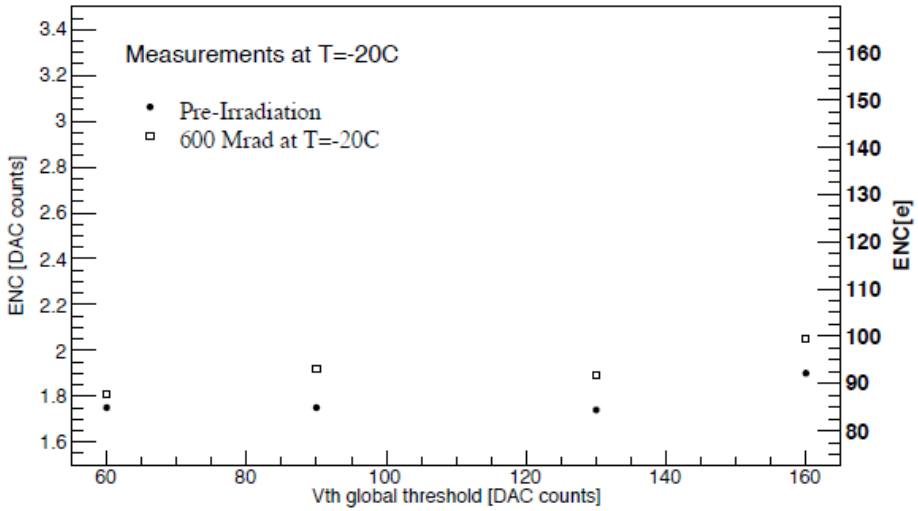
FE_SYNC architecture

- telescopic-cascode CSA with Krummenacher feedback for linear Time-over-Threshold (ToT) charge encoding
- synchronous hit discriminator with track-and-latch voltage comparator
- threshold trimming by means of autozeroing using capacitors
- 40 MHz 4-bit ToT or 5-bit fast ToT counting with latch turned into a local oscillator (100-900 MHz)
- efficient self-calibrations can be performed according to online machine operations
- successfully tested (also after irradiation) using dedicated mini@sic small-prototypes
- inserted and tested inside the CHIPIX65 demonstrator chip



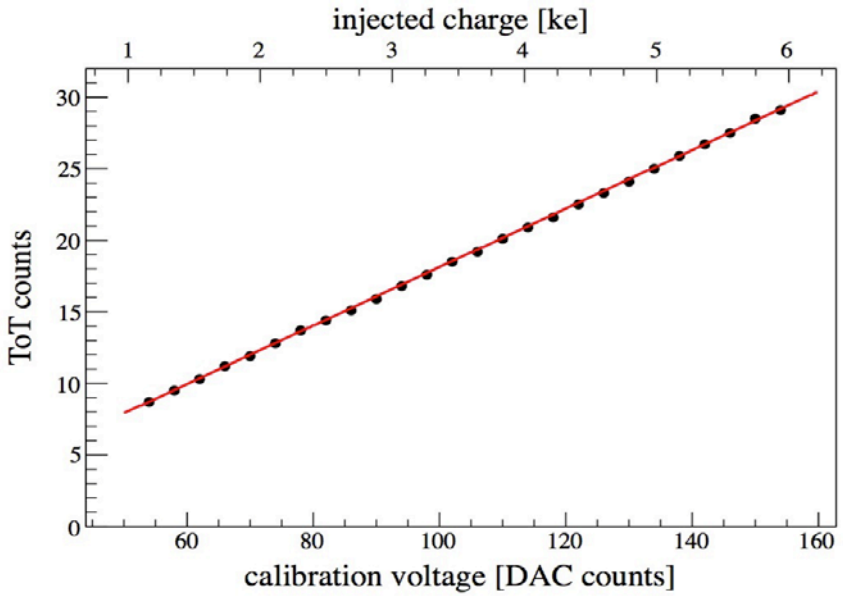
FE_SYNC – Test results / 1

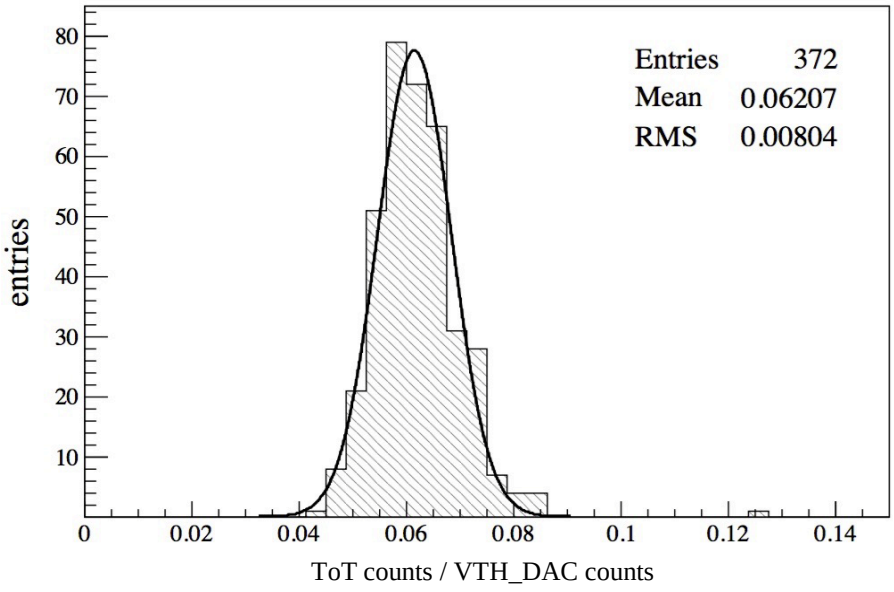




- Through the S-curves technique noise and threshold dispersion have been evaluated for 1024 pixels with different global threshold values
- The measurements have been repeated after a TID = 600 Mrad has been reached with X-ray irradiation at -20° C with the chip in working conditions
- The irradiated chip is still fully operational
- For thresholds below 1 ke^-, which is the region of interest, the increase of the dispersion with radiation is below 10%
- The ENC shows around 10% increase after irradiation

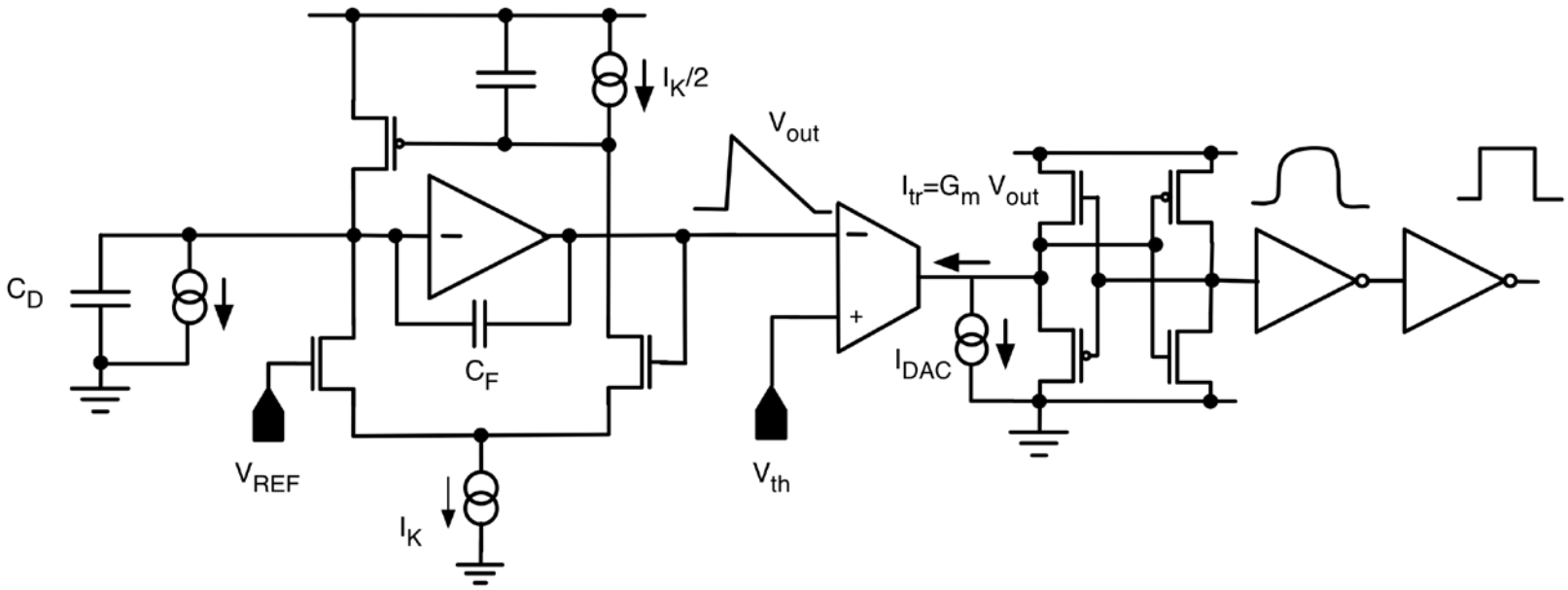
FE_SYNC– Test results / 2





- The fast Time-over-Threshold counting has been tested
- A very good linearity for the 5-bit fast ToT has been measured
- 320 MHz frequency reached before irradiation with 20% decrease after 600 Mrad
- The ToT distribution across the 1024 pixels is around 10% due to the mismatch effects and the result is compliant with CAD simulations

FE_LIN architecture

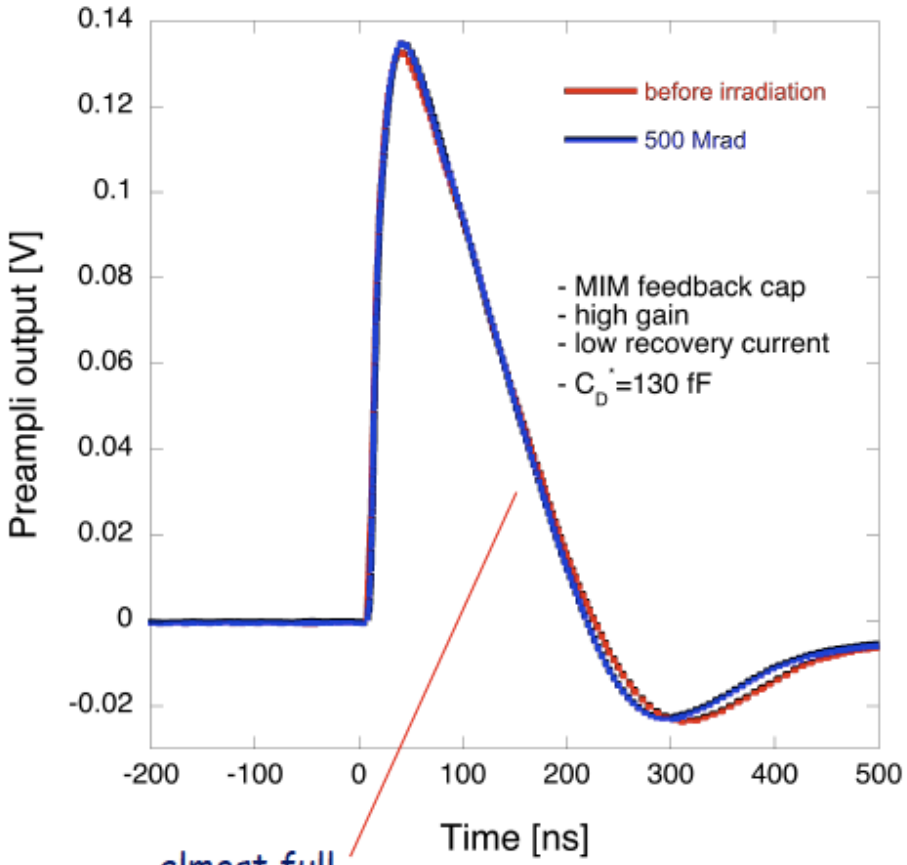


- **Single amplification stage** for minimum power dissipation
- **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- High speed, low power **current comparator**
- **4 bit local DAC for threshold tuning**
- **In-pixel calibration circuit**

- Selectable gain (1 bit)
- Overall **current consumption**: ~4 uA

FE_LIN : test results (mini@asic)

CSA response @500 Mrad



- Chip 10 (200 Mrad X-ray)

Time walk [ns]

	C_D=0	C_D=50 fF	C_D=100 fF
ch3	12.3	16.3	21.6
ch4	13.6	18.1	22.6

- Chip 11 (500 Mrad X-ray)

Time walk [ns]

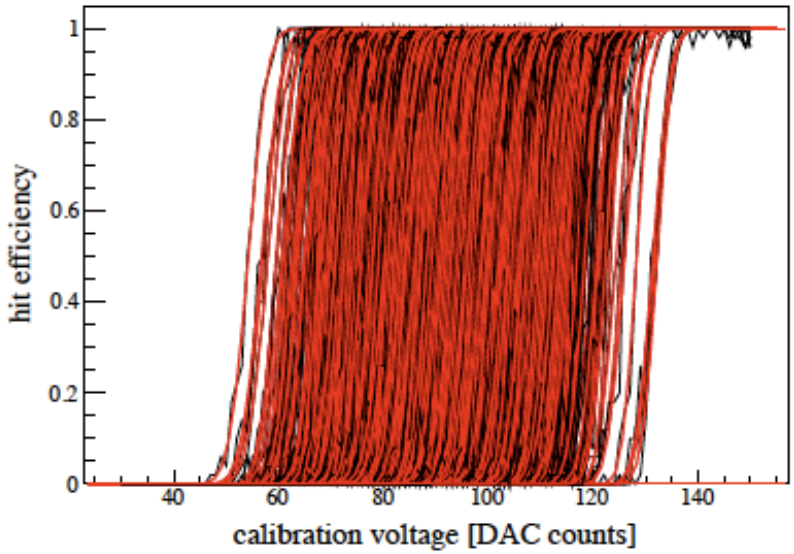
	C_D=0	C_D=50 fF	C_D=100 fF
ch3	13	16.4	19.5
ch4	14.2	19.2	23.6

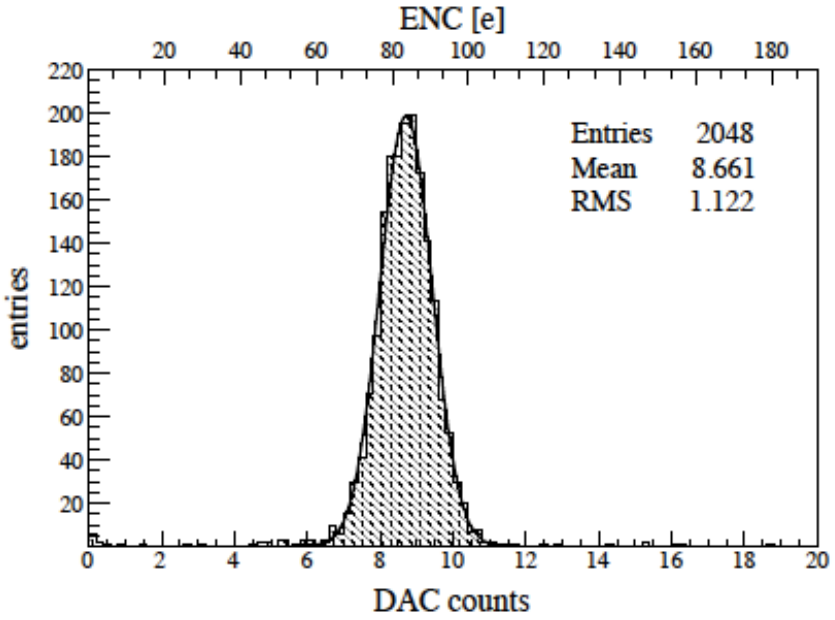
ch3=channel with PMOS feedback cap

ch4=channel with MIM feedback cap

FE_LIN : test results (Chipix65)

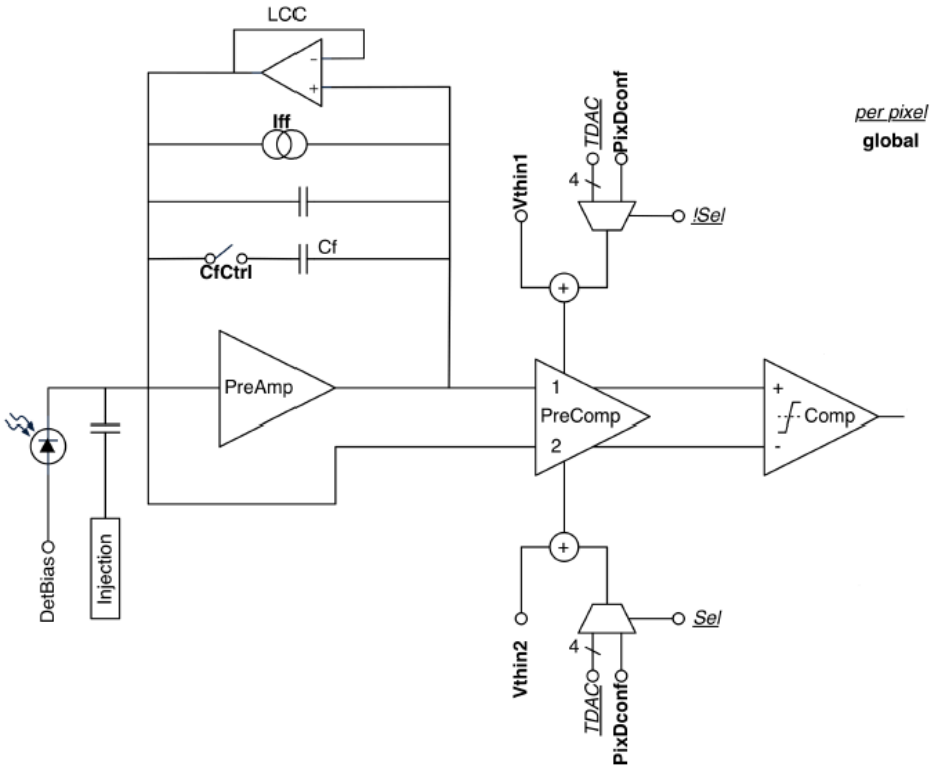
Preliminary





- Measurements on the CHIPIX demonstrator: all pixels tested and fully working
- 450e rms untrimmed threshold dispersion, ENC 85e rms noise before irradiation, in agreement with simulations. 125e rms residual threshold dispersion, still to be optimized
- Measurements on-going in Bergamo, mainly focused on the Threshold tuning

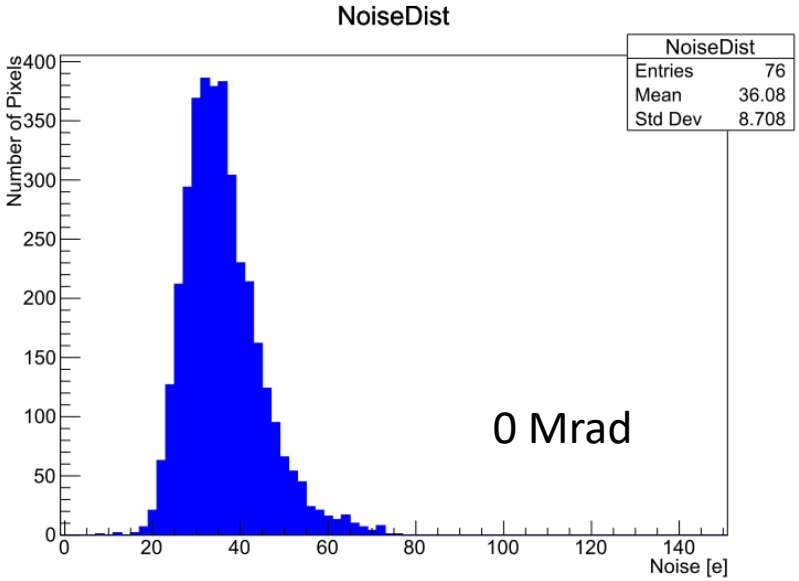
FE_DIFF architecture

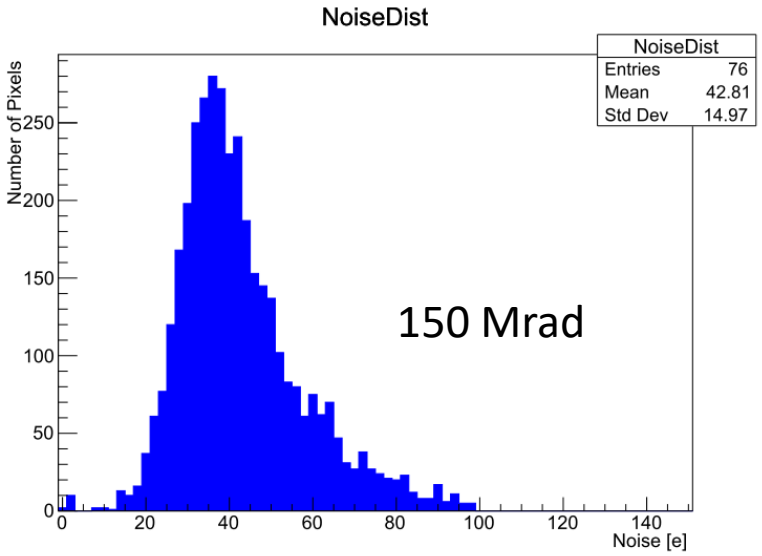


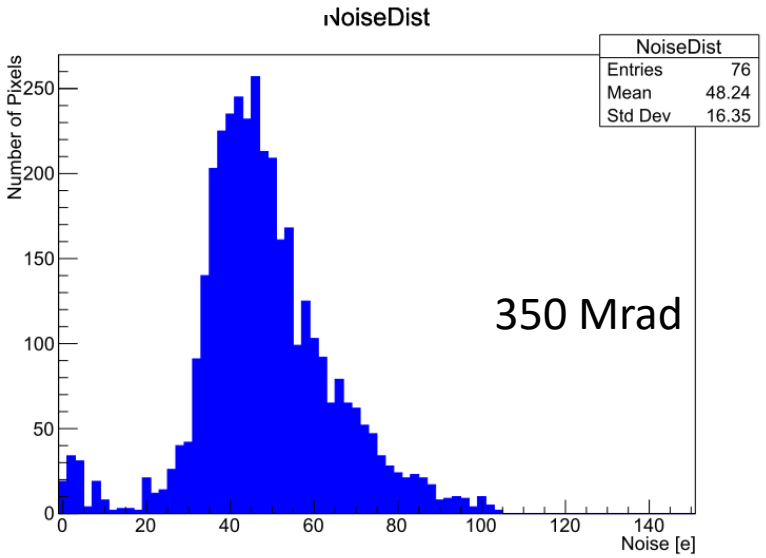
- **Continuous reset integrator** first stage with **DC-coupled pre-comparator stage**
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation** (not shown) a la FEI4
- **Threshold adjusting** with global 8bit DAC and two per pixel 4bit DACs

FE_DIFF: post irradiation noise (FE65_P2)

- The AFE prototype in FE65_P2 shows limited degradation of its noise performance







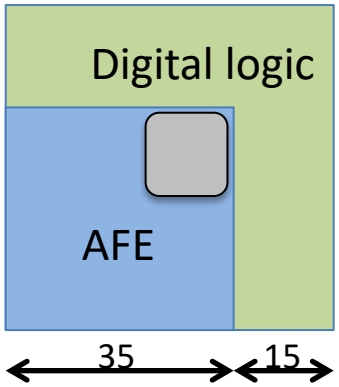
AFEs main features

	Synch AFE	Lin AFE	Diff AFE*	spec
Charge sensitivity [mV/ke]	43	25	103	-
ENC rms [e]	67	83	53	<<126
Threshold dispersion σ(Qth) rms [e]	93	32	20	<<126
$\sqrt{(ENC^2 + \sigma(Qth)^2)}$ [e]	115	89	54	≤126
In-time overdrive [e-]	≤50	≤100	0	≤ 600
Current consumption [μA/pixel]	3.3[1]	4.3	3.5	≤ 4
Time over threshold [ns]	121	99	118	< 133

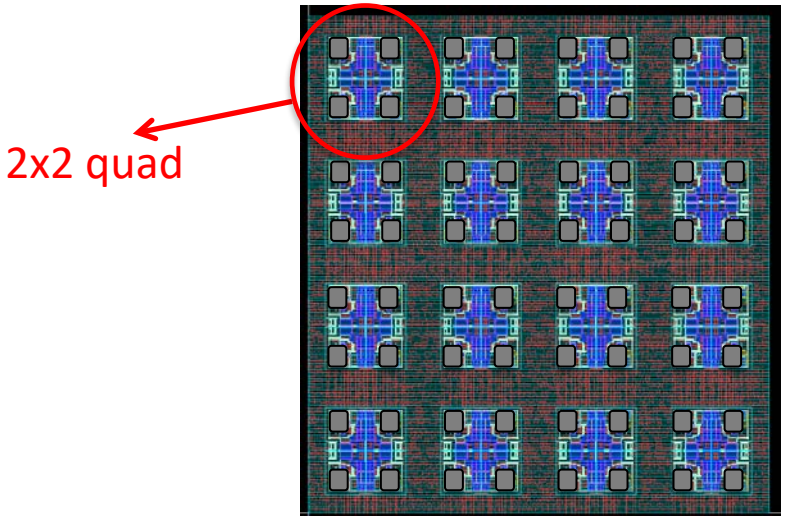
- Post-layout simulations (*except for the Diff AFE→ schematic level sim), CD=50fF, T=27°C, Qth=600e-.
- In-time overdrive→ relative to a Qin=30ke-
- Time walk → Qin=1200 e- (relative to a Qin=30ke-)
- ToT → Qin=6ke-
- [1] 5.1uA including the latch

50μm X 50μm Pixel floorplan

1) 50% Analog Front End (AFE)
50% Digital cells



2) The pixel matrix is built up of 8 x 8 pixel cores → 16 analog islands (quads) embedded in a flat digital synthesized sea



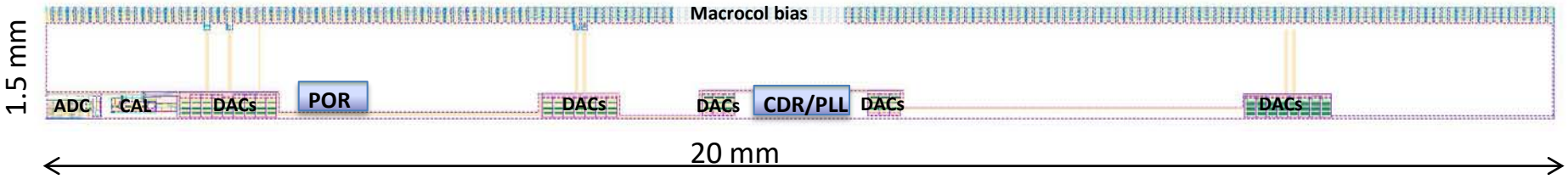
3) A pixel core can be simulated at transistor level with analog simulator

4) All cores (for each FE flavour) are identical → Hierarchical verifications

Analog Chip Bottom (ACB)

- Macroblock containing all analog IPs (all prototyped, tested and irradiated)

Building blocks	Function
12-bit Monitoring ADC	Monitoring
10-bit current DAC	Bias
12-bit voltage DAC	Calibration
Bandgap reference	Bias
POR	Reset
CDR (PLL)	Clock and data recovery
Temp. and rad. Sensors	Monitoring
Analog buffer	Calibration/Monitoring
Ring oscillators	Monitoring

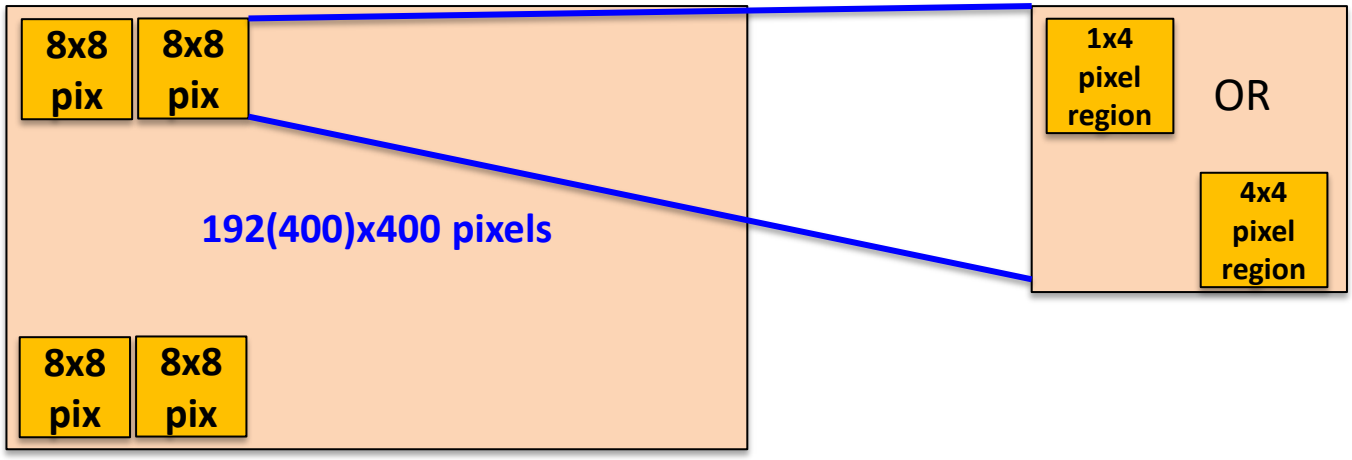


- ACB assembly: done → Mixed-signals simulations ongoing

Pixel array logic organization

Array organization

basic layout unit: **8x8 digital Pixel Core → synthesized as one digital circuit**



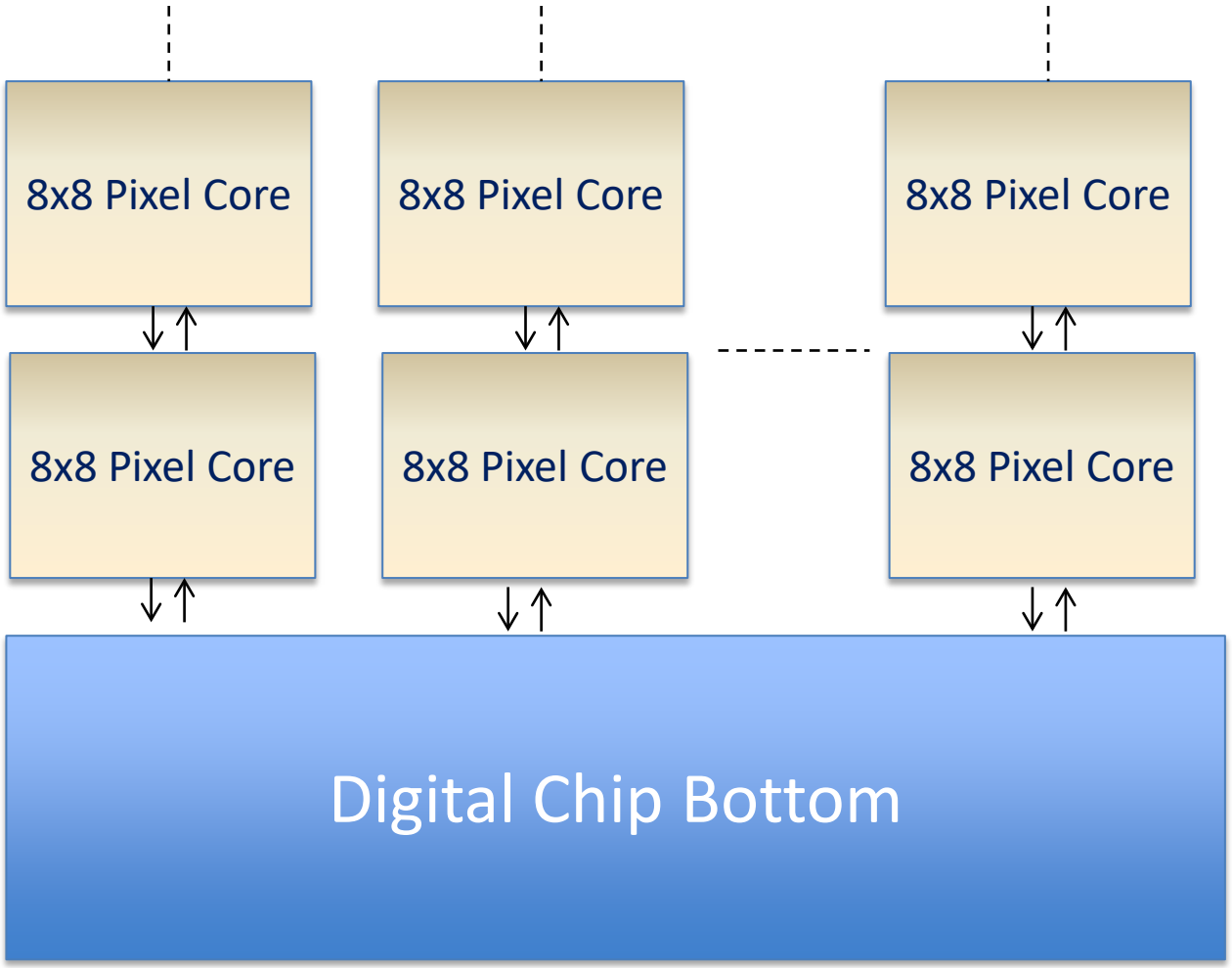
- **One Pixel Core** contains **multiple Pixel Regions (PR) and** some **additional arbitration and clock logic**
- **Pixel Regions share most of logic and trigger latency buffering**

Distributed Buffering Architecture (FE65_P2 based (2x2)):
- distributed TOT storage
- changed to **1x4** because more convenient for buffer occupancy

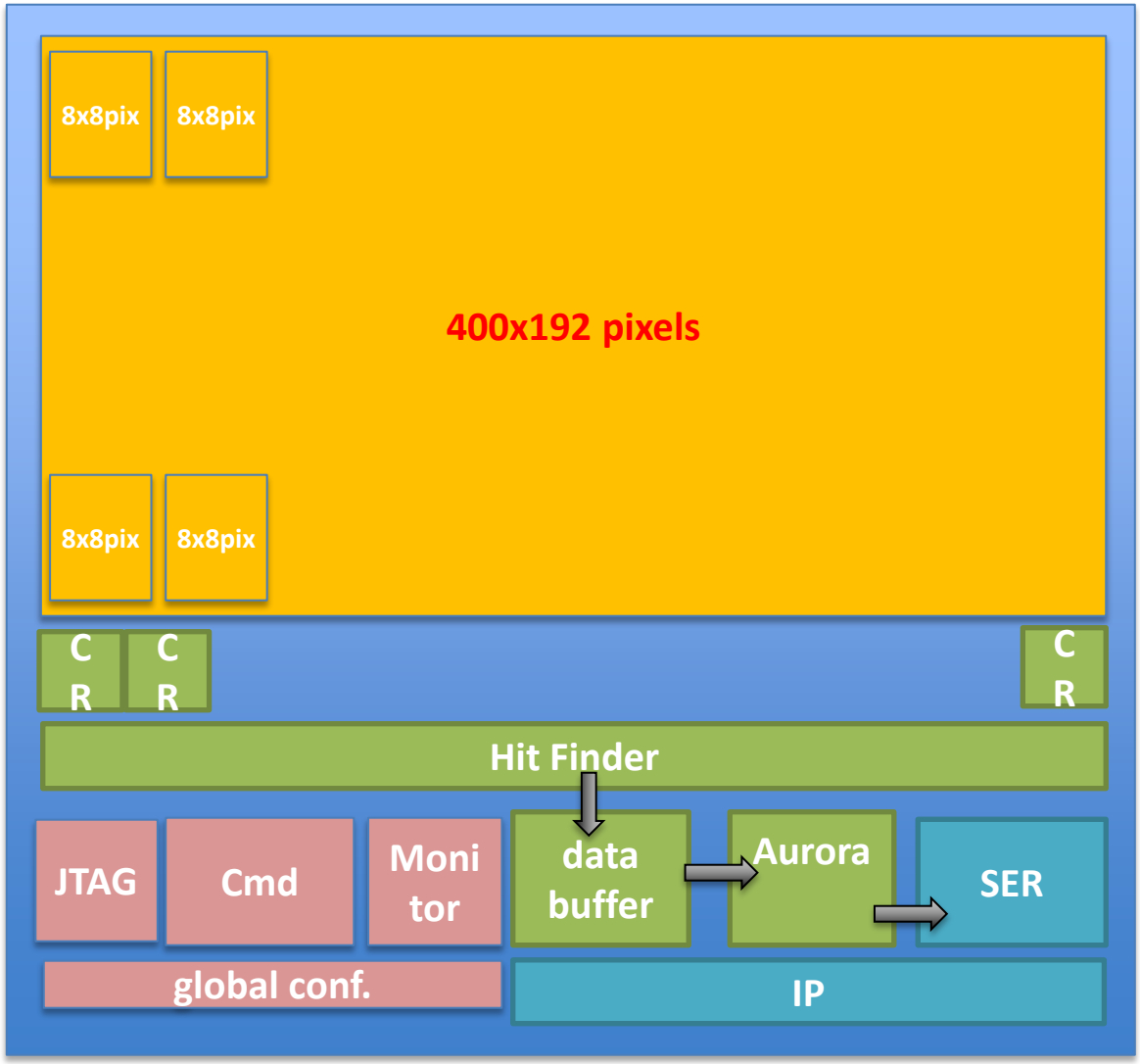
Centralized Buffering Architecture (Chipix based (4x4)):
- centralized TOT storage
- ~ same power
- ~ 10% less area
- Integrated with FE_SYNC (Fast ToT)

Pixel array logic organization

- Each Pixel Core receives all input signal from the previous core (closer to the Digital Chip Bottom)
- Regenerates the signals for the next core.
- The timing critical clock and calibration injection signals are internally delayed to have a uniform timing (within 1-2 ns)

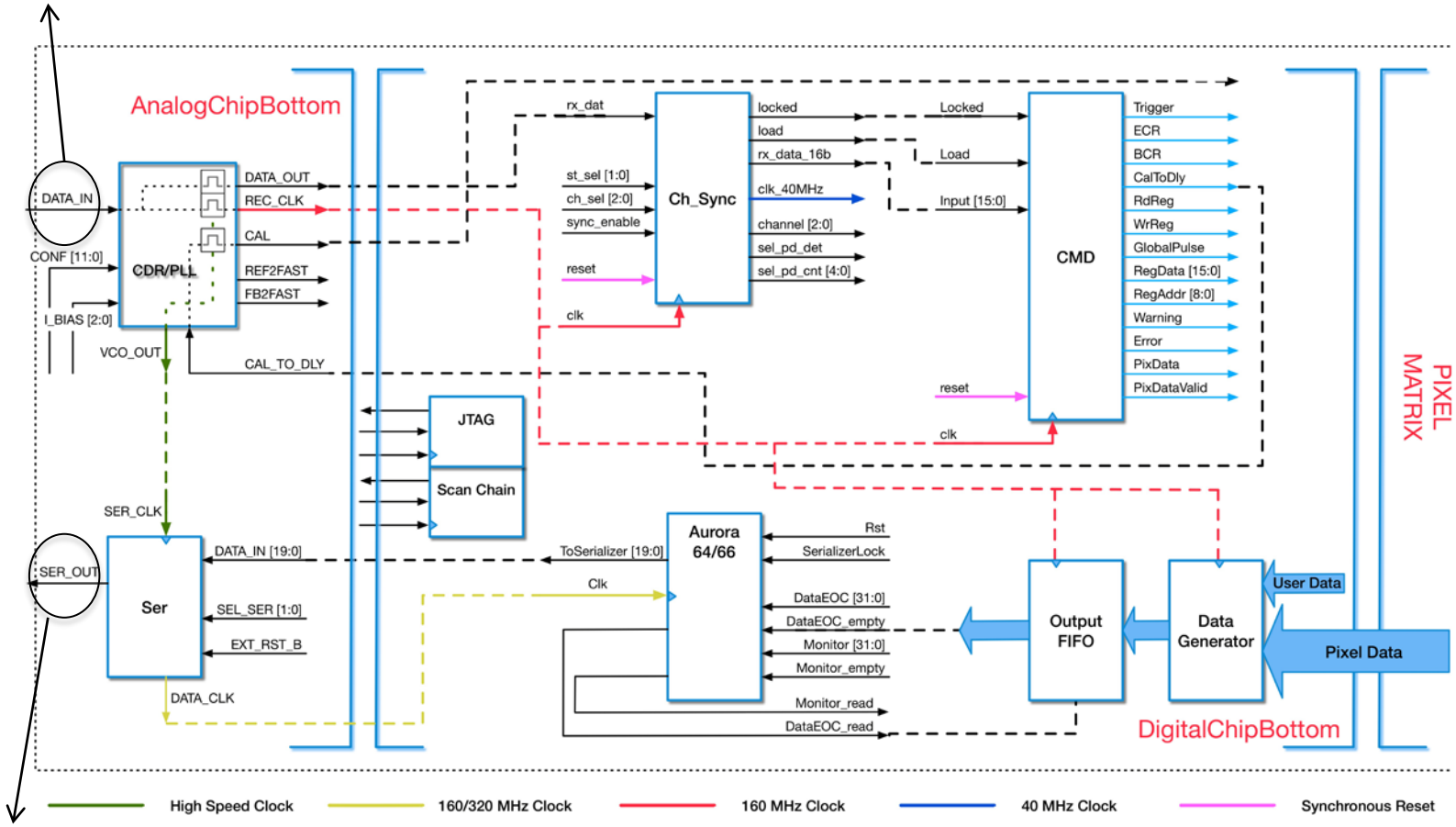


RD53A logical floorplan



Digital Chip Bottom

Single serial input stream



Port A: 1-2-4 CML outputs @ 1.28 Gbps

OR

(Port B: 1 output @ 5.12 Gbps)

} Encoding: Aurora 64/66

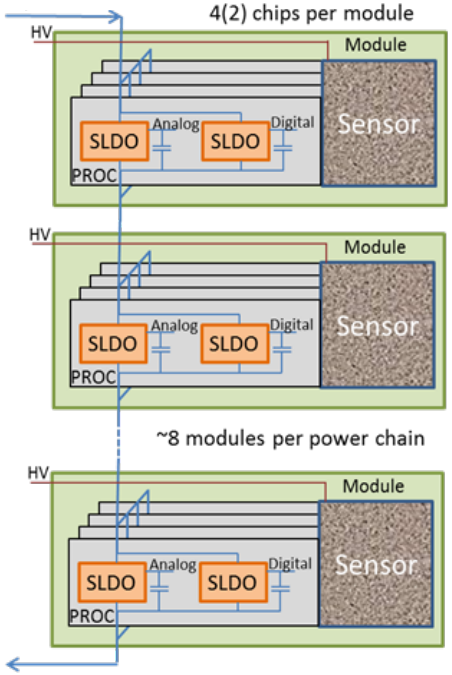
Digital (pixel matrix + chip bottom)

	RTL	Integrated
Distrib. Buffer. Arch (DBA)	+++	+++
Central. Buffer. Arch (CBA)	+++	+++
FE_SYNC	+++	+++
FE_LIN	+++	+++
FE_DIFF	+++	++
Pixel Configuration	+++	+++
Command Decoder	+++	+++
Data concentrator	+++	+++
Aurora 64b/66b: Single	+++	+++
Aurora 64b/66b: Multi	**+++**	+++
JTAG	**+++**	**+++**
DFT	-	-
Data Compression	-	-

	RTL	Integrated
Global Configuration	+++	+++
Monitoring/Readback	++	+
SEU	+++	+
ACB	**++ (characterization)**	
IO	**+ (characterization)**	
Top LVS/DRC	**+**	
Top STA	**+**	
Top verification		

Serial powering

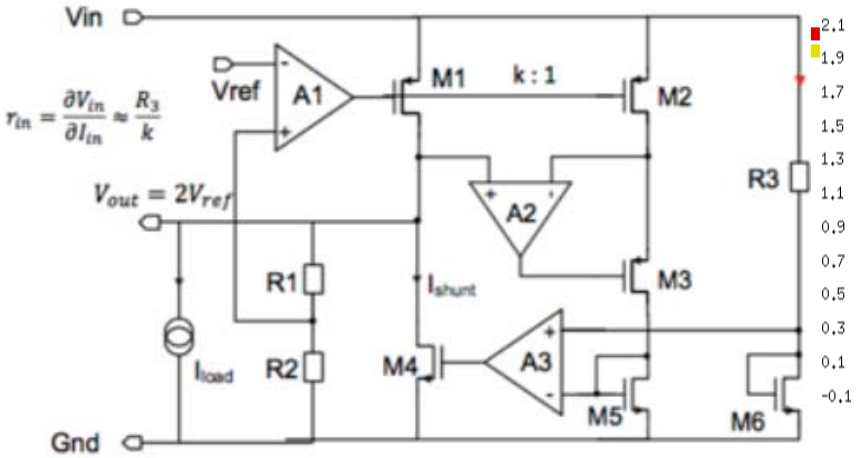
- RD53A is designed to operate with ***Serial Powering*** → constant current to power chips/modules in series
- Based on **ShuntLDO**
- Dimensioned for production chip

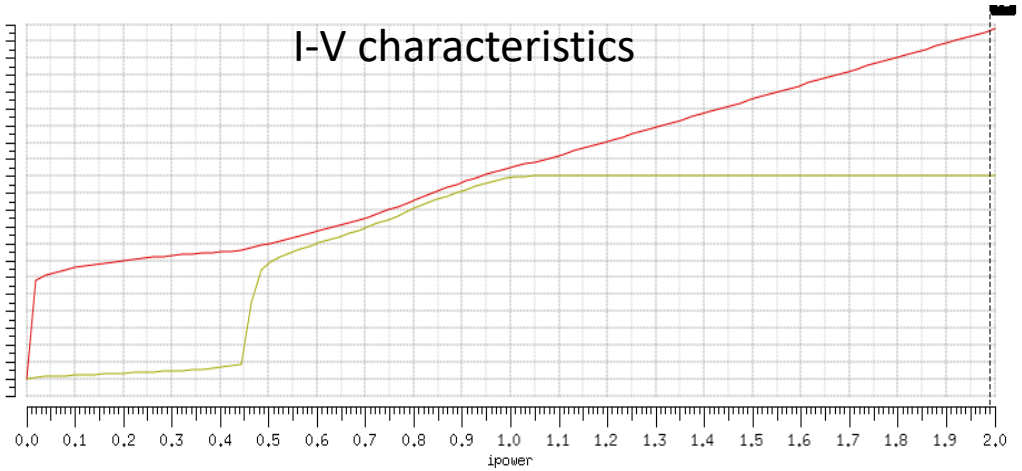


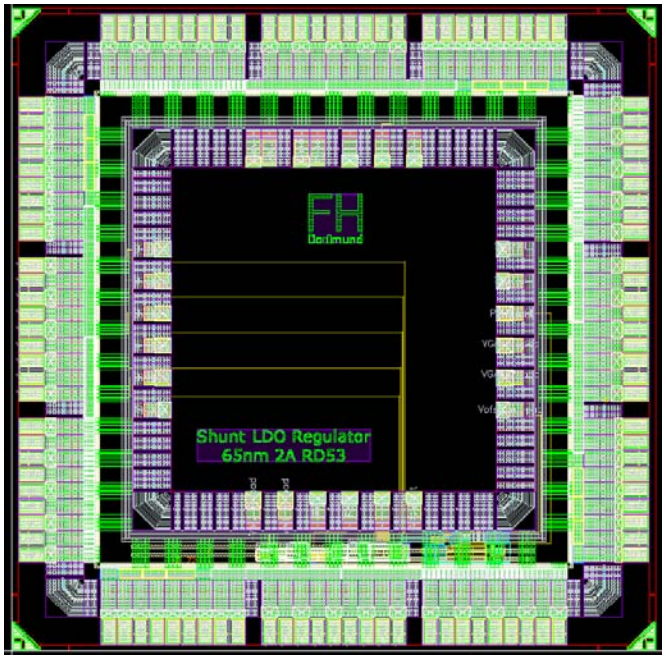
Three operation modes:

1. ShuntLDO: constant input current Iin → local regulated VDD
2. LDO (Shunt is OFF) : external un-regulated voltage → local regulated VDD
3. External regulated VDD (Shunt-LDO bypassed)

2A ShuntLDO



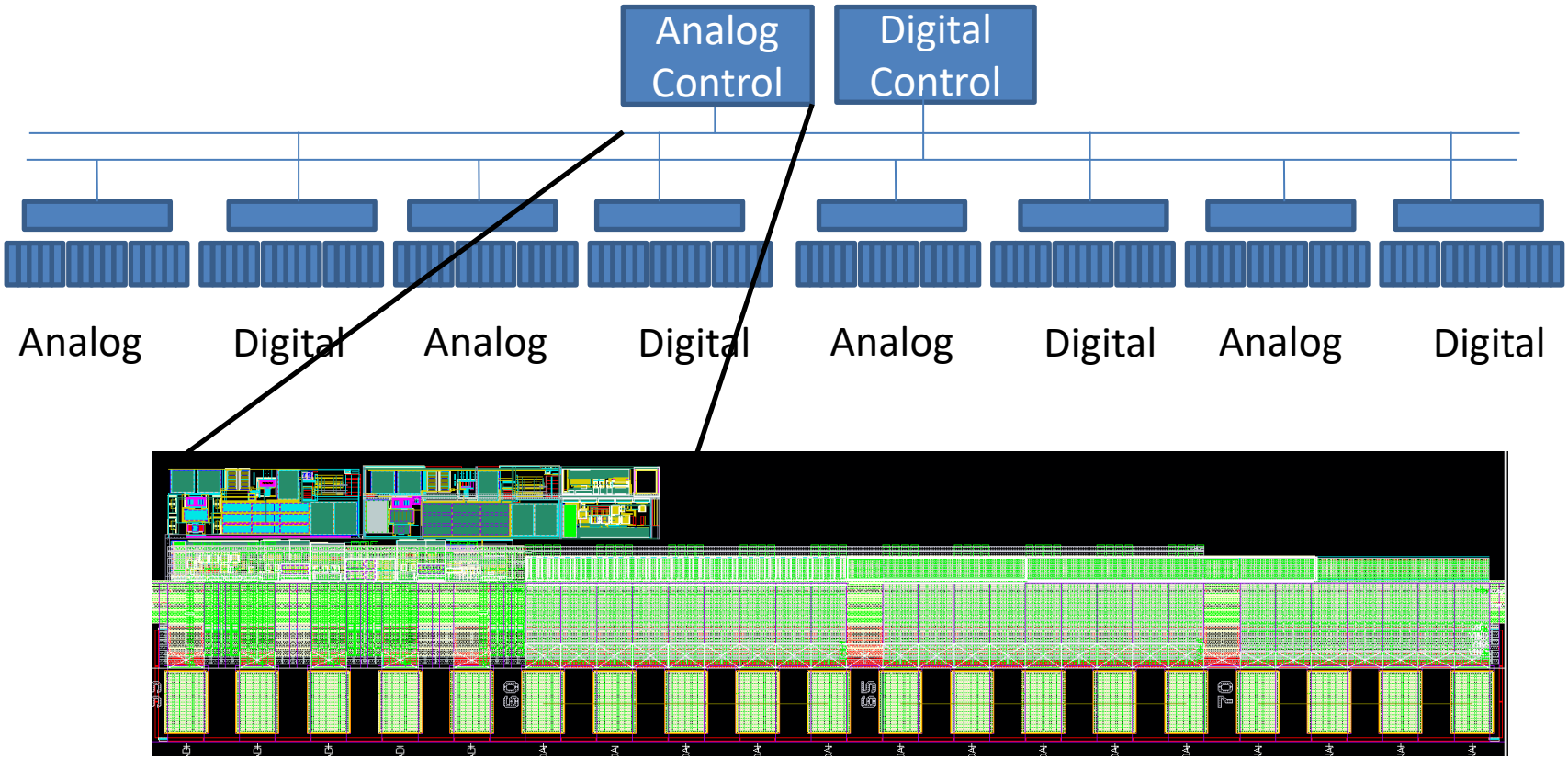




A prototype of 2A version is under testing

Shunt-LDO floorplan

- ShuntLDOs are located in the IO Frame → power lines come only from the bottom
- Power transistors are splitted into 4 blocks for better distribution of power

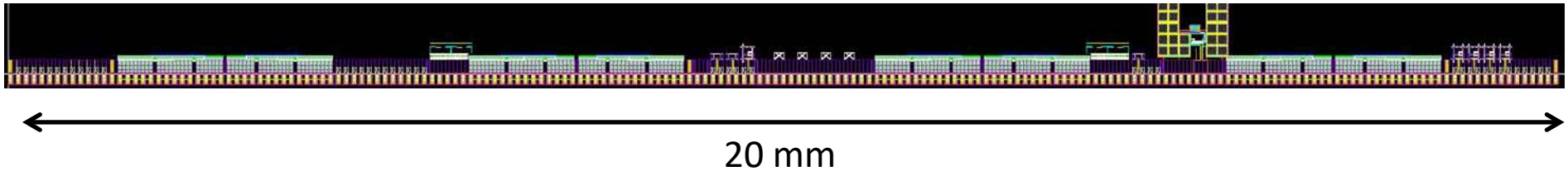


IO Bottom Padframe

This is a macroblock containing:

- ❑ IO Pads + ESD protection blocks
- ❑ ShLDO voltage regulators
- ❑ Drivers/Receivers

- 198 PADs with 100 μm pitch
- Passivation opening: 58 μm x 86 μm → reliable wire bonding
- Compatible with TSV (backside etch process)
- SLVS Drivers/Receivers
- Port A: 1.28 Gbps Serializer + CML driver
- Port B: 5 Gbps serializer + driver: not yet ready, not confirmed

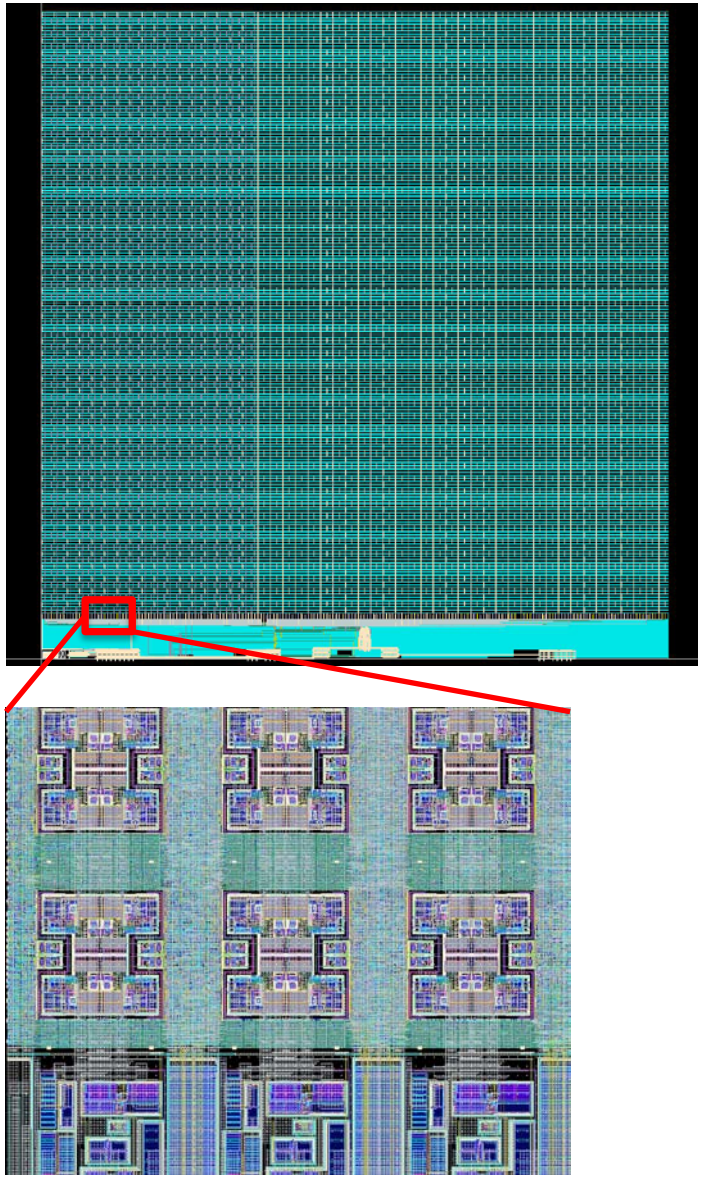


- Top PADFRAME (for test and monitoring, not in production chip): almost finalized

RD53A TOP LEVEL INTEGRATION

Top level integration flow works smoothly

Full chip physical verifications (DRC, LVS) are relatively fast (3.5 hrs) thanks to hierarchical structure



RD53A Verification

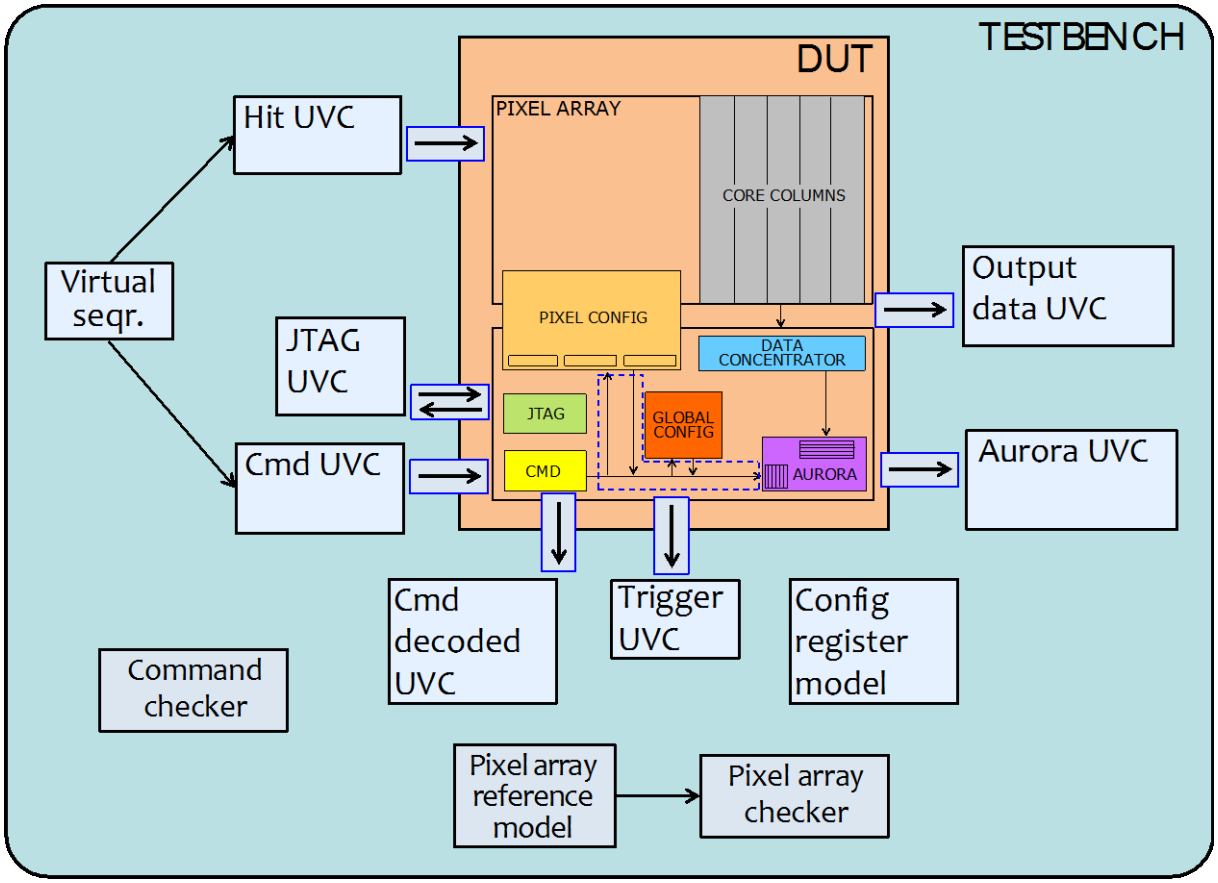
UVM testbench allowing for reusability and automated verification functions

Main interface verification components (UVC):

- Hit (sensor pixel hit data)
- Command (custom input protocol for control and trigger)
- Aurora (monitor pixel chip output)
- JTAG (reuse from verification IP)

Automated verification components:

- Pixel array reference model (predict output hits according to trigger)
- Pixel array checker (compare predicted output vs real output)
- Lost hits classifiers
- Configuration register model (reference for operations to global configuration and pixel configuration)



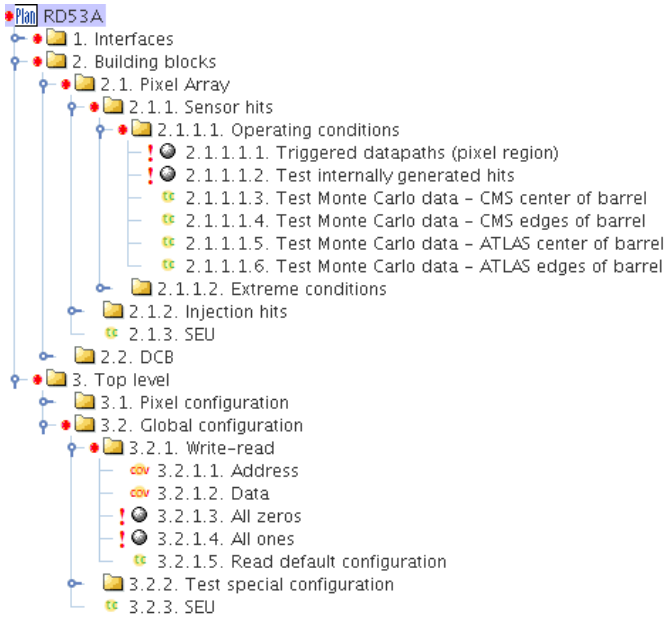
RD53A Verification

Verification approach:

1. *Constrained-random tests* → functional coverage collection
   - Based on generation of constrained-random inputs (e.g. hits and triggers at operating conditions, from physics Monte Carlo simulations)
   - Automated pixel array verification through reference model and checker
   - Automated global configuration and pixel configuration registers verification through register model
2. *Directed tests* → specific test cases aimed to verify specific functions and unlikely perturbations (e.g. extreme hit/trigger conditions)
   - Custom command sequences
3. *Generation of stimuli for analog simulations*
   - Dump VCDs

Verification plan containing planned coverage elements and testcases

Updated with test regressions for measuring verification progress



Implementation status:

1. *Interface UVCs:* finalizing development and reusing IPs
2. *Configuration register model:* being added
3. *Directed tests:* writing custom command sequence for verifying specific functions (e.g. digital injection, command protocol errors)

Summary

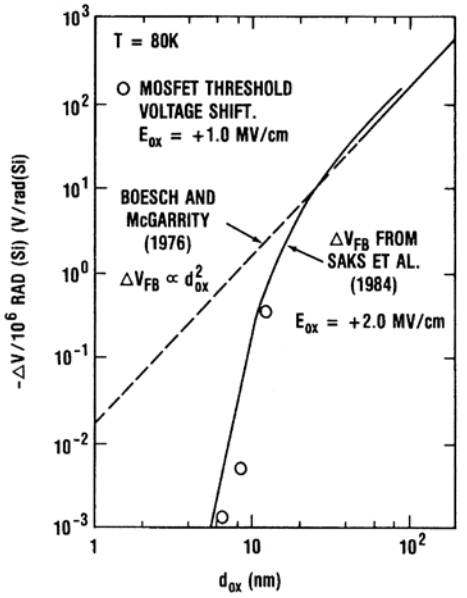
- **RD53A demonstrator** chip design is ongoing
- Excellent sharing of resources/ideas among ATLAS and CMS
- Design based on production chip but include different AFEs and pixel logic architectures for detailed comparison
- Many test features and backup solutions adopted for chip debugging
- Design strategy to withstand the expected radiation environment (500Mrad at -15°C)
- Final design is almost ready, extensive verifications are on-going
- Verification plan for chip debugging

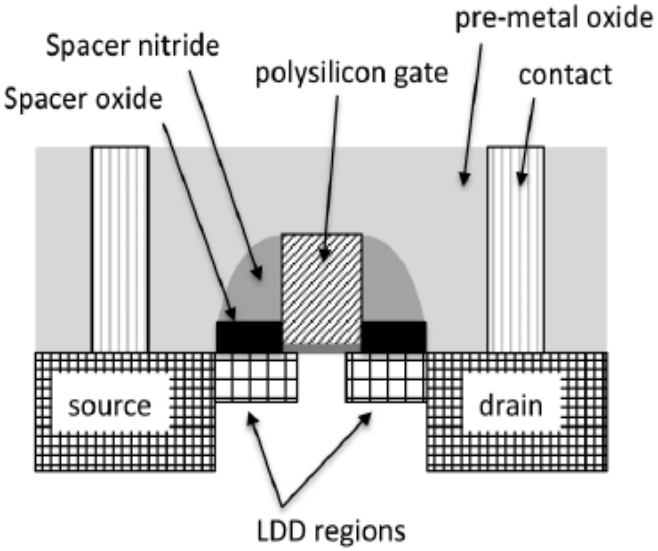
Chip submission on 31 May 2017

Backup

Radiation effects in CMOS

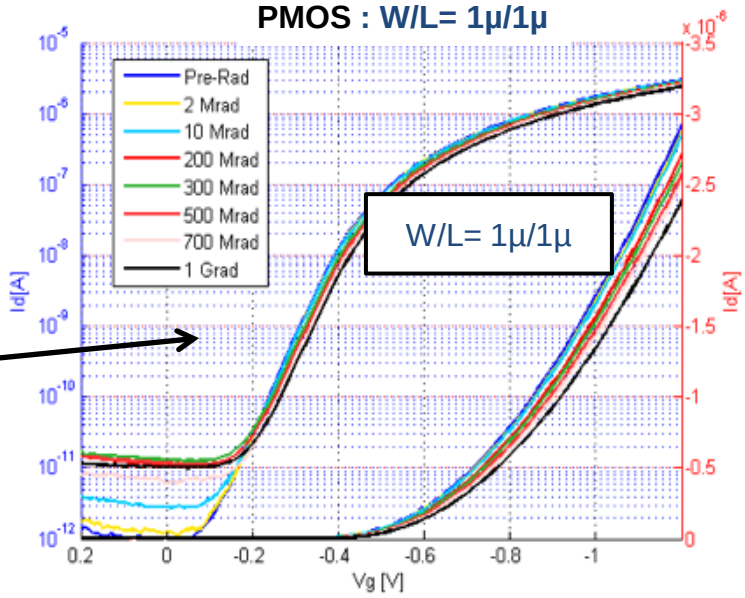
- Baseline technology : 65nm CMOS for the RD53 project
- The TID-induced charge in the thin oxide decreases with the thickness of the oxide
- In highly scaled processes
  - The thin gate oxide is very tolerant to the TID
  - Thick oxide used for isolation : Thick Shallow Trench Isolation Oxide (STI)
  - Thick oxide exists everywhere around the device
- Radiation Induced Leakage Current (RILC)
- Radiation Induced Narrow Channel Effect (RINCE)
- Radiation Induced Short Channel Effect (RISCE)



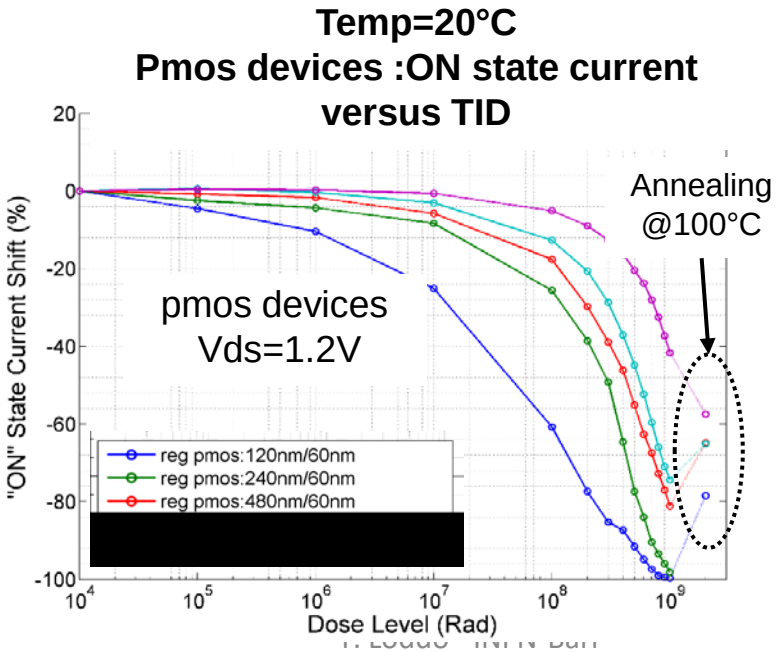


TID effects on the 65nm devices

- The increase of the leakage current is very limited
  - Factor 100 for the worst case
- The enclosed layout is not needed
- PMOS devices more sensitive than NMOS
- TID effect on large and long devices (NMOS and PMOS) is limited



- Analog Design : <u>Avoid the use of narrow or short transistors</u>
  - Analog designs following these rules showed a good radiation tolerance up to 1 Grad
  - Irradiation damage depends on the bias. This affect the matching and can be an issue
- Digital design :
  - Requires high integration density
  - Digital cells are designed with minimum size devices and so are subject to RINCE and RISCE effects

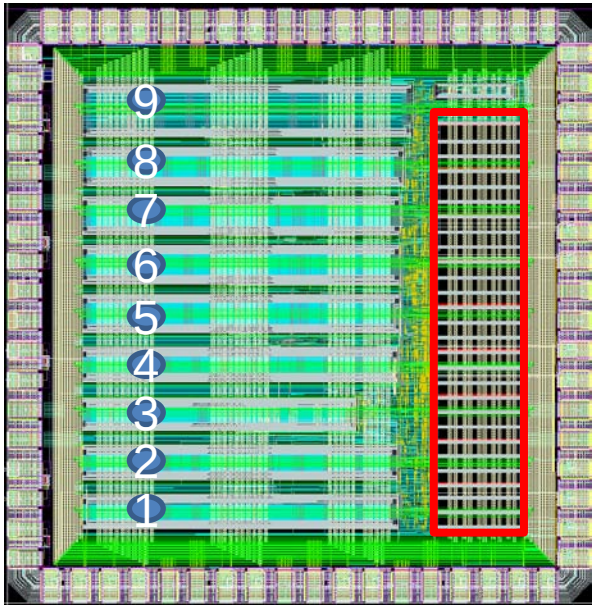


Temperature and annealing effect

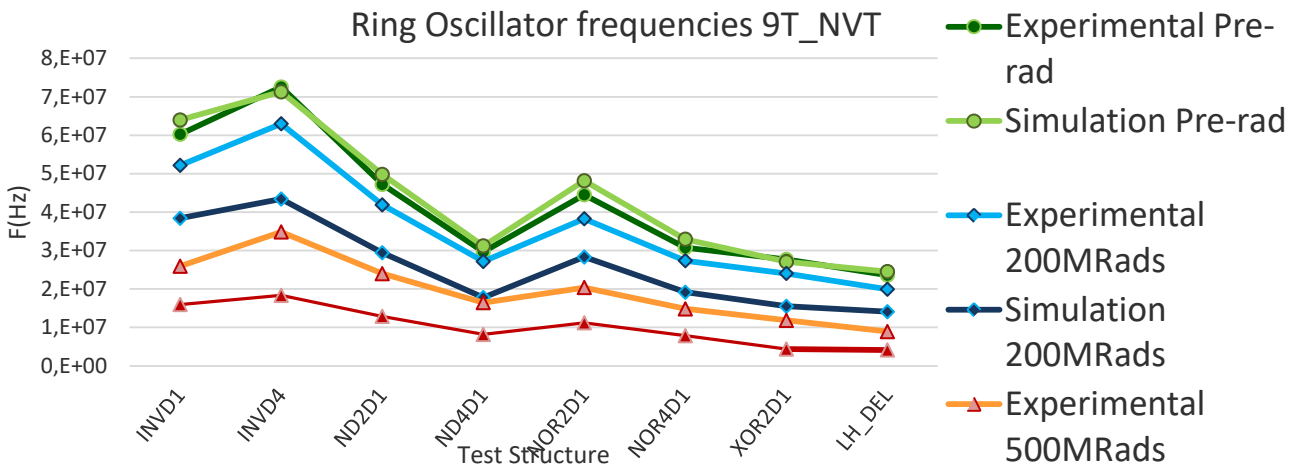
- Less damage for the PMOS and NMOS when Irradiation is done at low temperature
- High temperature annealing (100 °C for 7 days) degrades strongly the DC parameters and show a high Vth shift
- A long term annealing at room temperature was done for ~1 year on irradiation devices at the PS-CERN -> more degradation
- Qualification and annealing for different temperature were done at CERN
- The Vth shift of the PMOS device is a thermally activated process
- Extrapolation for lower temperatures
- For the RD53 Front end chip, this temperature effect can be avoided by keeping the system :
  - In cold environment : -20°C for 5 years
  - Unbiased at room temp for few months

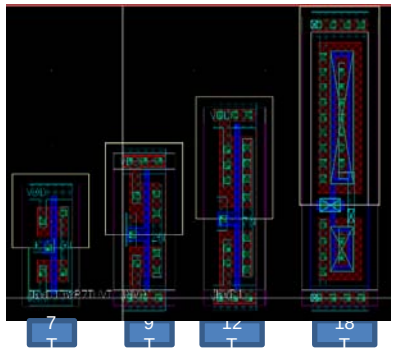
DRAD Chip : Test chip for digital design

- DRAD chip is designed at CERN :
- To study the effect of radiation on digital standard cells for the 65nm technology
- To test the efficiency and the validity of the digital simulations with the irradiation corner model
- Simulation results goes in the same direction than irradiation tests but the model overestimates the TID damage level
  - Models were done for worst case of biasing
- NOR gates should be avoided since show a strong degradation



ANNEALING NOT INCLUDED IN THE MODELS





CELL HEIGHT
7 Track: 1.4 uM
9 Track: 1.8 uM
12 Track: 2.4 uM
18 Track: 3.6 uM