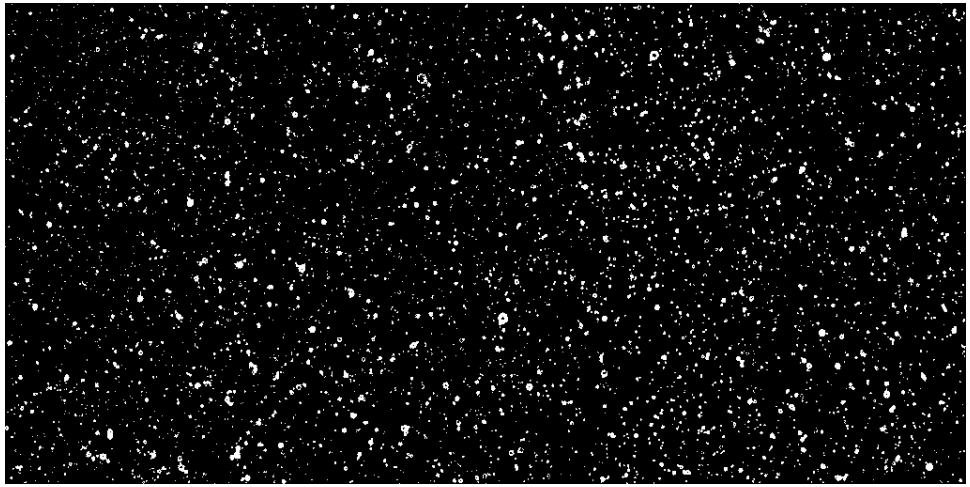
DESY, April 12th, 2017

The ALPIDE CMOS Pixel Sensor development for the ALICE ITS upgrade

W. Snoeys, CERN, for the ALICE collaboration



p-ALPIDE3 chip: 200 MeV p at PSI

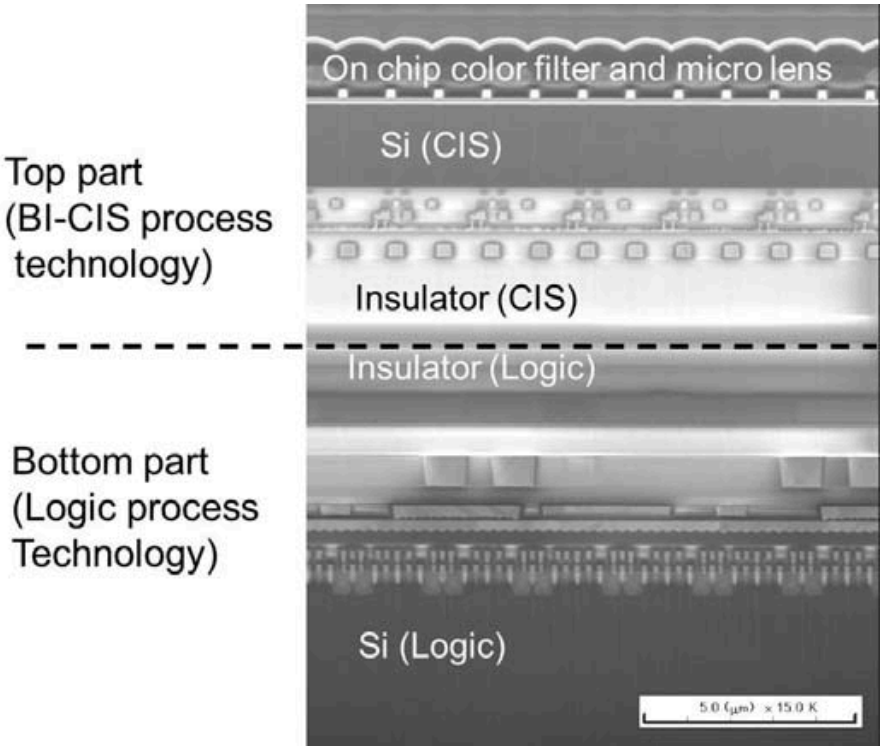
Acknowledgements

- The workshop organizers
- G. Aglieri, G. Anelli, F. Anghinolfi, P. Aspell, R. Ballabriga, S. Bonacini, M. Campbell, J. Christiansen, R. De Oliveira, F. Faccio, P. Farthouat, E. Heijne, P. Jarron, J. Kaplon, K. Kloukinas, A. Kluge, T. Kugathashan, X. Llopart, A. Marchioro, S. Michelis, P. Moreira, K. Wyllie, L. Musa, P. Riedler, M. Mager, M. Keil, D. Kim, A. Dorokhov, A. Collu, C. Gao, H. Hillemanns, S. Hristozkov, A. Junique, M. Kofarago, M. Keil, A. Lattuca, M. Lupi, C. Marin Tobon, D. Marras, M. Mager, P. Martinengo, G. Mazza, H. Mugnier, L. Musa, H. Pernegger, T. Pham, J. Rousset, F. Reidt, P. Riedler, J. Van Hoorne, P. Yang, D. Gajanana

  and other collegues from CERN and the ALICE ITS upgrade

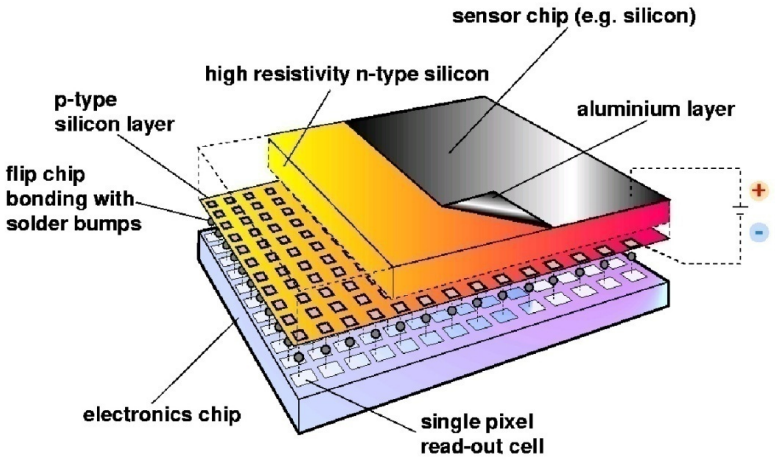
CMOS Monolithic Active Pixel Sensors

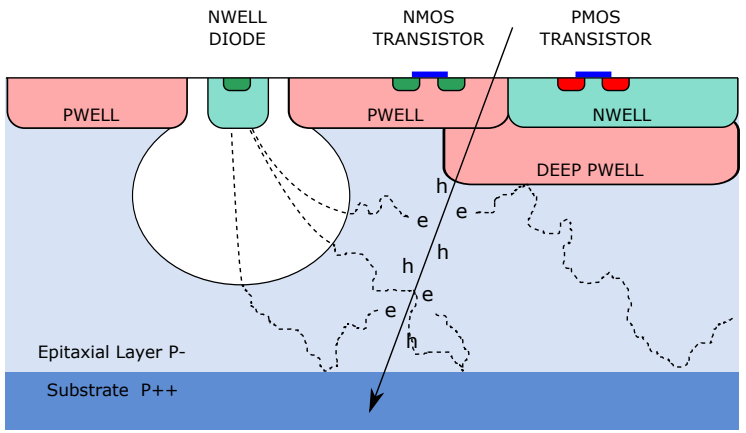
- CMOS MAPS have changed the imaging world, reaching:
  - less than 1 e^- noise
    (cfr S. Kawahito, PIXEL 2012)
  - > 40 Mpixels
  - Wafer scale integration
  - Wafer stacking
  - …
- In High Energy Physics silicon has become the standard in tracking applications both for sensor and readout
- … and now CMOS MAPS make their way in High Energy Physics !



Backside Illuminated 8M Pixel Stacked Imaging Sensor
S. Sugawa et al. Sony Corp.
ISSCC 2013

Hybrid versus Monolithic





Hybrid

- Large majority of presently installed systems
- 100 % fill factor easily obtained
- Sensor and ASIC can be optimized separately
  - Sensor other materials
  - ASIC standard CMOS

Monolithic

- Easier integration, lower cost
- Promising not only for pixel detectors but also for full trackers
- Potentially better power-performance ratio and strong impact on material budget
- MAPS installed in STAR and adopted for ALICE ITS upgrade

New technologies (Through-Silicon-Vias, microbumping, etc) could make distinction more vague. Stacked CMOS imagers are available in industry, but usually not with per pixel connection. ATLAS & CLIC (I. Peric, R. Ballabriga et al.) are investigating capacitive coupling between sensor and readout chip.

Objectives of the ALICE Inner Tracking System Upgrade

1. Improve impact parameter resolution by a factor ~3
   - Get closer to IP (radius of first layer): 39 mm -> 23 mm
   - Reduce pixel size: currently 50 μm x 425 μm -> O(30 μm x 30 μm)
   - Reduce x/X_0/layer from ~1.14% -> ~0.3% (inner layers)

2. Better tracking efficiency and p_T resolution at low p_T
   - Finer granularity: from 6 to 7 layers and all layers with pixels

3. Faster readout
   - Readout Pb-Pb interactions at 100 kHz
   - Readout pp interactions at >200 kHz (current ITS limited at 1 kHz)

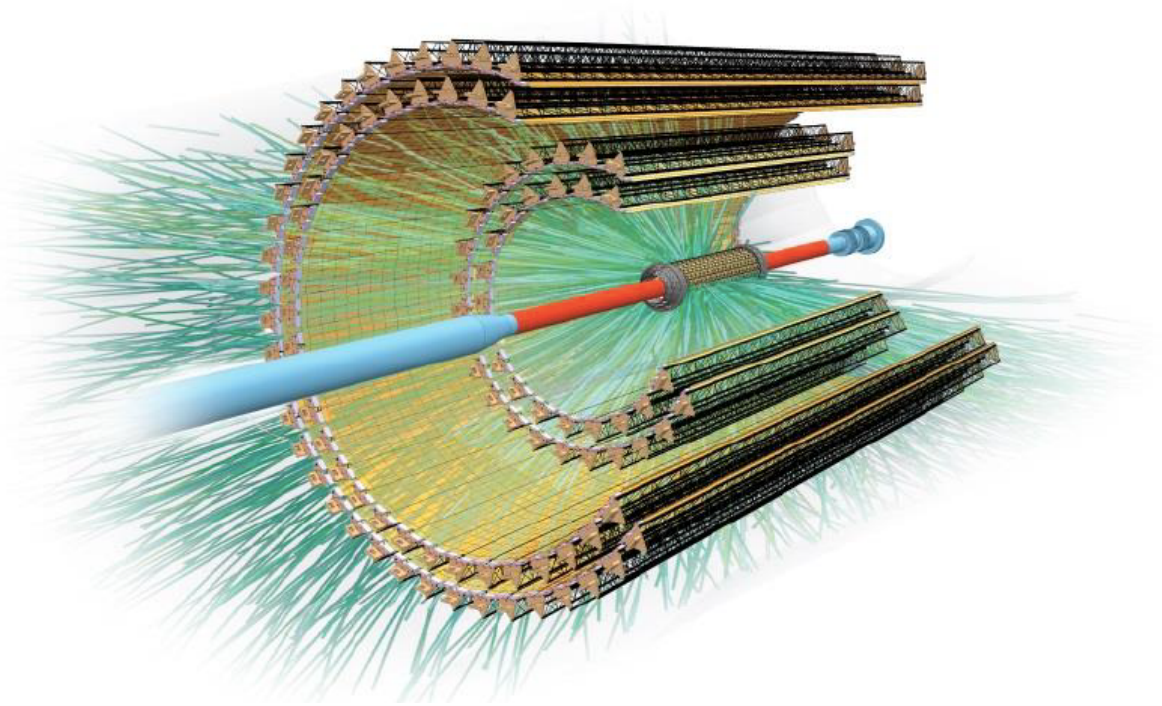
4. Design for fast removal and insertion
   - Maintenance during yearly shutdown

Technical Design Report for the Upgrade of the ALICE Inner Tracking System
J. Phys. G 41 (2014) 087002
CERN-LHCC-2013-024 ; ALICE-TDR-017

Installation of the new detector during LHC Long Shutdown 2 (2019-2020)

ALICE ITS Upgrade

Replace the inner tracking system with an entirely new detector in 2019-2020



Thin sensors (50 µm), high granularity (~30 x 30 µm^2), large area (10 m^2)
moderate radiation (TID 2.700 Mrad & NIEL 1.7 10^{13} 1 MeV n_{eq}/cm^2)

➡ Monolithic Active Pixel Sensors

General requirements for the sensor chip

Parameter	Inner Barrel	Outer Barrel
Chip size (mm x mm)	15 x 30	
Chip thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	> 99%	
Fake hit rate	< 10^{-5} evt^{-1} pixel^{-1} (ALPIDE << 10^{-5})	
Integration time (μs)	< 30 (< 10)	
Power density (mW/cm^2)	< 300 (~35)	< 100 (~20)
TID radiation hardness (krad) (**)	2700	100
NIEL radiation hardness (1 MeV n_{eq}/cm^2) (**)	1.7 x 10^{13}	1.7 x 10^{12}
Readout rate, Pb-Pb interactions (kHz)	100	
Hit Density, Pb-Pb interactions (cm^{-2})	18.6	2.8

(*) In color: ALPIDE performance figure where above requirements

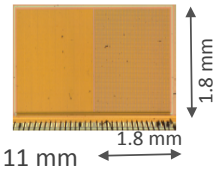
(**) 10x radiation load integrated over approved program (~ 6 years of operation)

ALPIDE Development

Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys
(Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test

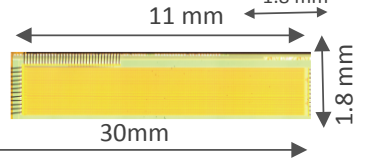
2012 Explorer

20μm x 20μm and 30μm x 30μm pixels (analogue readout)
pixel geometry, starting material, sensitivity to radiation



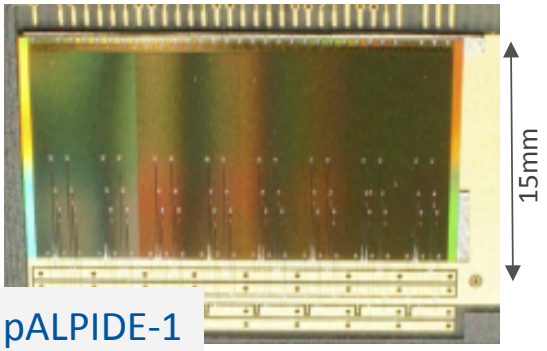
2013 pALPIDEss-0

Matrix with 64 columns x 512 rows
22 μm x 22 μm pixels
In-pixel discrimination and buffering
Zero suppression within pixel matrix



2014 pALPIDE-1

First full-scale prototype
Pixel pitch: 28 μm x 28 μm
4 sectors with pixel variants
1 register/pixel, no final interface



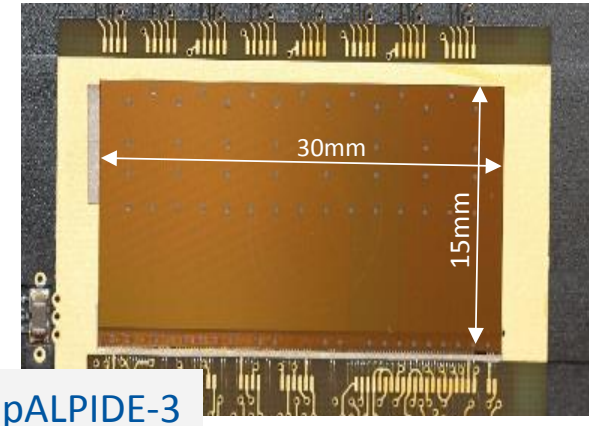
pALPIDE-1

Apr 2015 pALPIDE-2

4 sectors with pixel variants
Optimization of circuits
Allowing integration in ITS modules
No high-speed serial output

Oct 2015 pALPIDE-3

8 sectors with pixels variant
All Communication Features
(no ADC, no Temp Sens)



pALPIDE-3

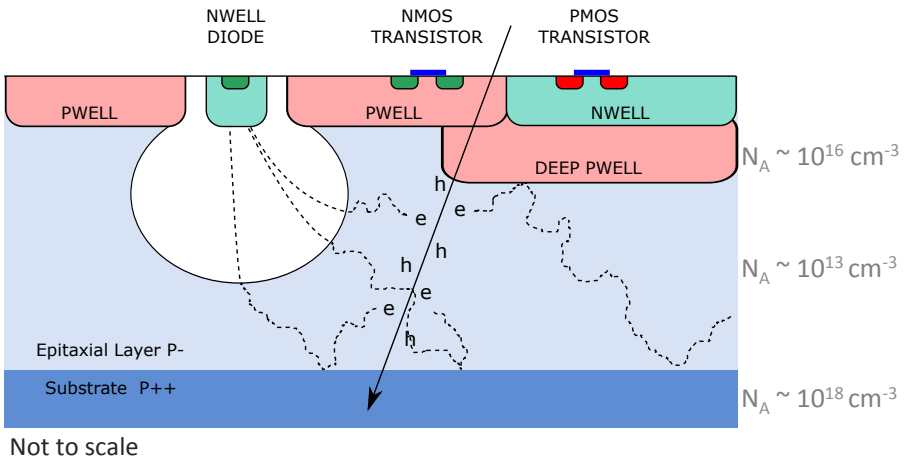
Aug 2016 ALPIDE

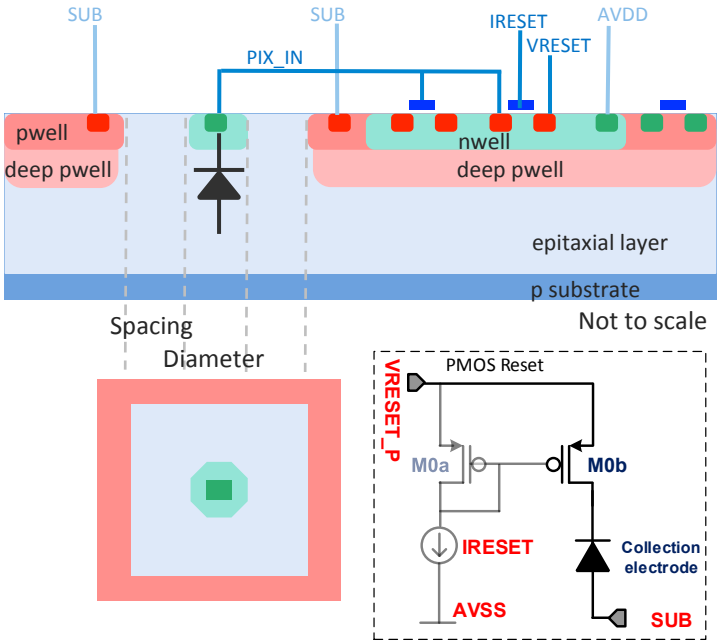
Single pixel variant
All features and optimization

ALPIDE Technology

Pixel Sensor CMOS 180 nm Imaging Process (TowerJazz)

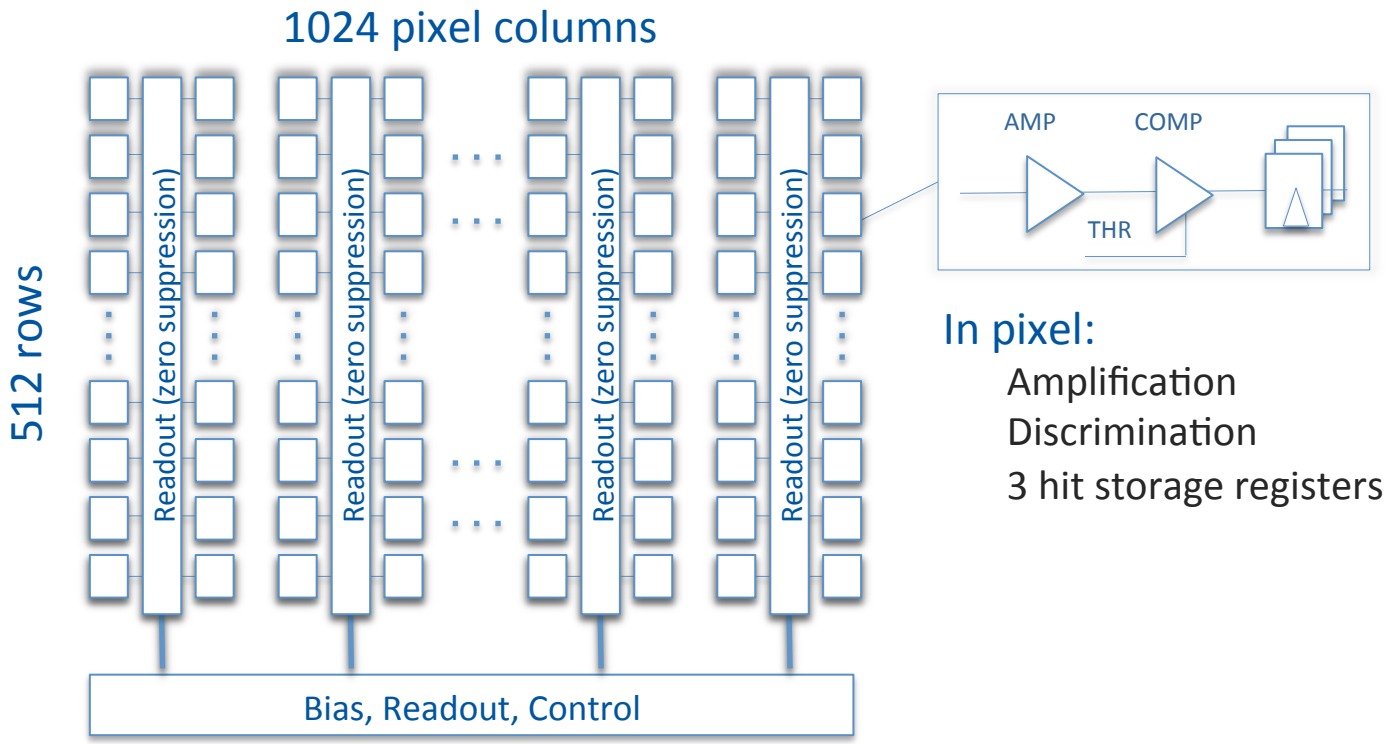
3 nm thin gate oxide, 6 metal layers





- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18 μm to 30 μm) on p-type substrate
- Deep PWELL shielding NWELL allowing PMOS transistors (full CMOS within active area)
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance => large S/N
- Reverse bias can be applied to the substrate to increase the depletion volume around the NWELL collection diode and further reduce sensor capacitance for better analog performance at lower power

ALPIDE Architecture



In pixel:

- Amplification
- Discrimination
- 3 hit storage registers (MEB)

29 μm x 27 μm pixel pitch

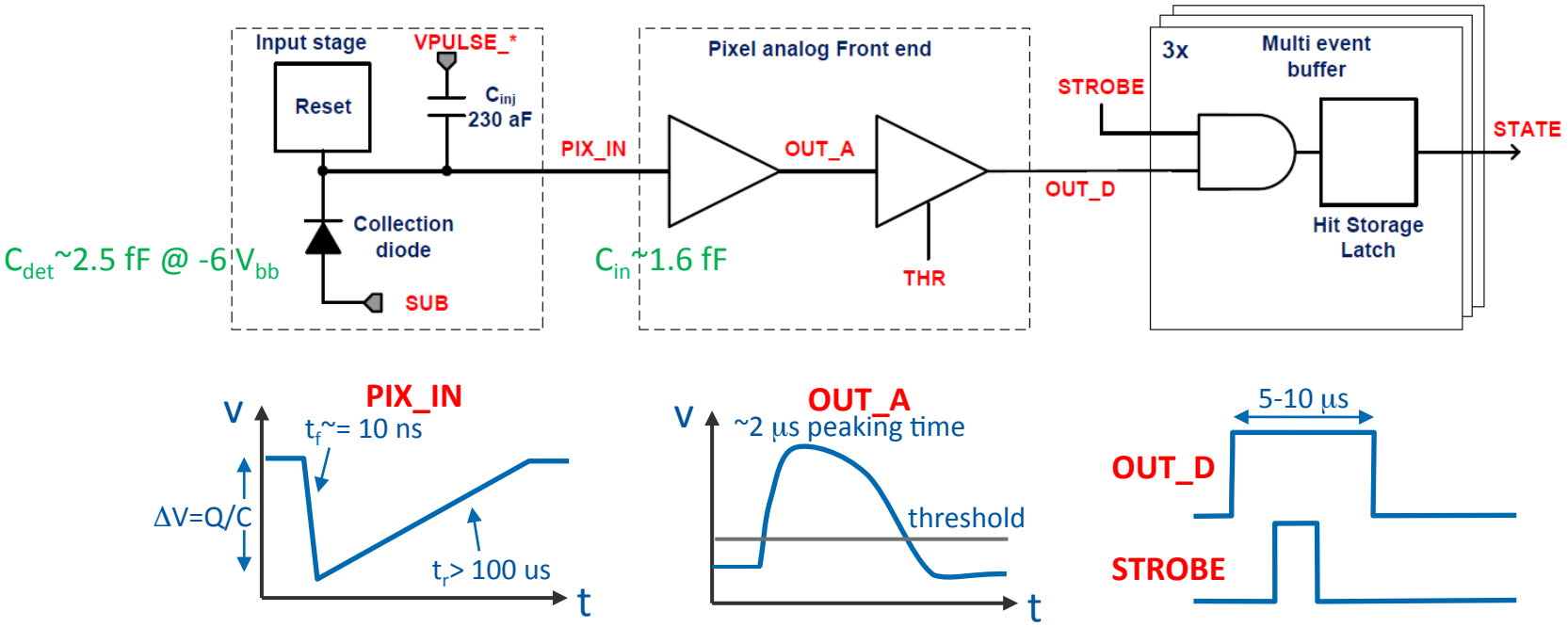
Continuously active front-end

Global shutter

Zero-suppressed matrix readout

Triggered or continuous readout modes

Pixel



Analog front-end and discriminator continuously active

Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel

The front-end acts as analogue delay line

Test pulse charge injection circuitry

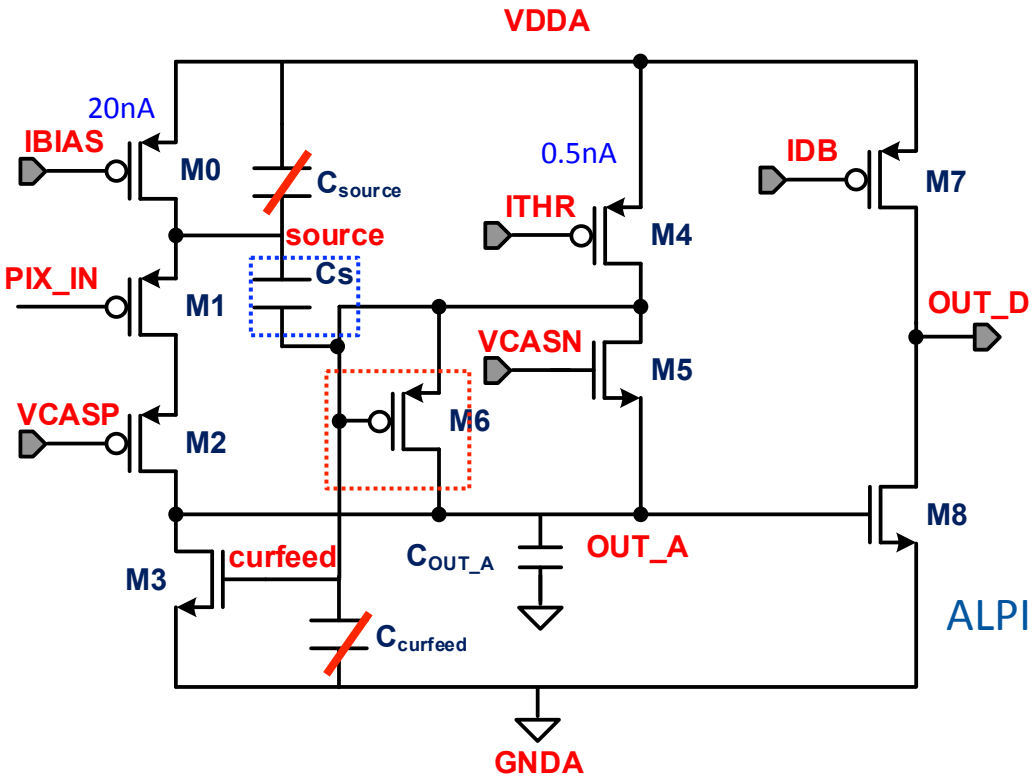
Global threshold for discrimination -> binary pulse OUT_D

Digital pixel circuitry with three hit storage registers (multi event buffer)

Global shutter (STROBE) latches the discriminated hits in next available register

In-Pixel *masking* logic

Front end



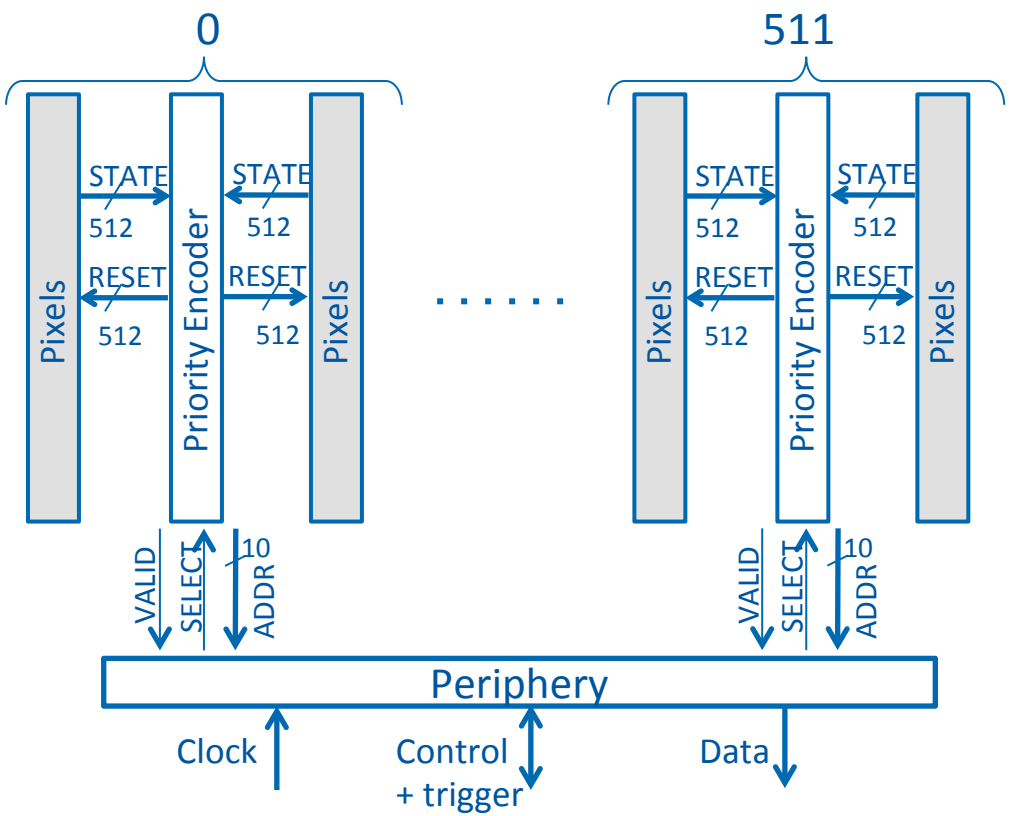
Analog power ~ $(Q/C)^{-2}$ *

*NIM A 731 (2013) 125

ALPIDE front end – D. Kim et al. TWEPP 2015

- Also used with increased current for ATLAS development

Matrix readout

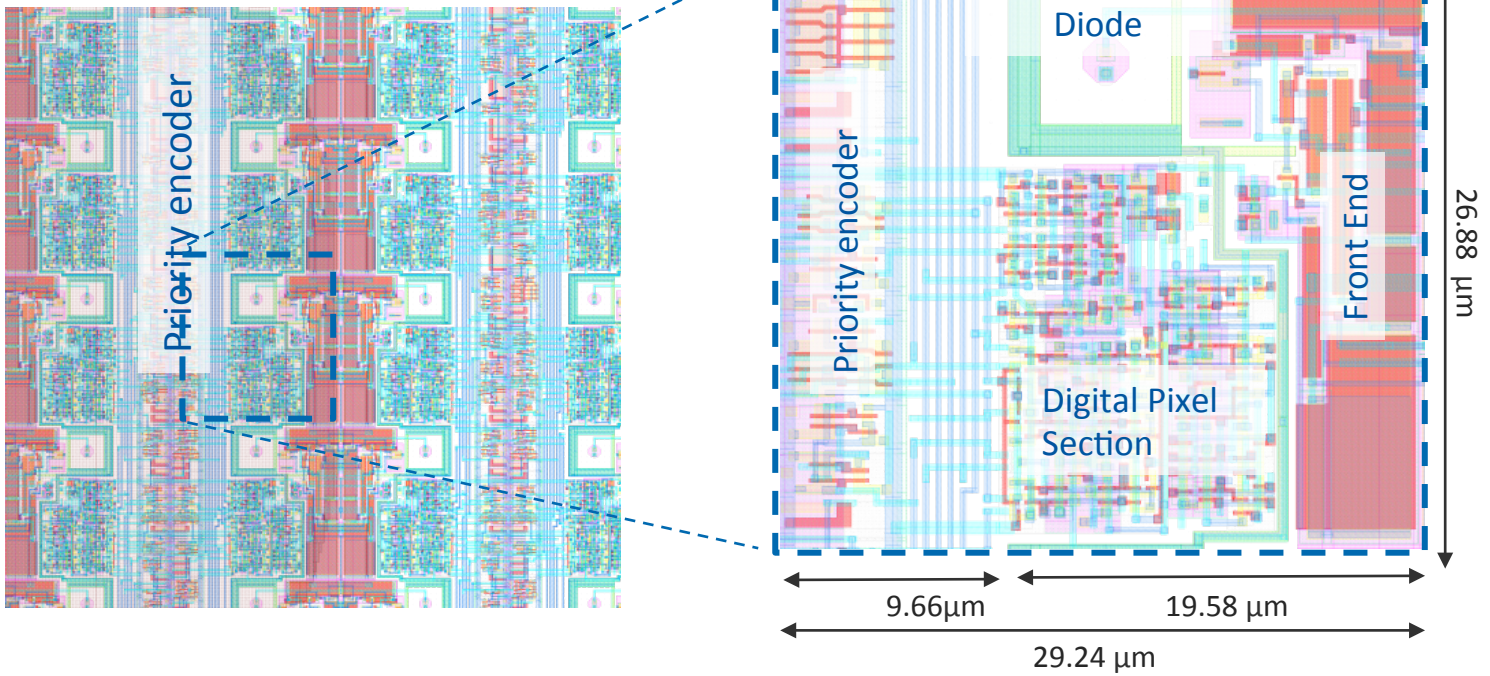


The Priority Encoder sequentially provides the addresses of all hit pixels in a double column

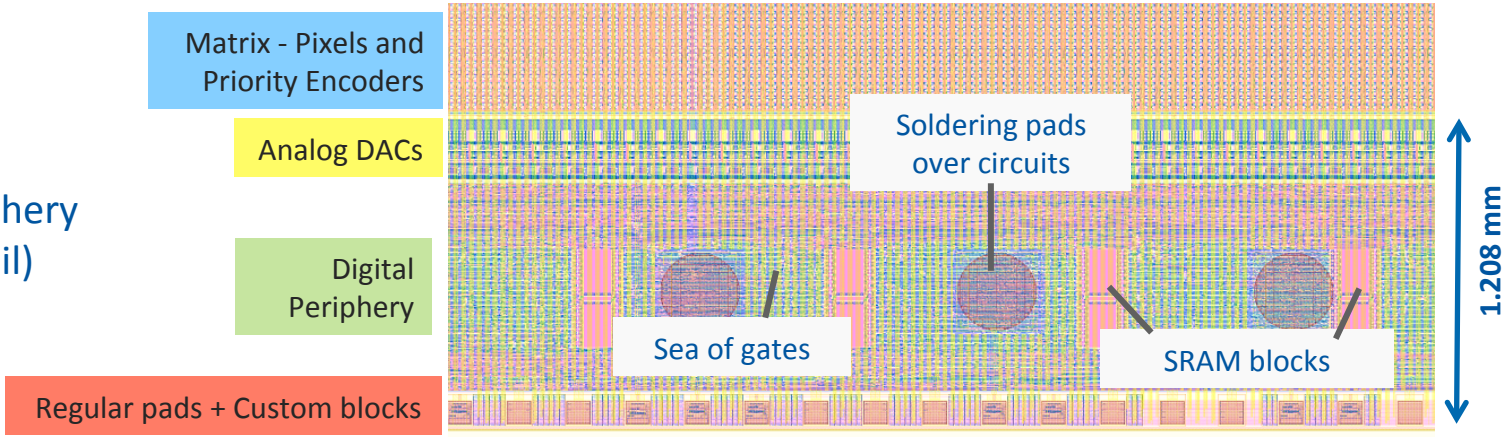
- Combinatorial digital circuit steered by peripheral sequential circuits during readout of a frame
- No free running clock over matrix. No activity if there are no hits
- Energy per hit: E_h ~= 100 pJ -> ~3 mW for nominal occupancy and readout rate
- Buffering and distribution of global signals (STROBE, MEMSEL, PIXEL RESET)

ALPIDE Layout features

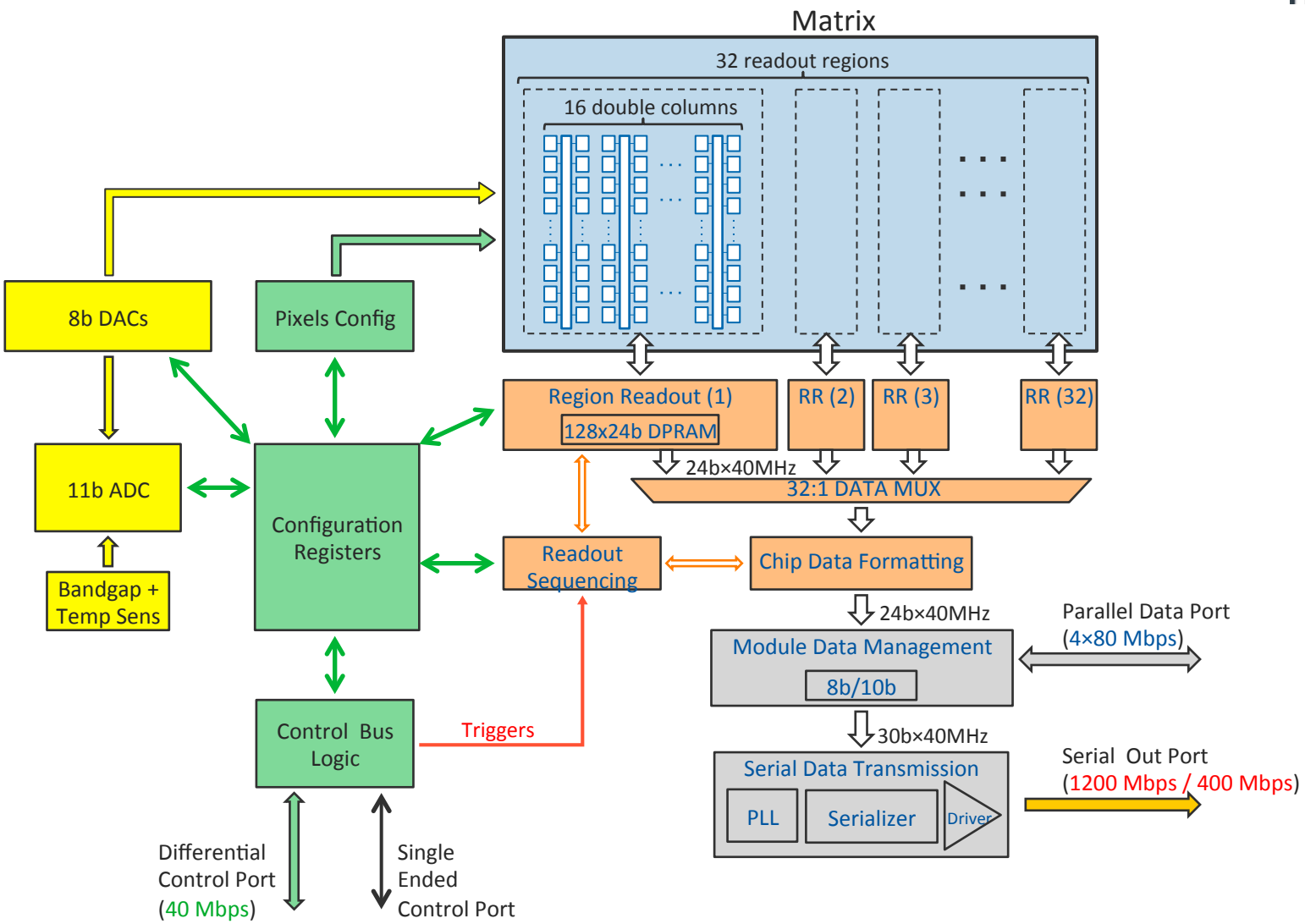
Matrix (detail)



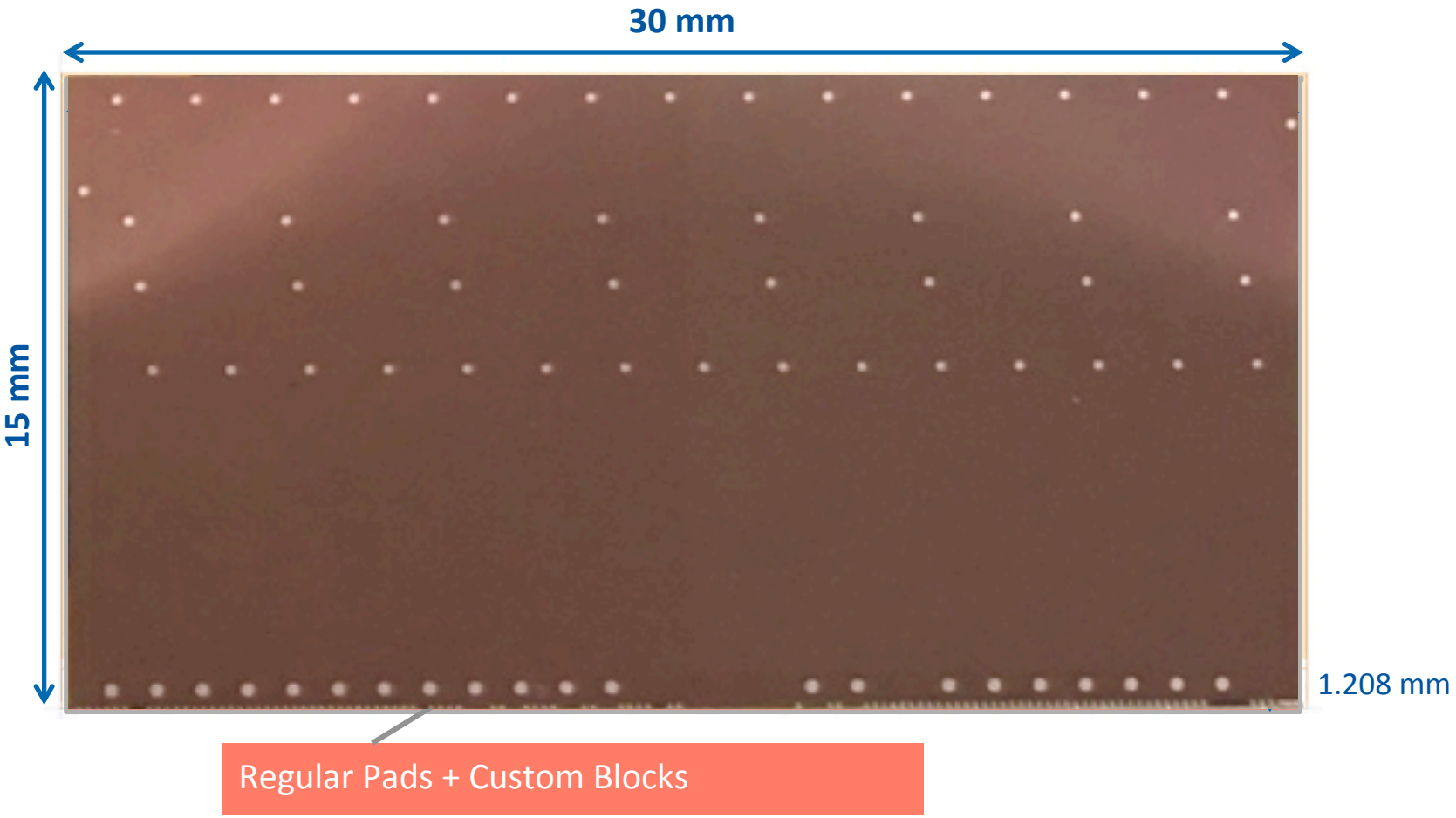
Periphery (detail)



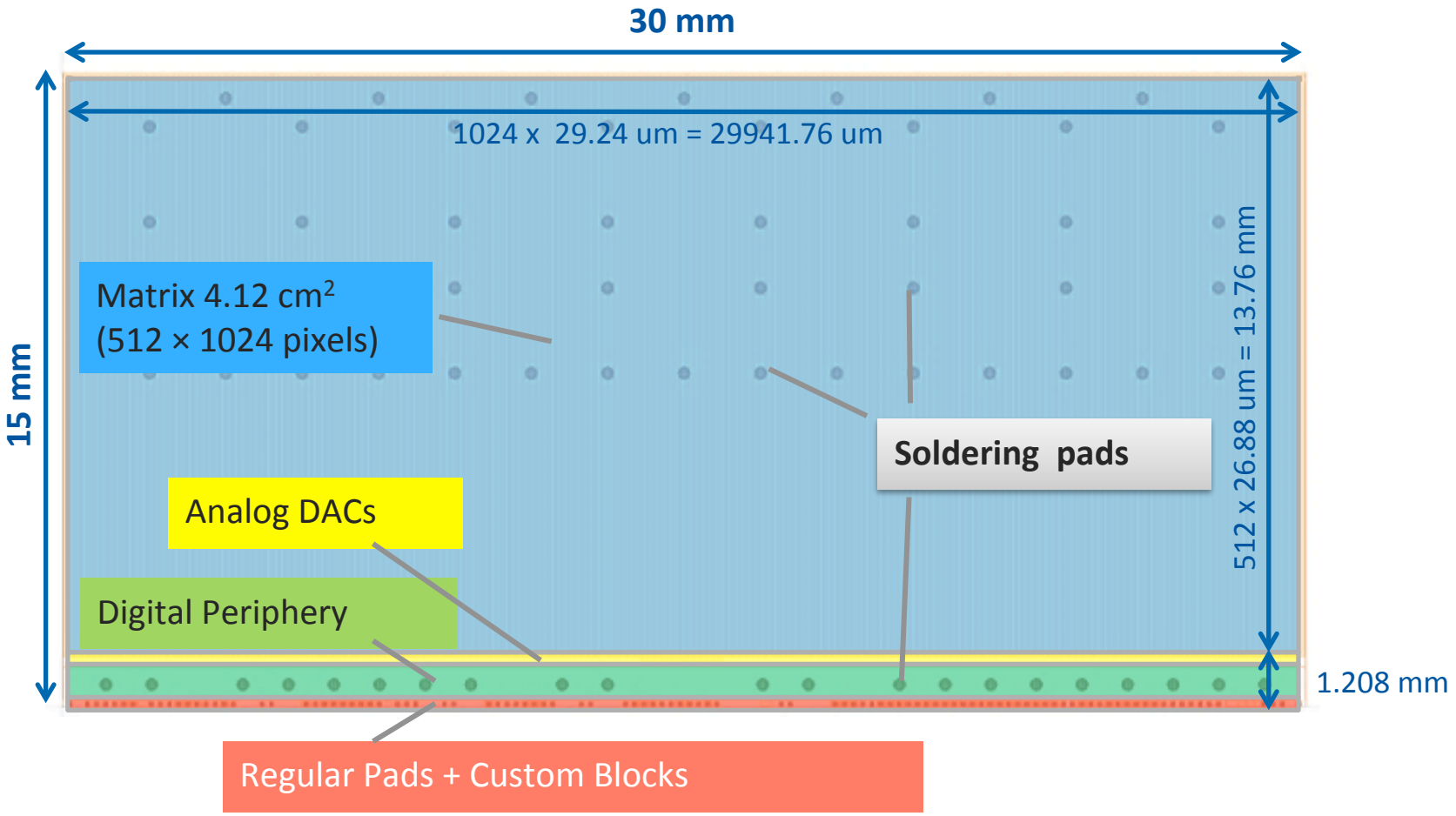
ALPIDE Readout and Control Features



ALPIDE Floorplan



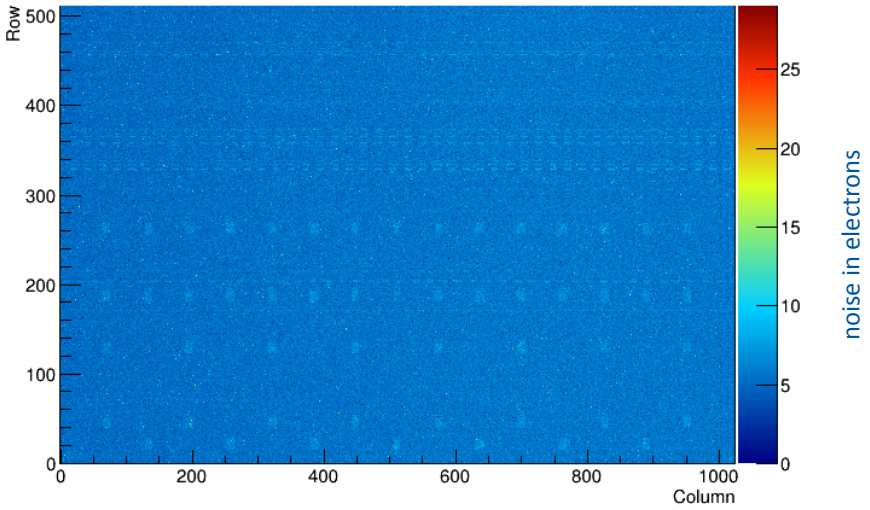
ALPIDE Floorplan

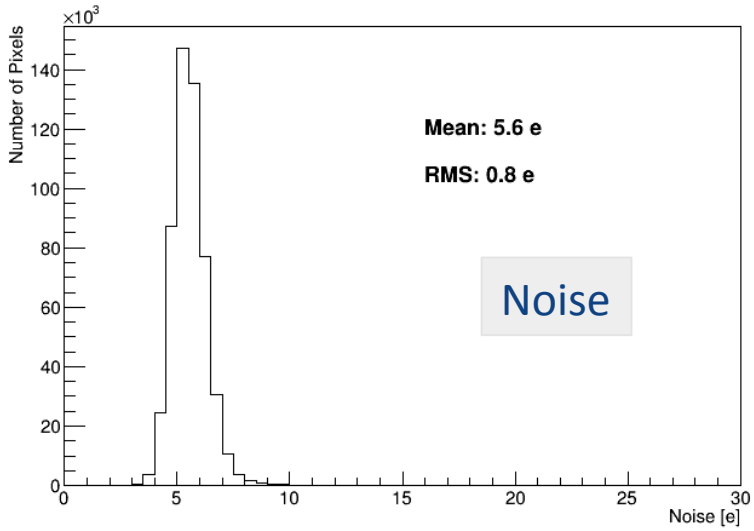


ALPIDE – Some Results

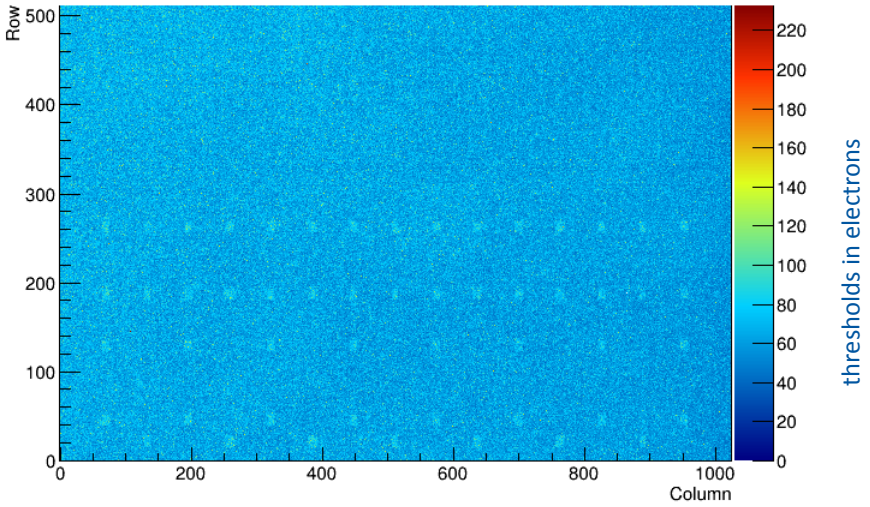
Charge threshold and Noise

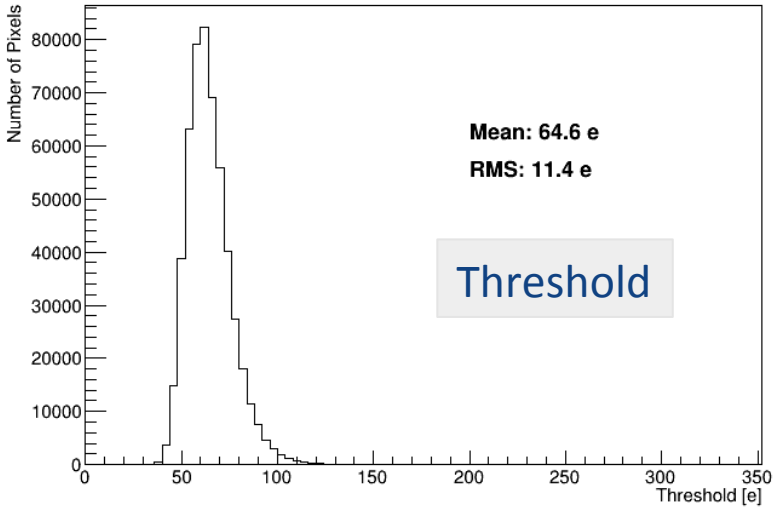
Noise Map



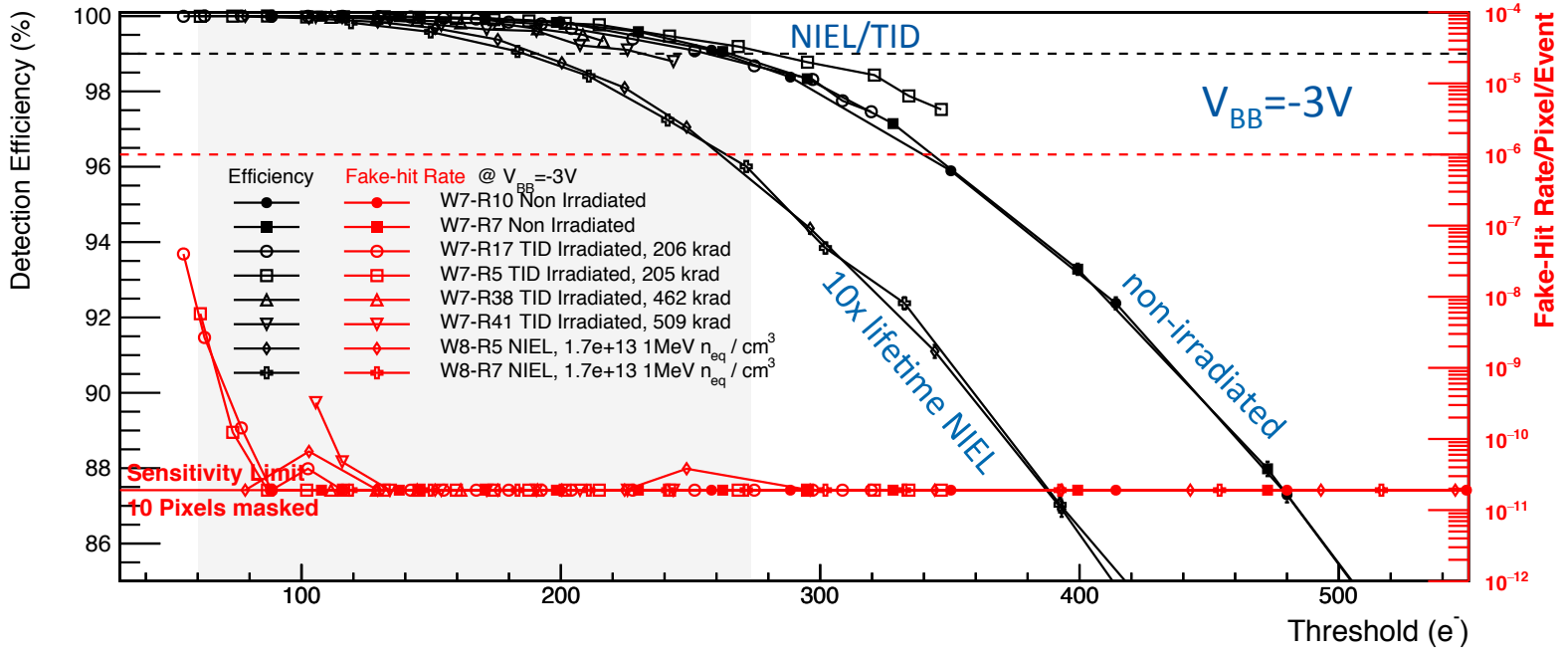


Threshold MAP



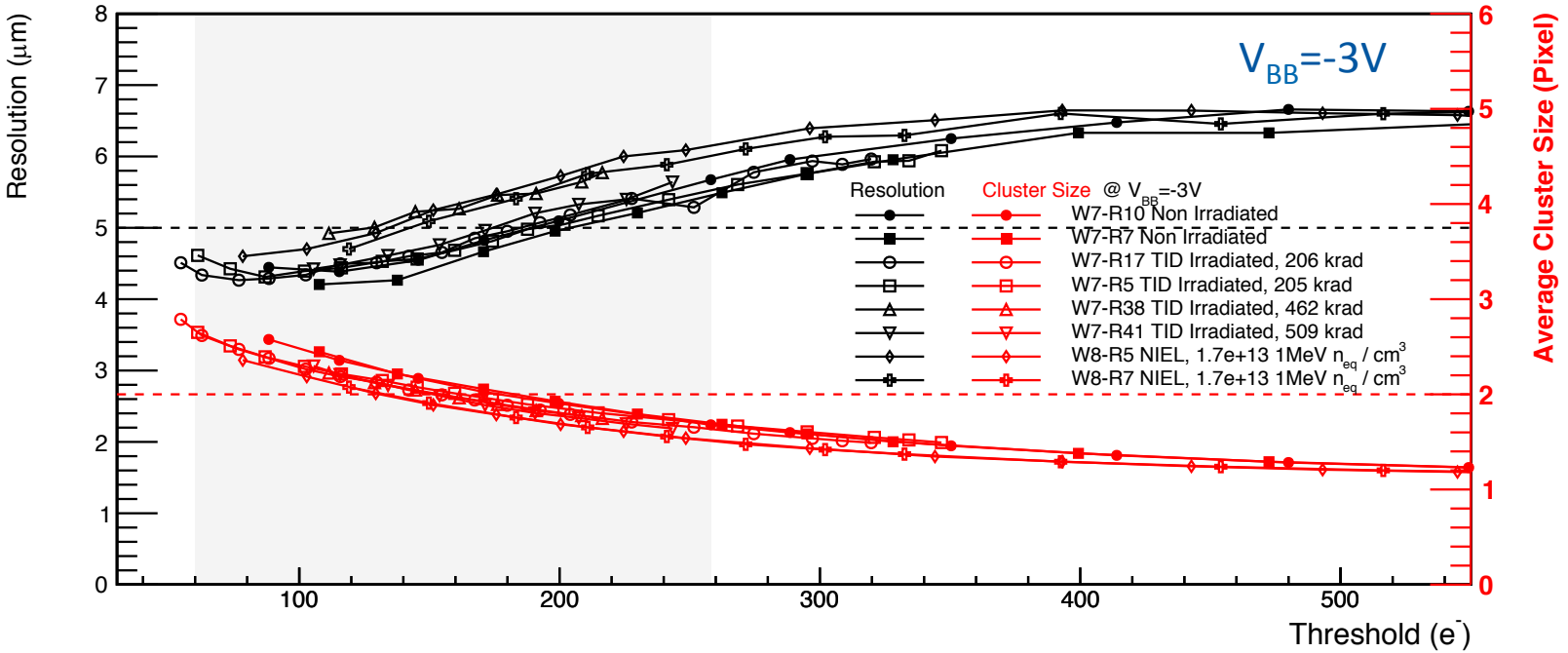


Detection Efficiency and Fake Hit Rate



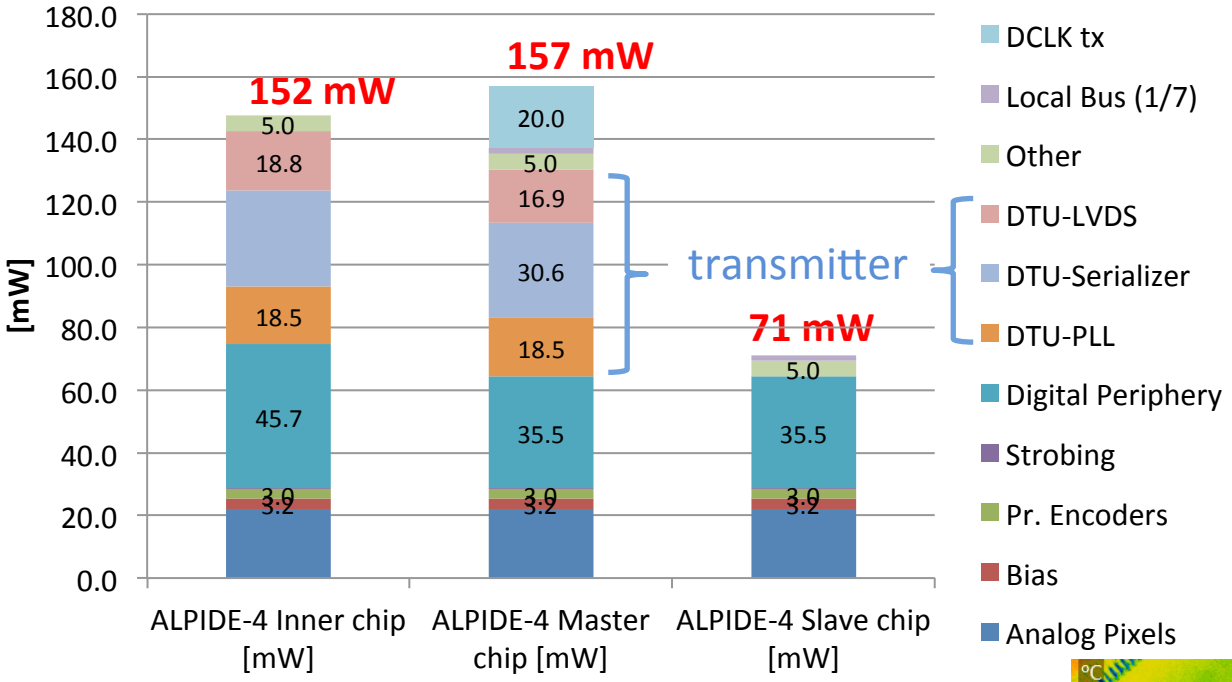
- Large operational margin with only 10 masked pixels (0.002%)
- Chip-to-chip fluctuations negligible
- Non-irradiated and NIEL/TID chips show similar performance
- Sufficient operational margin after 10x lifetime NIEL dose

Position resolution and cluster size



- Chip-to-chip fluctuations negligible
- Non-irradiated and TID/NIEL chips show similar performance
- Resolution of about 6µm at a threshold of 300 electrons
- Sufficient operational margin even after 10x lifetime NIEL dose

ALPIDE Power consumption



Sensitive area: 4.12 cm^2

Inner Barrel: 36.9 mW/cm^2

Outer Barrel: 20.2 mW/cm^2

In the matrix:

(analog + digital)/area

(22.2 + 3.2)/4.12

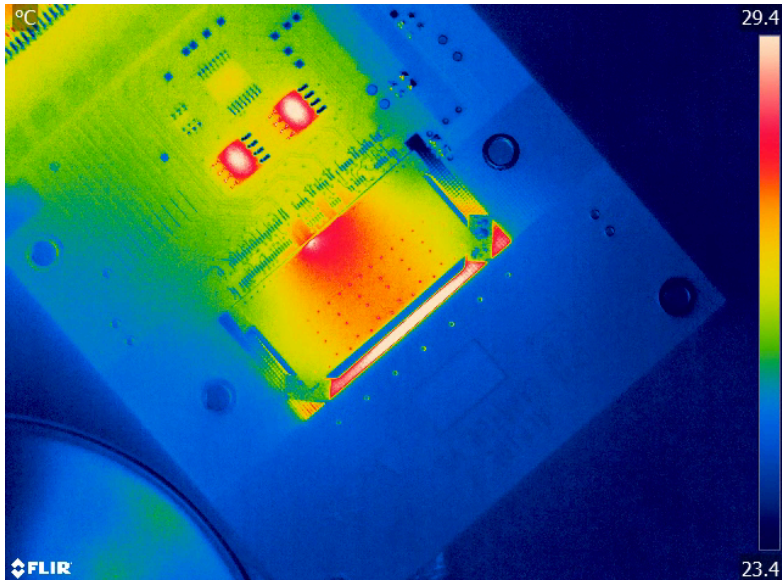
= 6.2 mW/cm^2

With 40 nW front-end and Q/C ≈ 80 mV analog power consumption still dominant within the matrix

Matrix readout only active if hit present

Clock gating in the digital periphery

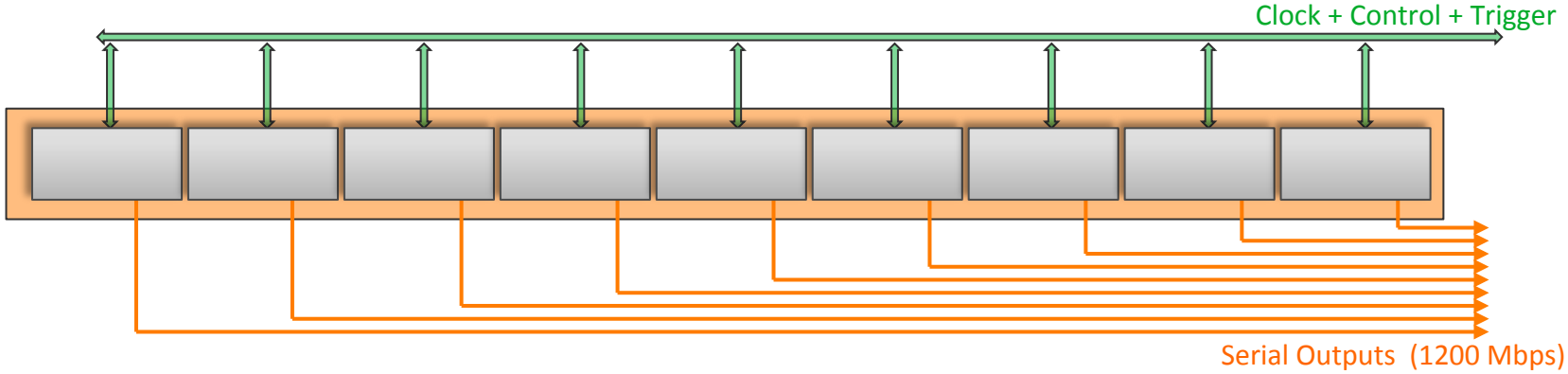
For the future more work needed on Q/C, architecture periphery and transmitter for overall power consumption



walter.snoeys@cern.ch

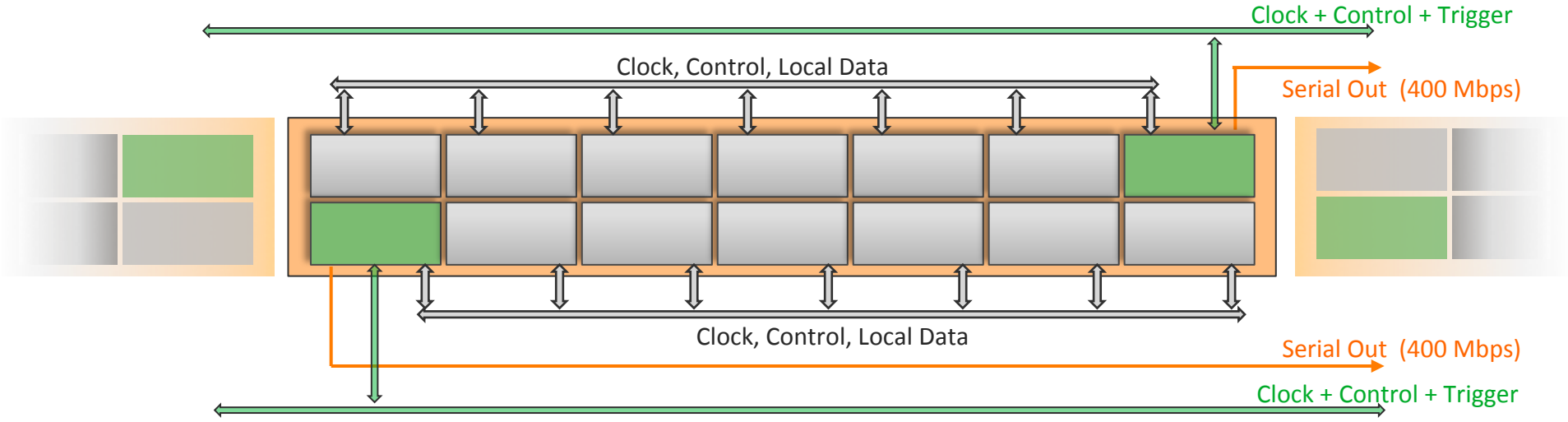
Detector Modules with ALPIDE Chips

ITS Inner Barrel Module – 9 chips, common clock and control, independent data lines



ITS Outer Barrel Module – 2 groups of chips, Master + 6 Slaves

Only the Master interfaces to the external world and bridges control and data transfer

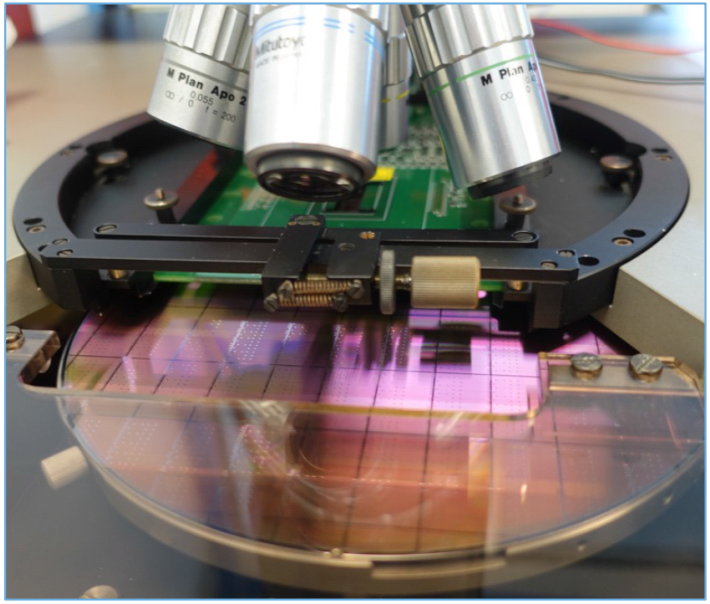


ALPIDE & ITS Upgrade status

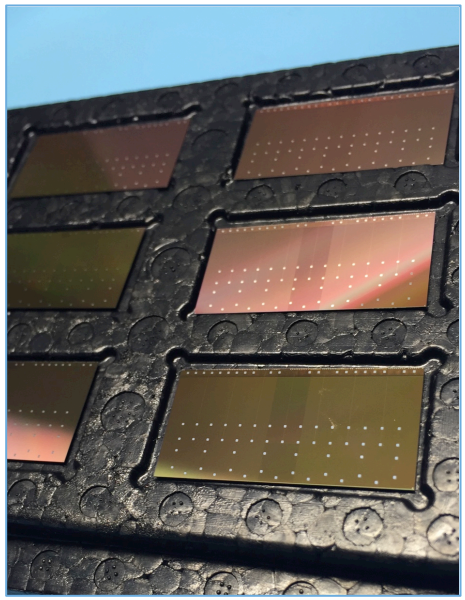
ALPIDE – production readiness review 25/11/2016

Production now launched

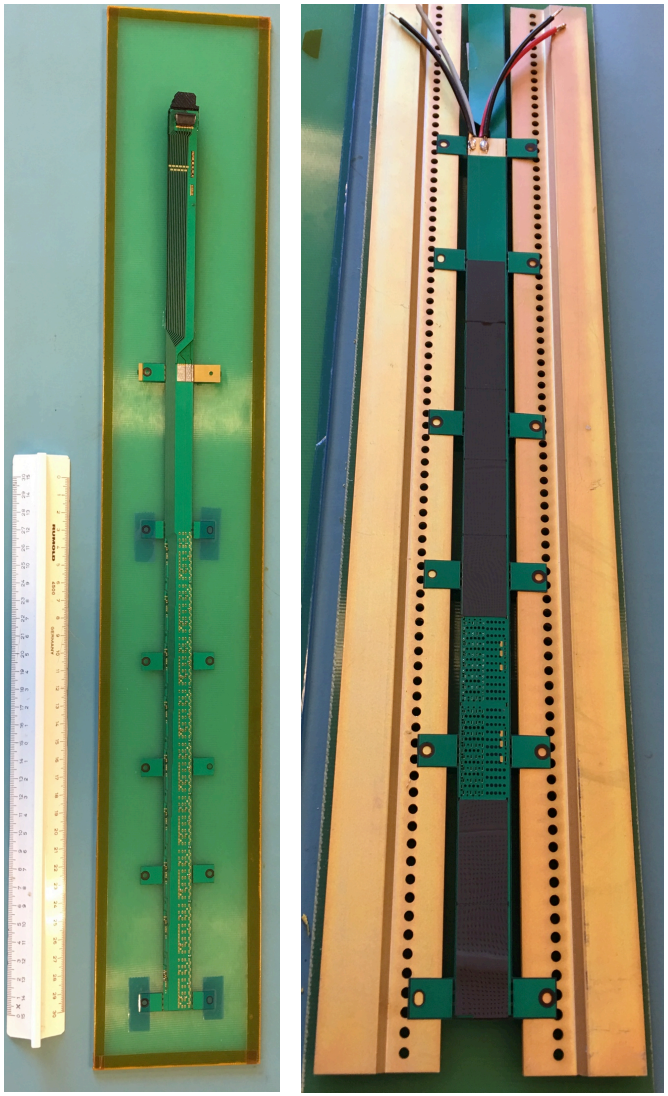
Wafer probe testing



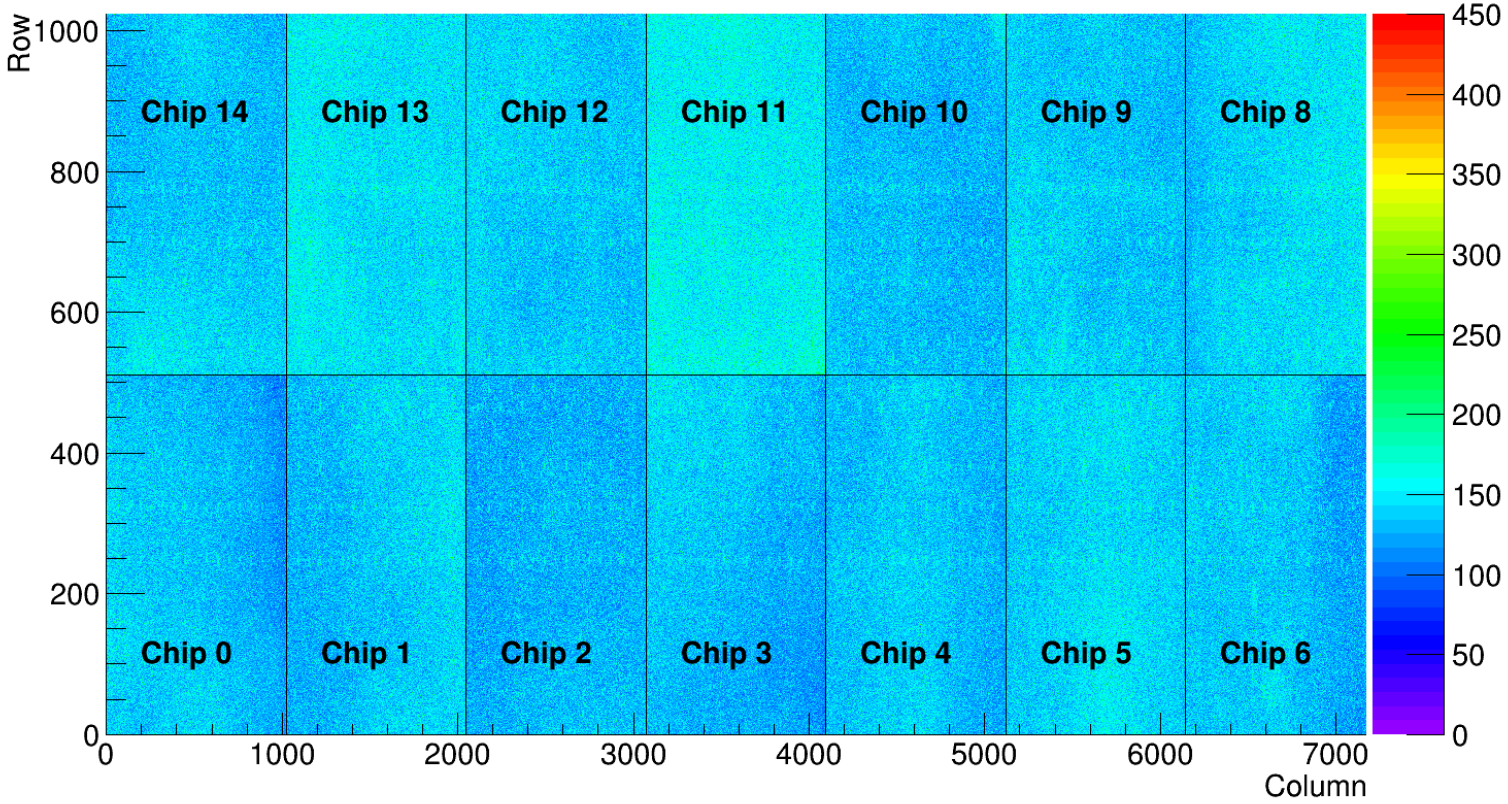
Single chips after thinning & dicing



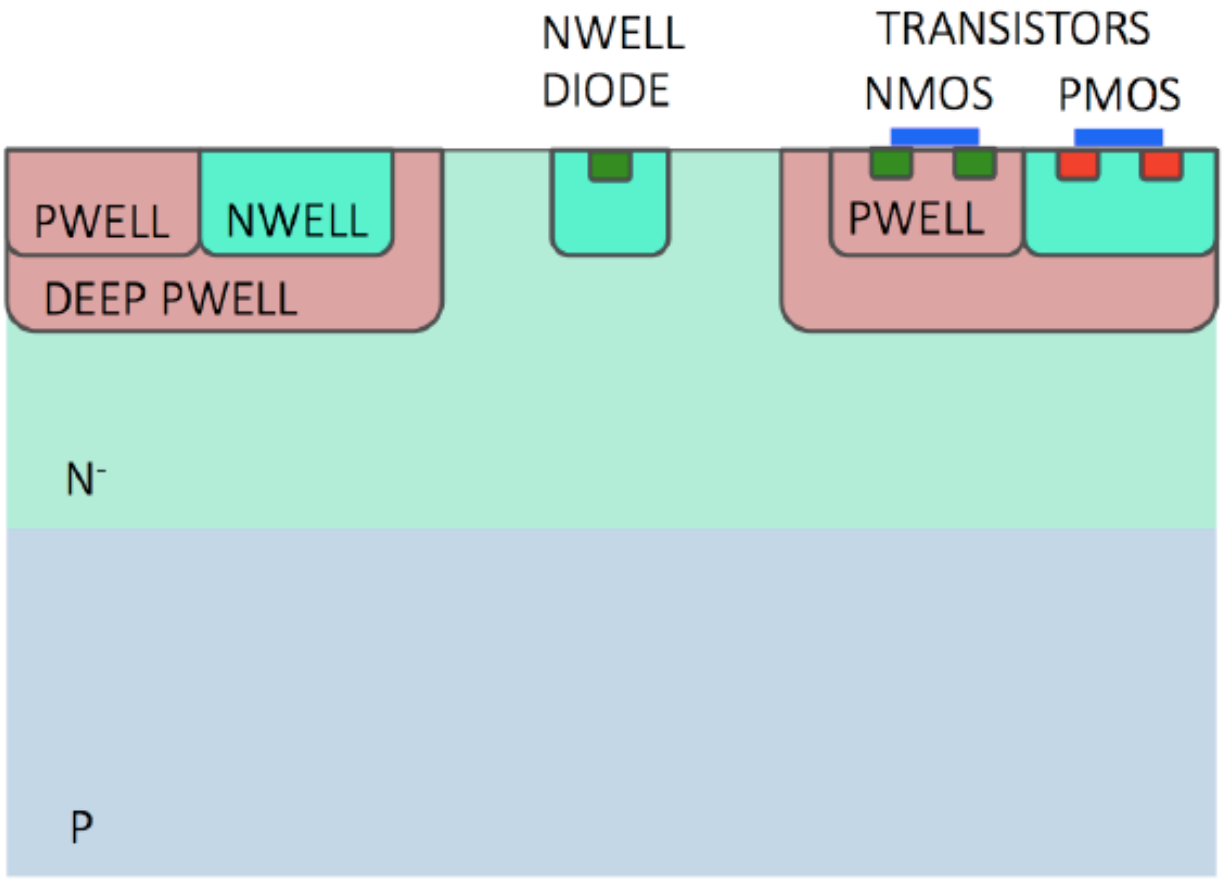
Inner Barrel Module (9 chips)



Threshold scan on Outer Barrel Module

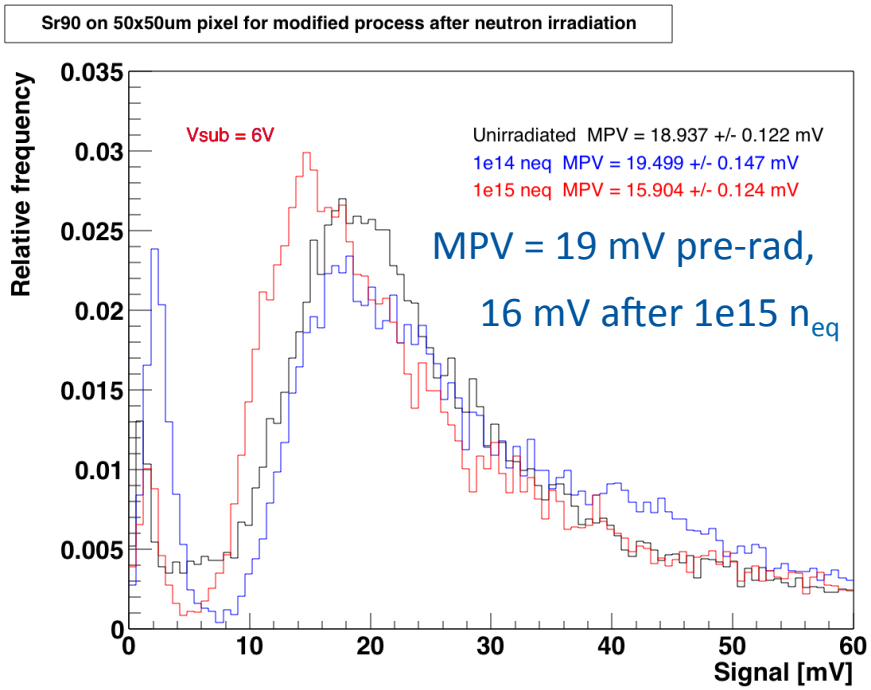


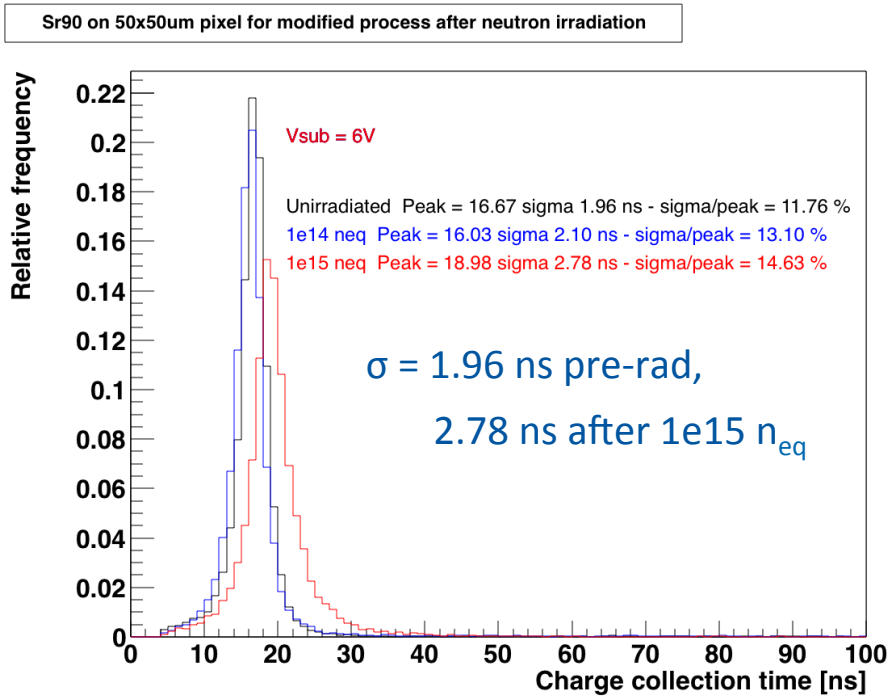
Process modification for radiation tolerance



Planar junction across the pixel => full lateral depletion

Measurement results after irradiation





Courtesy H. Pernegger et al.

Results on detection efficiency after irradiation (1e15 n_{eq}/cm^2) also encouraging

Initiated development for the ATLAS ITK involving several groups

-> see H. Pernegger's presentation

CMOS Sensor submission in TowerJazz for ATLAS

- Two large chips
  - MALTA (Monolithic Sensor from ALICE To ATLAS) (CERN) (2 cm x 2 cm)
  - MONOPIX (Bonn U. + CERN) (2 cm x 1 cm)
- Investigator (sensor test structures)
- Transistor test structures
- LVDS chip
- Sensor test structure (RAL)
- …

CERN (& MIND) design team:
I. Berdalovic, B. Blochet, R. Cardella, N. Egidos Plaja, T. Kugathasan, C.A. Marin Tobon, H. Mugnier, J. Rousset, W. Snoeys

Bonn design team:
T. Wang, T. Hemperek, K. Moustakas, H. Krueger

Several groups participate in measurements (Ljubljana, Glasgow, CERN …) – Thank you !

Summary

ALPIDE CMOS Pixel Sensor Chip for the ALICE ITS upgrade now in production

Used also for the new Muon Forward Tracker (MFT) detector

Key features

15 mm × 30 mm, 512 × 1024 pixels, 29 μm x 27 μm pitch

High resistivity epitaxial layer, deep pwell, reverse bias

40nW analog front-end, in-pixel discrimination and multi-event buffer

Global Shutter (<10 us). Triggered or Continuous readout modes

Versatile interfaces and features for the integration of multi-chip modules

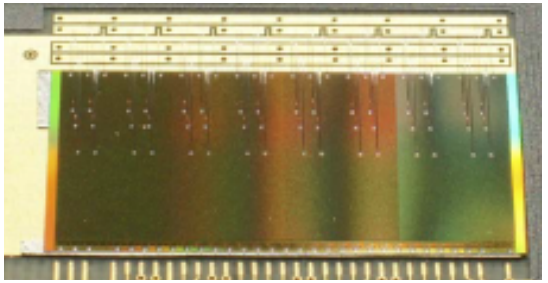
Power density < 35 mW/cm^2 (<20 mW/cm^2 with readout from parallel port)

Performance of full-scale prototypes in test beams

Detection Efficiency > 99%

Fake hit rate << 10^{-5} /event/pixel

Position resolution < 5 μm



Starting point for ATLAS development after first results of the process modification

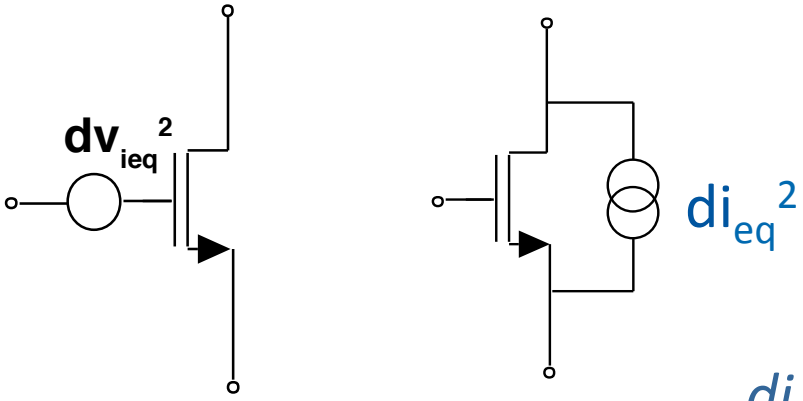
See H. Pernegger's presentation

THANK YOU !

Backup

Analog Power Consumption:
Noise sources in a FET

EQUIVALENT WITH :



WHERE:

$$di_{eq}^2 = g_m^2 dv_{eq}^2$$

In weak inversion (WI): $g_m \sim I$

$$dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 2kTn/g_m)df$$

In strong inversion (SI) $g_m \sim \sqrt{I}$

$$dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 4kT\gamma/g_m)df$$

Transconductance gm related to power consumption