Pixel detectors for HL-LHC upgrades
-
Pixel Technologies: Hybrid Pixel

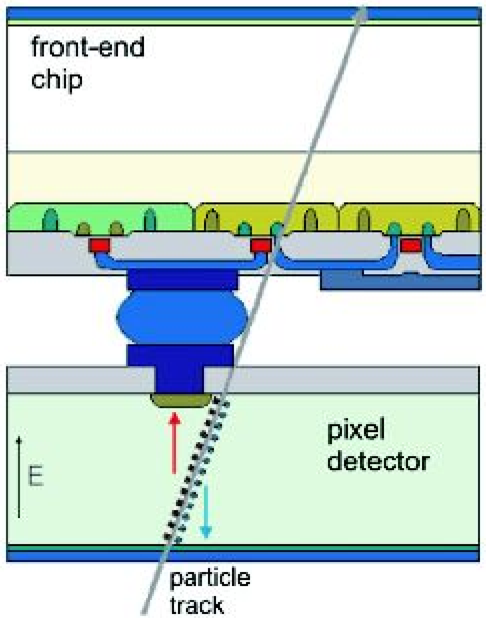
10th Terascale Detector Workshop

12.04.2017

Susanne Kühn, CERN

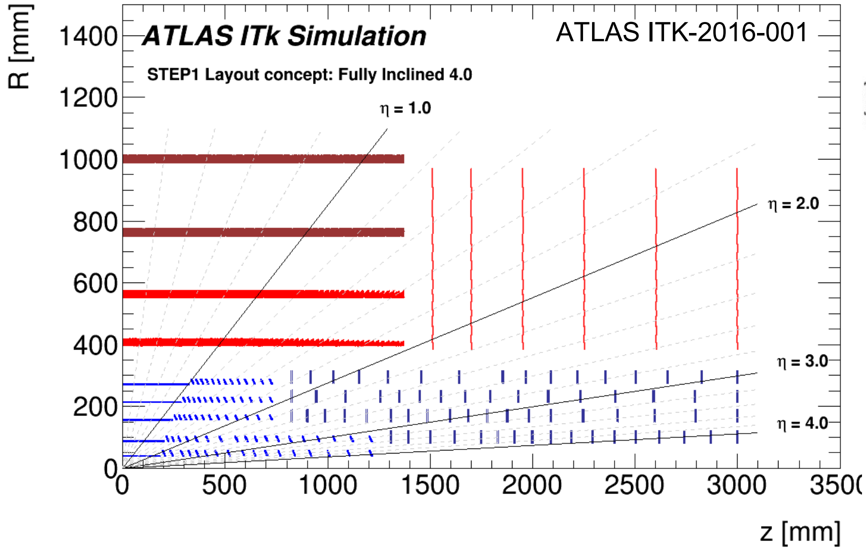
Overview

- Pixel modules for the tracker upgrades
  - Challenges
  - Concept of hybrid modules
- Results for sensor options
  - Planar p-type sensors
  - 3D sensors
- Challenges for hybrid modules
  - HV protection for n-in-p sensors
  - Interconnection: bump-bonding
- Summary



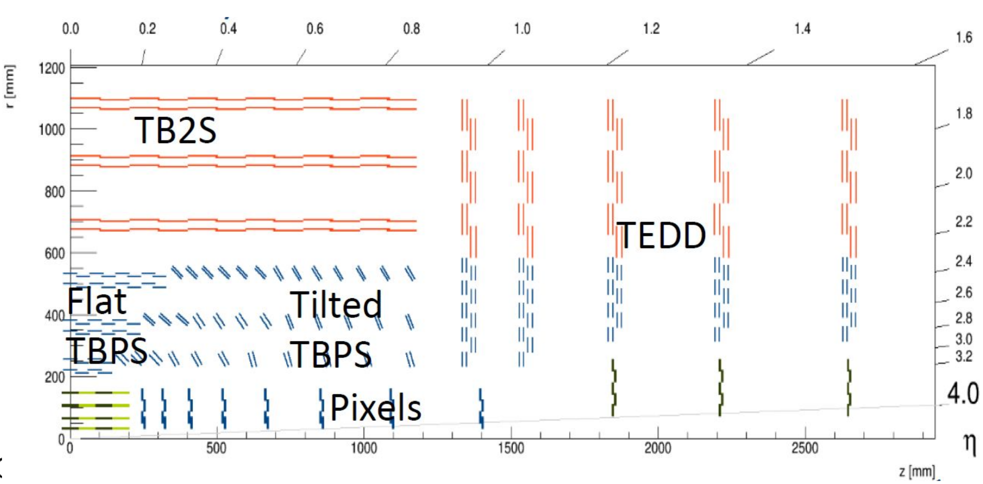
Upgrade of the ATLAS and CMS tracker

For ATLAS various layouts under evaluation for pixel detector



CMS tilted layout

G. Steinbrück, VERTEX 2016



Challenges for pixel modules

See talk by Loddo Flavio on RD53 Pixel Asic

→ Fast, radiation-hard sensors, readout chips, support materials

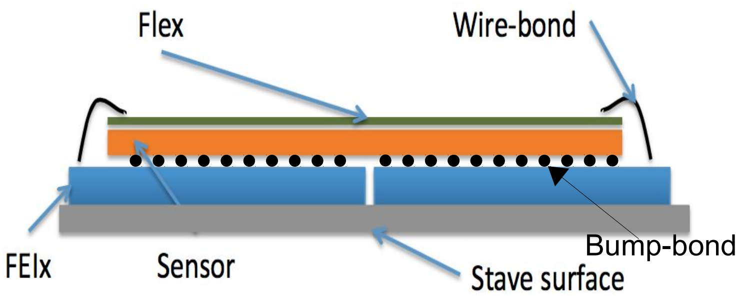
→ Silicon detector modules to be assembled and placed on larger structures

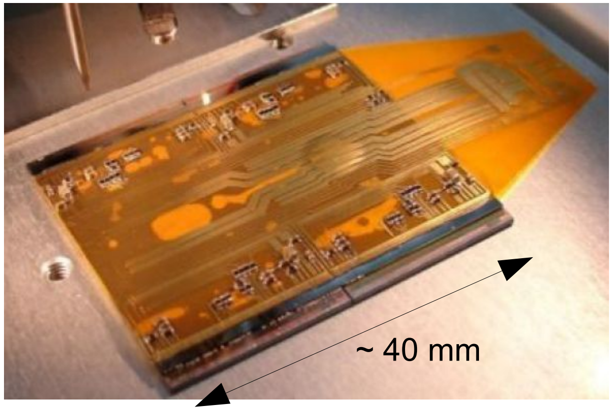
→ In ATLAS: 5 barrel layers, many rings in end-cap (~ 13 m²), various module geometries, production volume of up to 13000 pixel modules

→ In CMS: 4 barrel layers, 7 disks (~ 4.9 m²), minimal number of module types, 1960 2x1 and 2392 2x2 ROCs/module with typical size of a ROC 2x2 cm²

Hybrid pixel module concept

- For ATLAS
  - Sensor and front-end electronics connected to module with high density bump bonding → bare module
  - Flex glued on top of bare module (on sensor side)
  - Flex and bare module connected via wire-bonds (data, LV, HV)
  - Quad (4-chip) modules and single, double modules for inner most layers
- Prototyping of different assembly methods in several institutes ongoing
  - Based on FE-i4 and various sensor options
  - Assembly of bare module and readout flex advanced
  - Irradiation study of glues and composite materials started





Quad pixel module prototype, 4 FEi4 chips

Sensor options

- Various sensor types foreseen:
  - ATLAS: 3D inner layer, planar baseline for other layers, CMOS technologies under evaluation
  - CMS: planar baseline, 3D or planar sensors for 1st layer under evaluation

See talk by Heinz Pernegger on CMOS

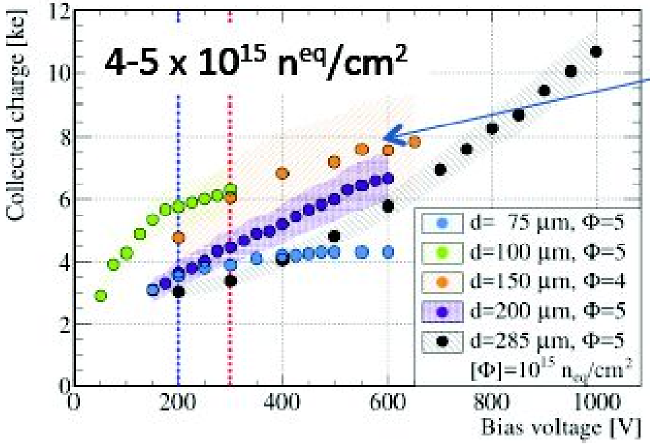
- Thickness: thin sensors
  - ATLAS: depending on radius 100 μm, 150μm, 200 μm
  - CMS: thin sensors under study
- Thin/active edges
- Small pixel sizes
  - 50x50 μm^2 or 25x100 μm^2

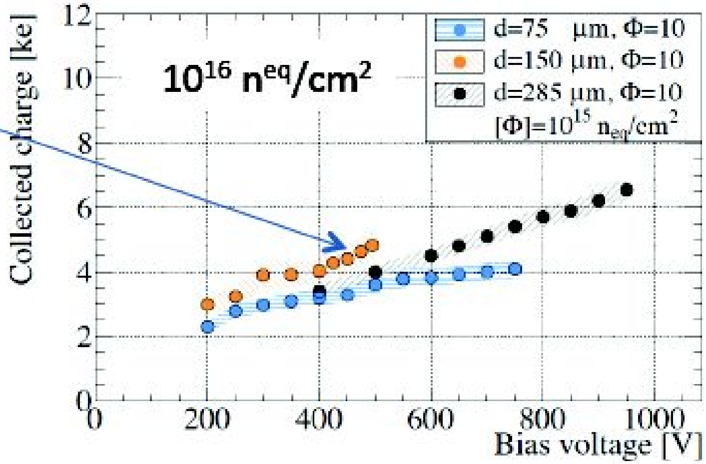
→ Many performance studies in laboratory and test beam before and after irradiation

Planar sensors in ATLAS: thickness

•Thin n-in-p sensors after neutron irradiation to high fluences

Terzo, Andricek, Macchiolo, Nisius et al, JINST 9 (2014) C05023

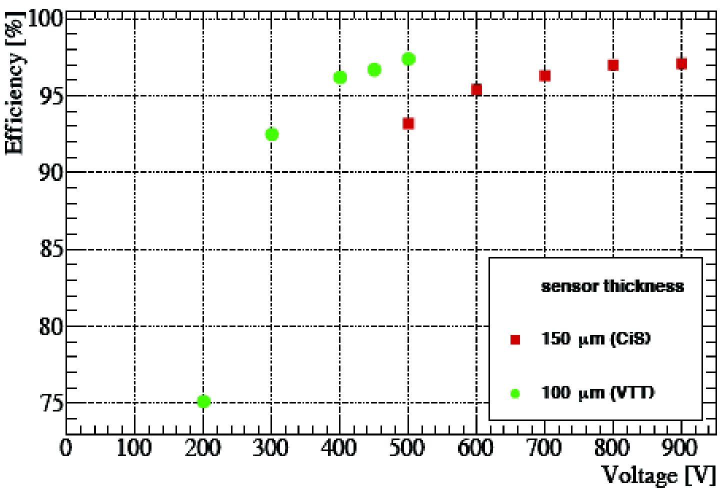




- **6000 – 7000 e-**
  for 100 - 200 μm sensors @ 300 V – 600 V bias

- hit efficiencies still reasonable at Φ > 10^{16}

A. Macchiolo



CiS sensors after 1x10^{16} neq/cm²

Next: Need 50x50 μm² chip to investigate hit efficiency after irradiation

Planar sensors in ATLAS: slim edge

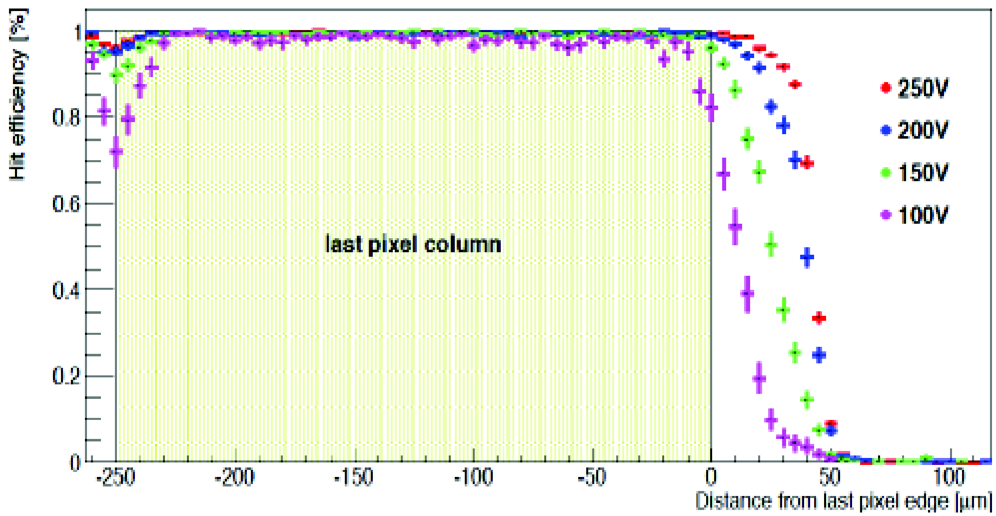
- Slim edge sensor, 150 µm thin, irradiated to $1x10^{15}$ neq/cm²

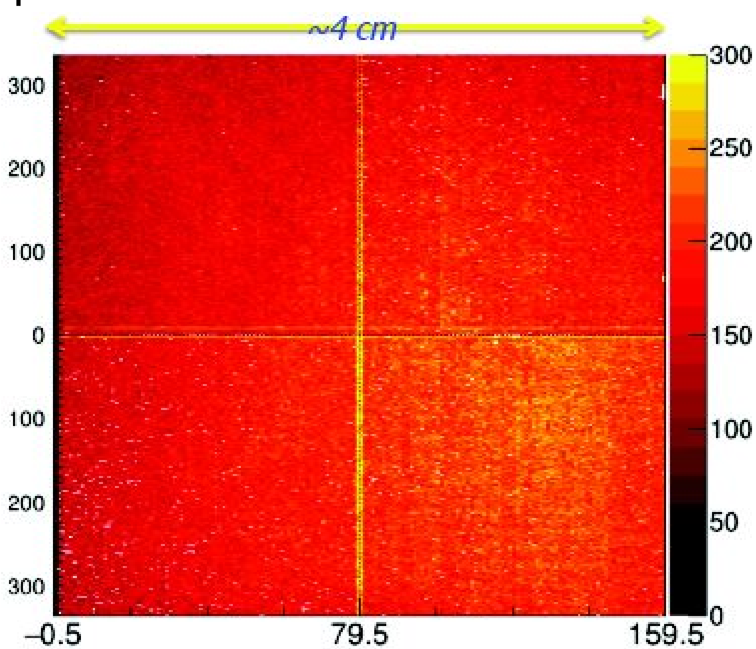
  → high efficiency at edges

- Quad module HPK sensor 100 µm with RD53-P2 front-end in test

- RD53A compatible sensors already produced

A. Macchiolo

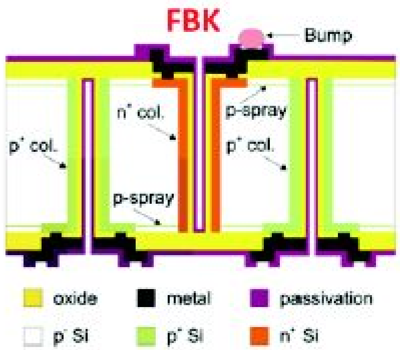




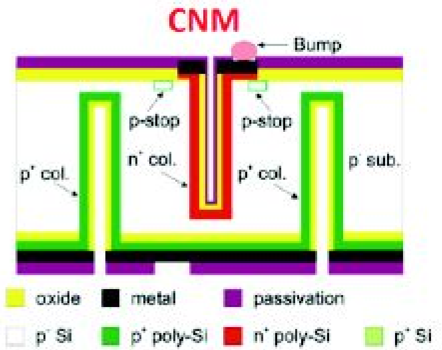
- From the experience with recent productions, a good yield is achievable with sensors of 100 µm thickness and above
- Baseline thin p-type sensors (6” production) with 100 µm and 150-200 µm thickness
- Power dissipation (in range 500 -700 V) about 25-45 mW/cm²

3D sensors in ATLAS

- 3D sensor technology has been proven to be reliable with the IBL detector and more recently in AFP and PPS

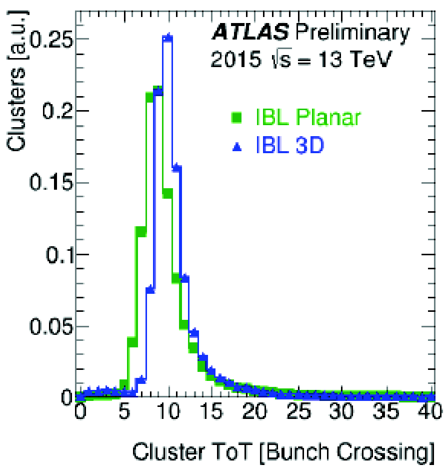


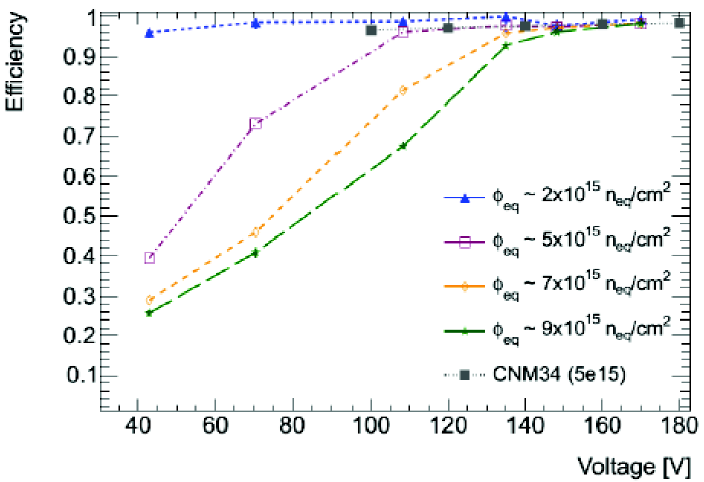
G.F. Della Betta et al.,
PoS Vertex2012 (2013) 014



G. Pellegrini et al..
NIM A731 (2013) 198-200

S. Parker, NIM A 395 (1997) 328-343



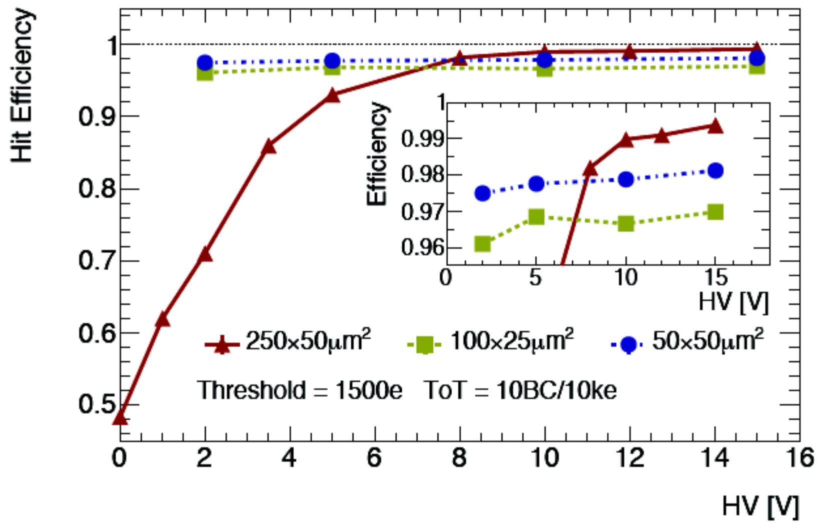


ε=97% at 170V for fluence $1\times10^{16}\ n_{eq}/cm^2$
*power dissipation of **11** mW/cm^2 at -25C*

3D sensors in ATLAS ctd'

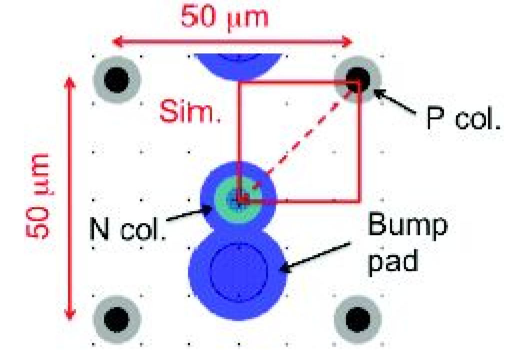
- New thin 3D pixel sensors on 6” p-type wafers at FBK
  – 250x50 µm² (2E), 50x50 µm² (1E), 100x25 µm² (1E)

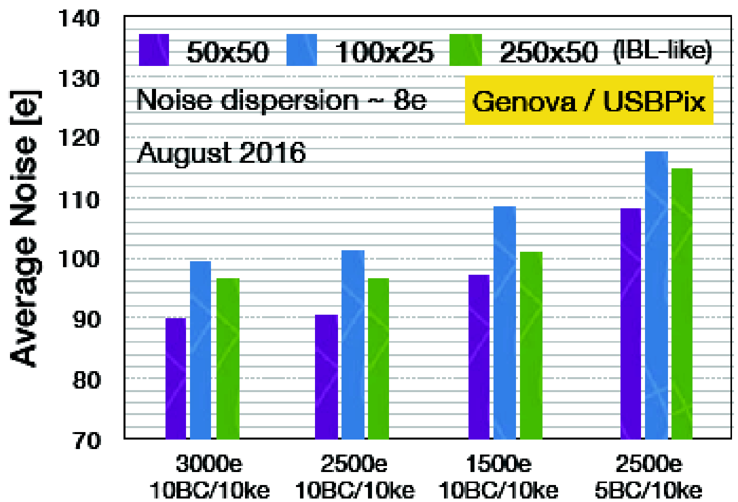
H. Oide



High efficiency before irradiation

Clustering relevant





Radiation hardness at low operational voltages and moderate temperatures with low power dissipation

→ Baseline for the innermost layers

Planar sensor study in CMS

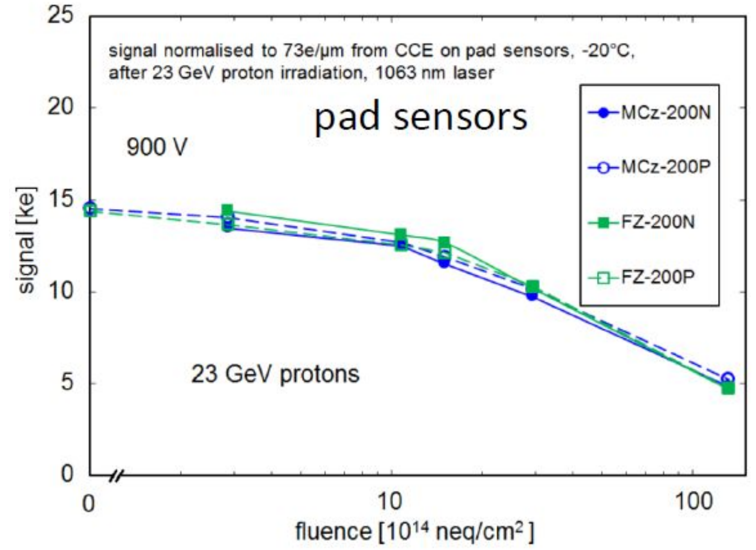
- Charge collection studied for irradiated 200 μm thick n-in-p pad diodes
  - 5k electrons after1x10^{16} neq/cm² (900 V bias)

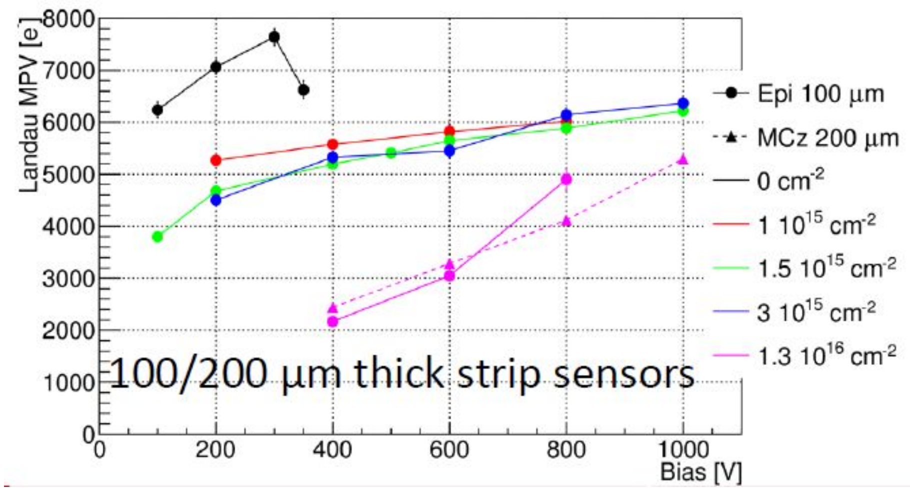
Thin sensors:

- Similar signal in 100 μm epi strip sensors as in 200 μm (MCz: 5 k electrons at ~800 V)
- However: Strong increase of current and noise with voltage, signs of soft breakdown/ charge multiplication
- Charge collection measurements repeated with pixel sensors: Weighting field

→ HPK submission

→ INFN/FBK submission

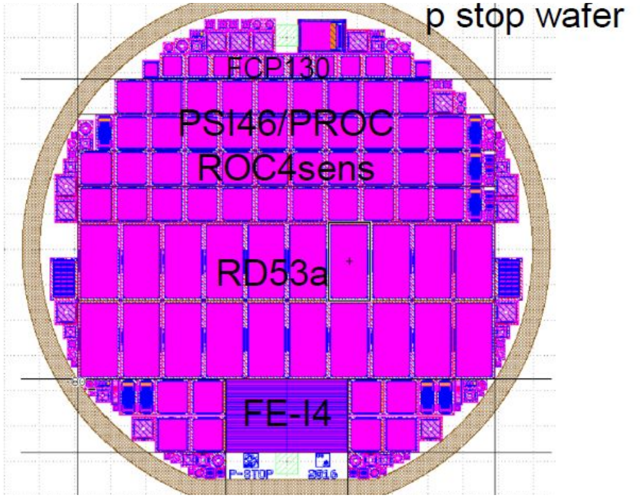


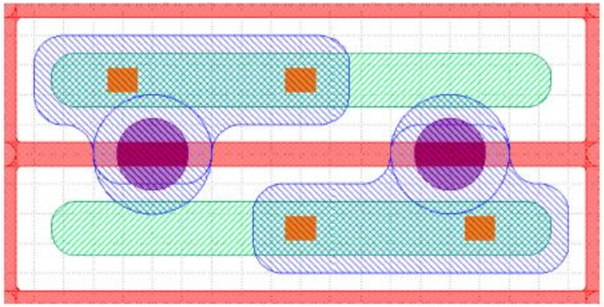


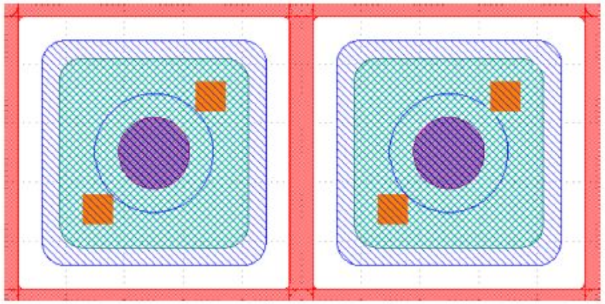
CMS HPK planar sensor study

G. Steinbrück

- HPK submission on 6” n-in-p wafers
  - 35 wafers, 3 materials
    - 150 µm, no handle wafer
    - 150 µm + 50 µm Si-Si direct bond
    - Deep diffused 150 µm + 50 µm
    - P-stop and p-spray isolation (only dir. bond)
  - Pixel size 50x50 µm² and 25x100 µm²
  - Bias schemes: no bias, common punch-through, polysilicon bias
  - Metal overhang to mitigate E-field







INFN-FBK planar sensors in CMS

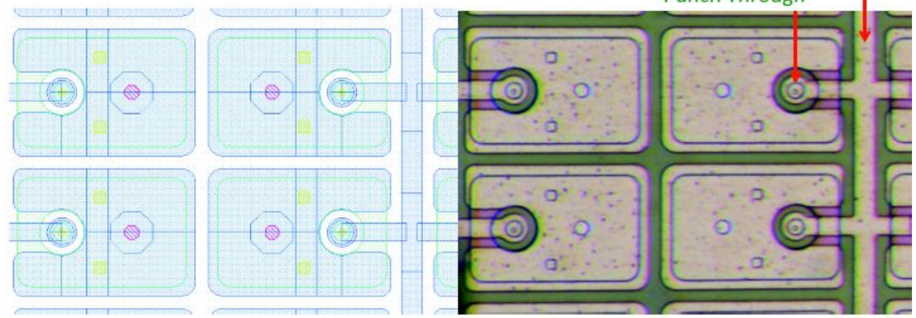
- N-in-p pixels on 6” production line, various sensor types
  - P-stop, p-spray
  - With/without punch-through bias structure
  - Evaluate: thinning, BCB, bump-bonding

Test of punch through bias structure

Picture and gds layout of a sensor identical to the proton irradiated one

Metal Bias Grid

Punch Through

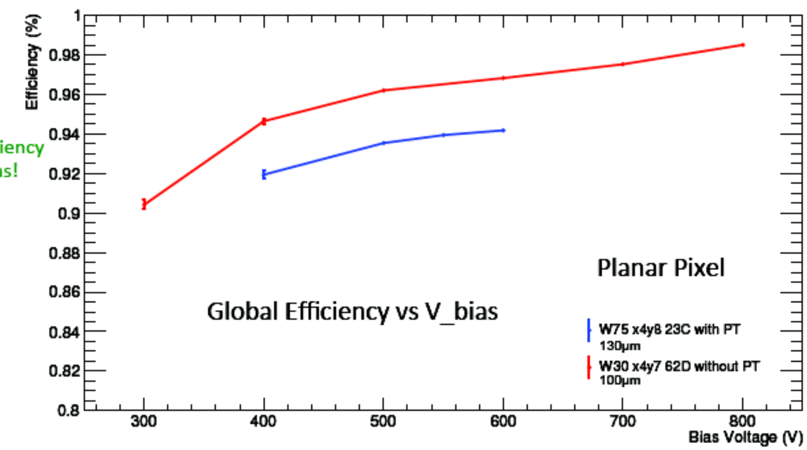


PT Design layout

PT Real life picture

Projected efficiency on transverse section

High hit efficiency at high V_bias!

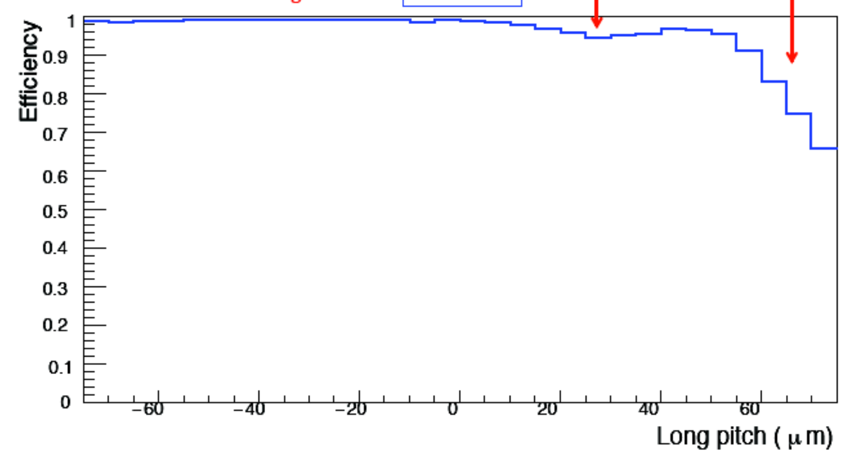


Efficiency is > 99% away from PT and metal grid

600 V bias

Punch Through

Metal Bias Grid



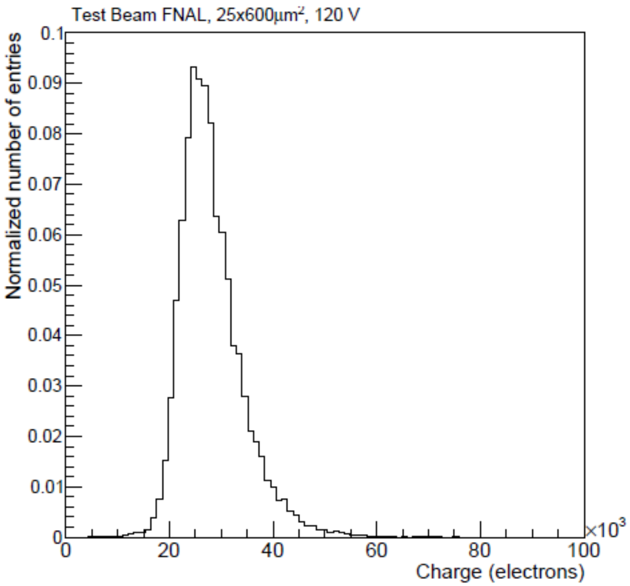
100 μm and 130 μm thickness, irradiated with protons to 3×10^{15} neq/cm²

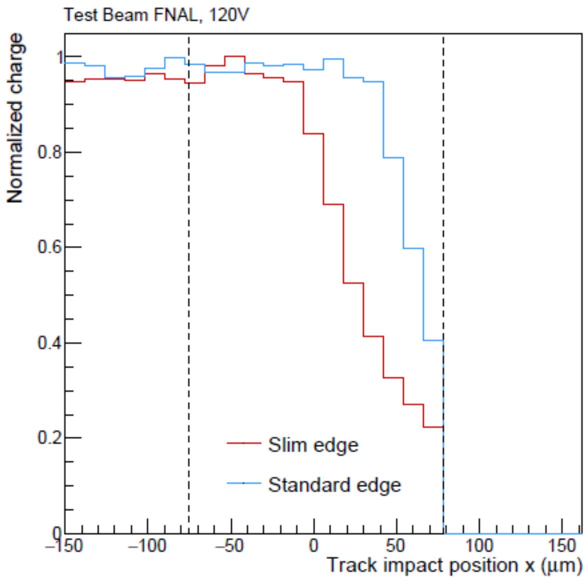
More tests ongoing

CMS Sintef planar sensor study

- n-in-n sensors at Sintef, 300 µm thickness
  - Testbeam measurements:
  - 25x600 µm² pixel size

– 100x150 µm² pixel size





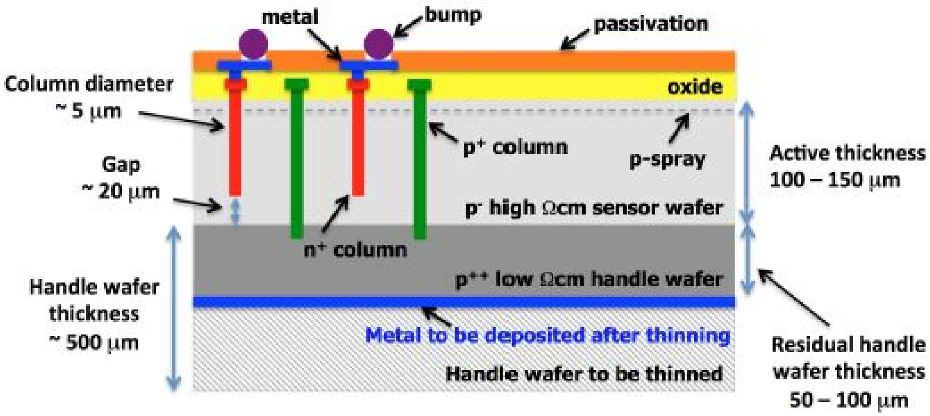
First thin small pixel test sensors work well
Next step: Demonstrate radiation hardness

(SINTEF (n^+-n))

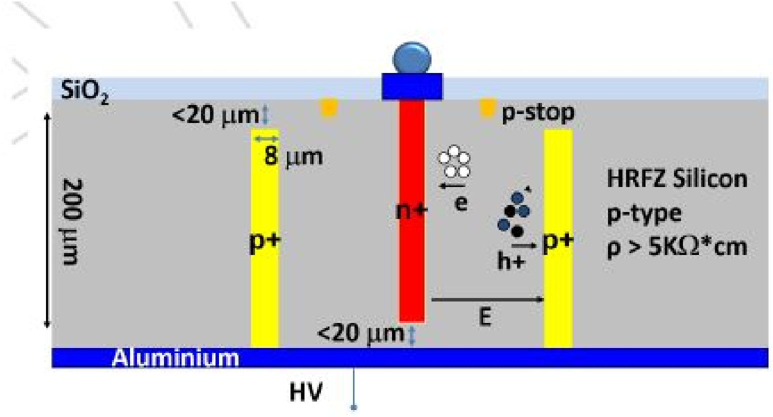
INFN/FBK

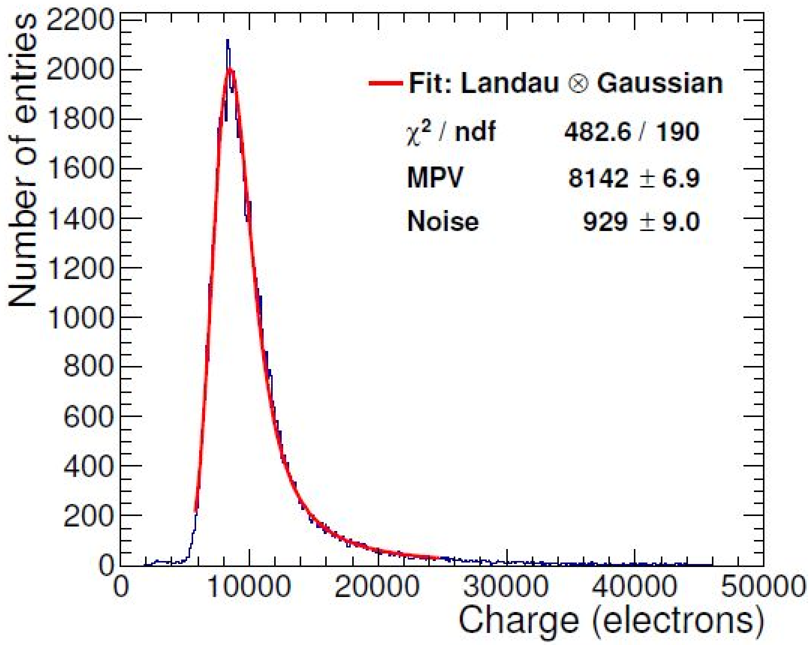
3D sensors in CMS

Single-sided process FBK



Double-sided process CNM





Testbeam results

FBK 3D sensor with 130 μm active thickness, 100x150 μm² pixel size

Bump-bonded to FE-i4 at Selex

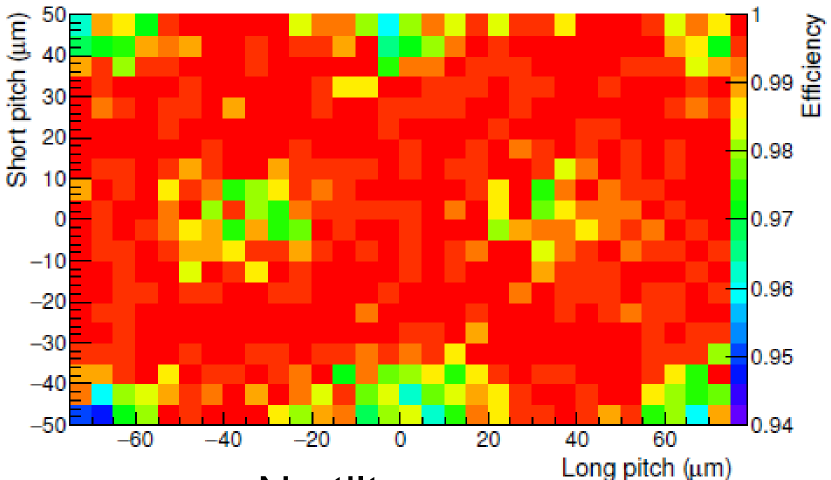
G. Steinbrück

3D sensors in CMS ctd'

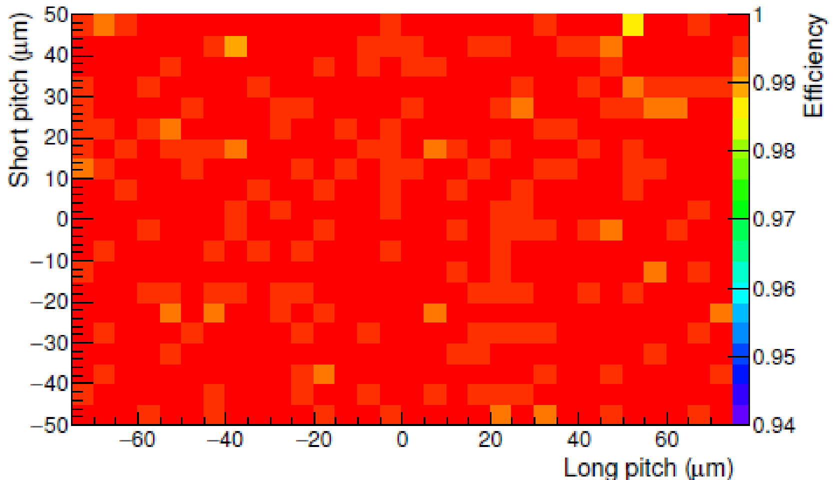
G. Steinbrück
A. Messineo

Testbeam results

FBK 3D sensor with 130 μm active thickness, 100x150 μm² pixel size



No tilt



Tilt 5°

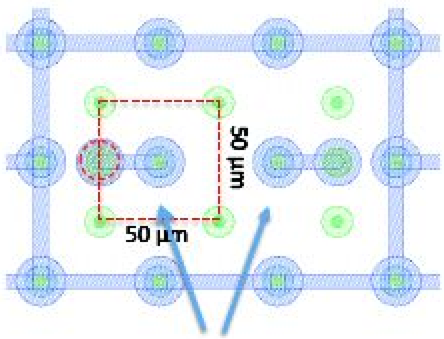
Angle (degrees)	*Efficiency 3E*	*Efficiency 2E*
0	**99.27%**	**99.45%**
5	**99.77%**	**99.85%**
10	**99.88%**	**99.87%**
max Δ Efficiency	**0.62%**	**0.43%**

- Efficiency improved for non orthogonal tracks

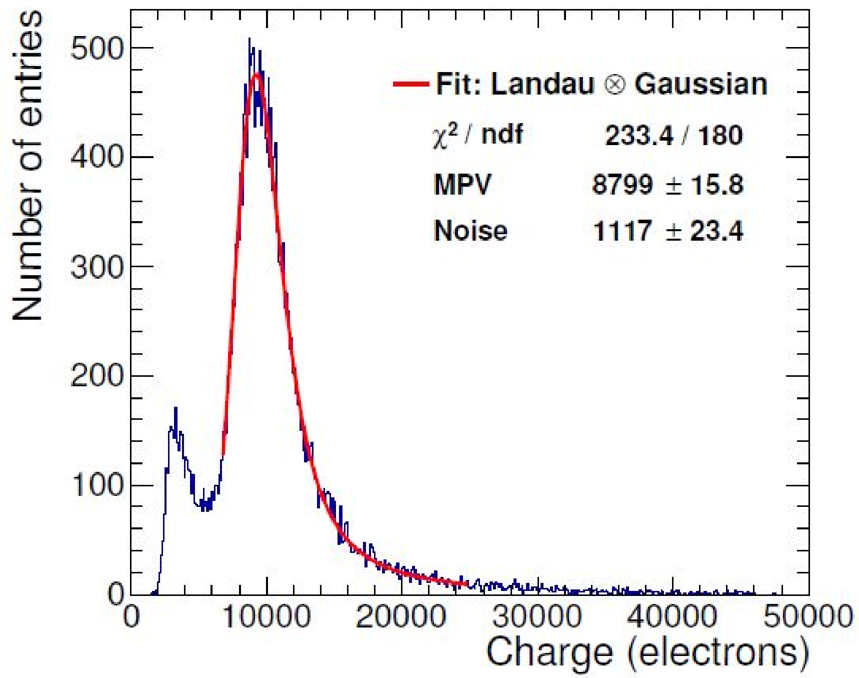
3D sensor at CMS with fine pitch 50x50 µm

G. Steinbrück

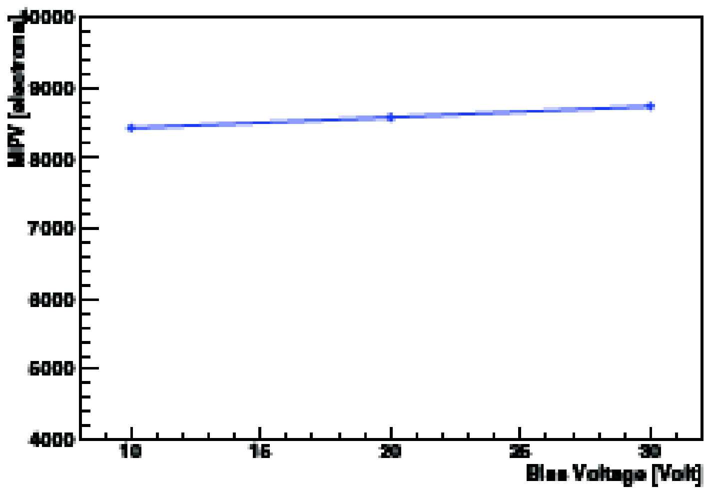
- 3D sensor with fine pitch 50x50 µm and 130 µm (HV=30 V)



Two adjacent double columns pixel readout
ROC (PSI46dig) fully connected
Sensitive area readout: 1/6



MPV vs Bias Voltage



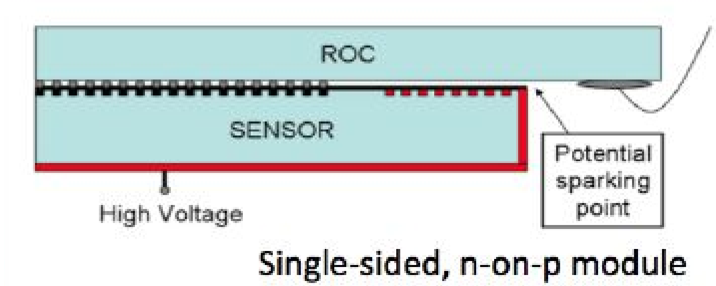
Successful production of 3D sensors. Next step: Demonstrate feasibility of small pixels.

INFN/FBK
CNM

Sensor – FE insulation

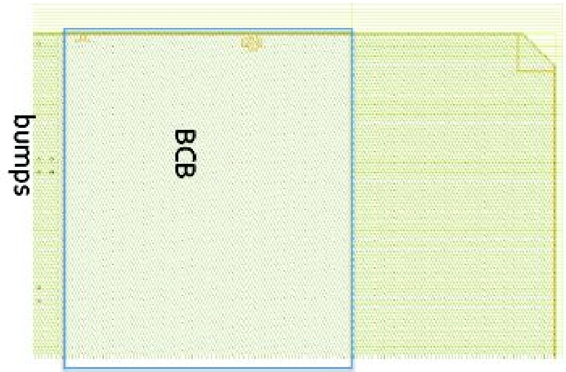
A. Macchiolo

- Insulation of sensor HV and FE ground
  - ATLAS study of BCB polymere isolation layer on FE and parylene coating of module

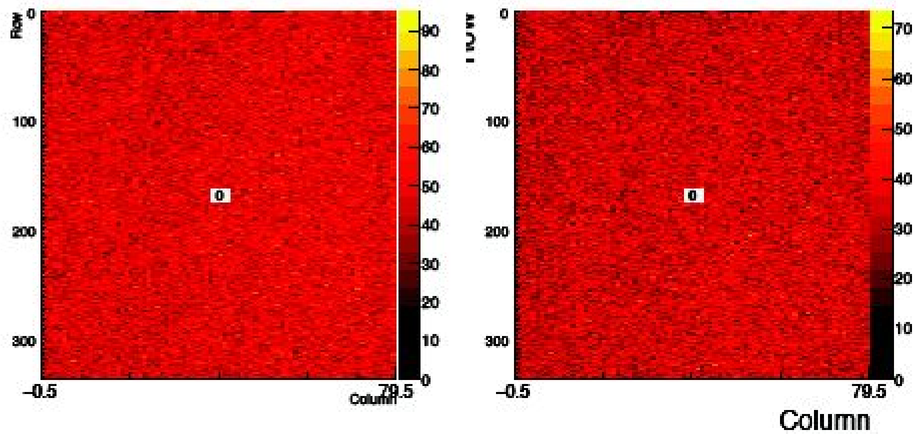


Sensor coated with BCB proven HV up to ~900 V

- For some sensor production technology (backside cavities, active edge sensors) the deposition of BCB isolation layer on the sensors is problematic or impossible → Have the BCB isolation deposited on the chip side



FE-I4 wafers with BCB processed at IZM (LPNHE and MPP project)



Occupancy of new modules during self-trigger source scan using a radioactive Cadmium source

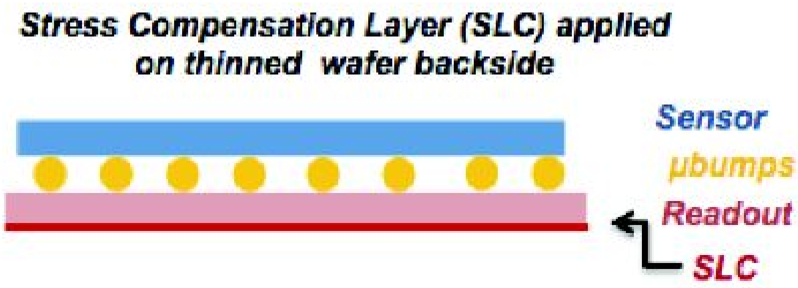
- HV capabilities to be proven after irradiation
- Cost-reduction due to larger size of chip wafers

Challenges of interconnection

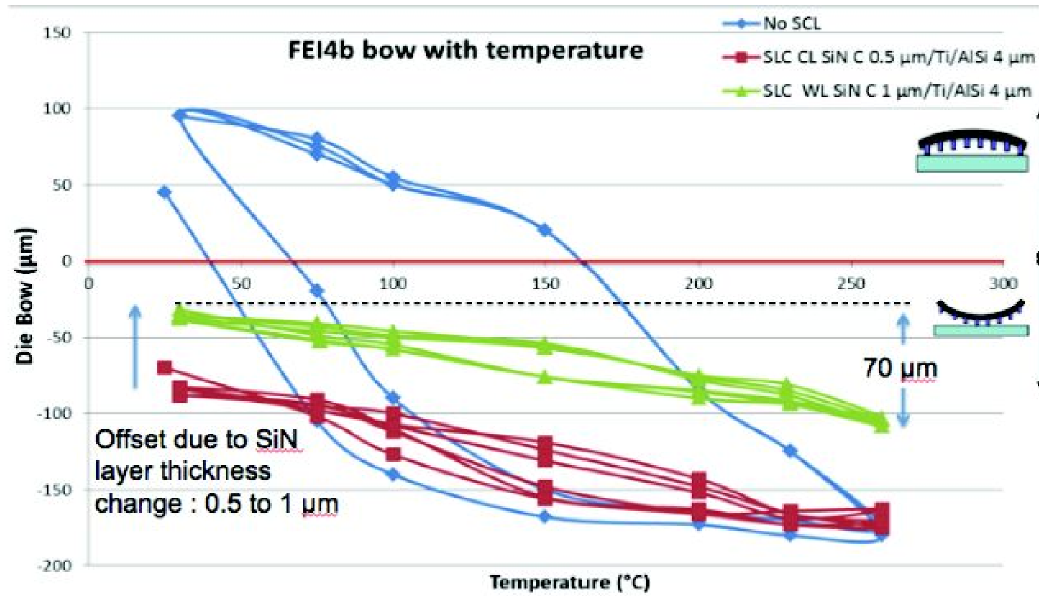
- Bump-bonding for connection between sensor and readout chip
  - Reduce cost and increase production speed despite fine pitch and thin silicon
  - Exploring solutions:
    - UBM at sensor foundry (CIS, HPK, MICRON, ADVACAM, …)
    - Chip to Wafer bonding requires TSVs
- Wire-bonds for connection of bare module chip and flex
  - Oscillations in magnetic field
  - Protection desired (potting): possible field for common R&D
  - Limit on active sensor area to have access to readout chip bond area, limit on envelops

Bump bonding

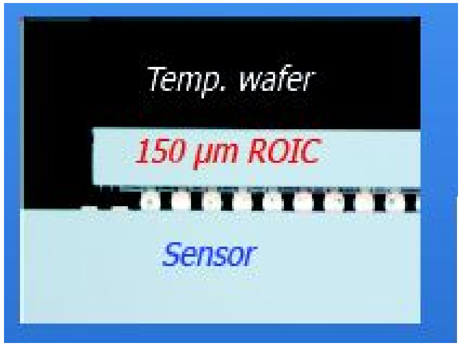
- 50 µm minimum pitch but high density on large chip surface (~ 4 cm²) and aim for large wafer sizes
- Thin sensors and chips to reduce material → stability, bow of wafers



Backside compensation layer to counteract bow from front side



- Temporary wafer for production steps, after flip-chipping laser debonding (300 µm glass)
- Comparison of various vendors in preparation in ATLAS



IZM

Summary

- Hybrid pixel working very well and advanced for Phase-II trackers in ATLAS and CMS
  - Sensor and FE bump-bonded
  - Signal processing in pixel cell
  - Radiation hard to > $1x10^{15}$ neq/cm^2
  - High rate capability and spatial resolution

BUT

  - Relatively large material budget
  - Complex and laborious module production
  - Costs

- Challenge: low cost for outer radii and radiation hardness, thermal runaway, material budget for inner radii
- R&D programs to develop thin, fine pitch sensors+FE and address pixel design issues

Thank you!

Thank you for material to Claudia Gemme, Anna Macchiolo, Alberto Messineo, Hideyuki Oide, Georg Steinbrück, Norbert Wermes

Sensors

Planar

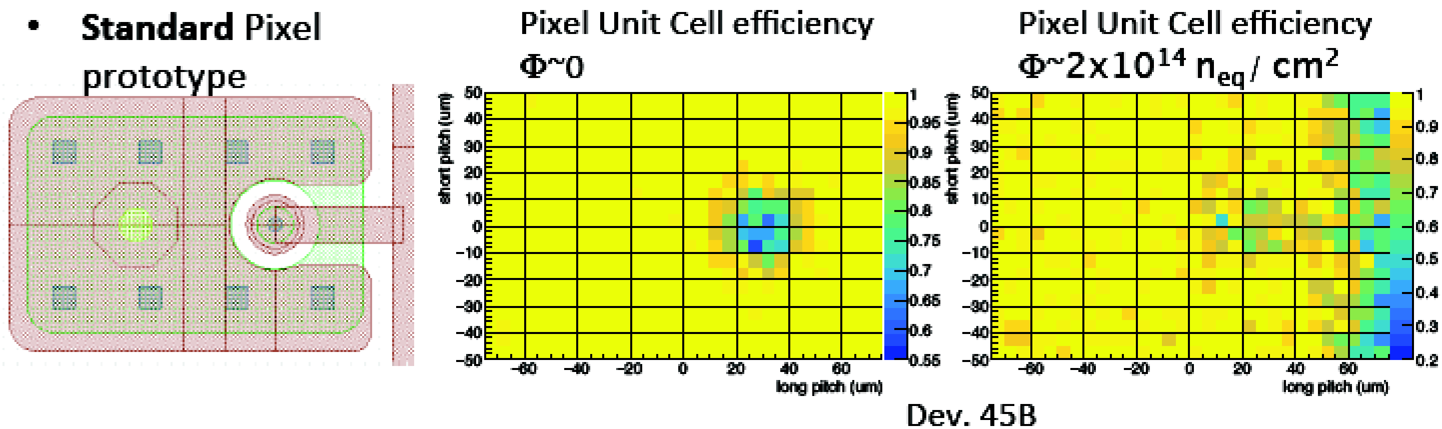
- low cost for outer radii and radiation hardness, thermal runaway, material budget for inner radii
- Baseline n-in-p sensors
- 50x50 μm² pixel test structures demonstrated
- Interconnection technologies investigated for thin planar pixel sensors of thickness 50-200 μm
- Good hit efficiencies up to the physical perimeter of the devices obtained with (100-150) μm thin active edge sensors
- Different vendors investigated: CiS, Advacam, MPG-HLL, FBK, HPK, ….

3D

- Design of small cells and thinner substrate
- Production rate and yield
  - Columns of 5-8 um diameter alternately n- and p-type doped
  - Single sided process, thin 50-200 μm thick thanks to support wafers
  - Slim edges of 15-150 μm, even active edges sensitive up to the physical edge
  - Steady progress on 50 x 50 μm² & 25 x 100 μm² pixel design
- Sintef, FBK and CNM making devices: moving at RD53A-prototypes

Effect from bias pads

- Tracks detection efficiency is affected by the pixel bias structure (CMS)



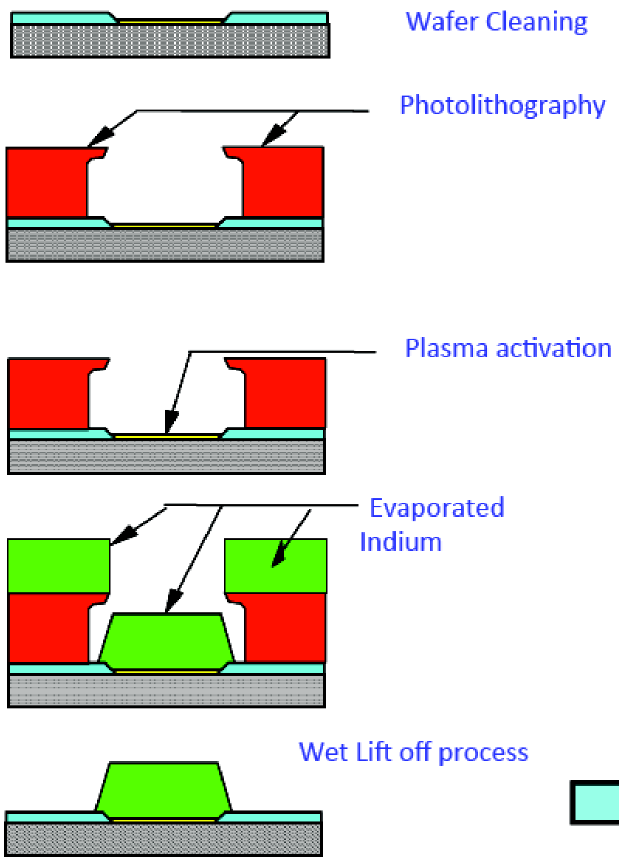
Geometry of the bias structure or moderated p-spray mitigate the inefficiency before irradiation, observed however after irradiation

→ Simulation study to optimize geometry/process of bias structure, critical for small pitch pixels

SPARE

Challenges of interconnection

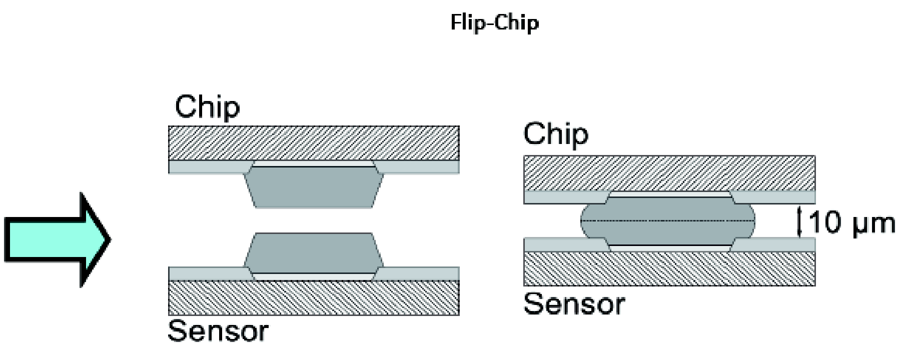
- Indium bumping process



universitätbonn

Process parameters:

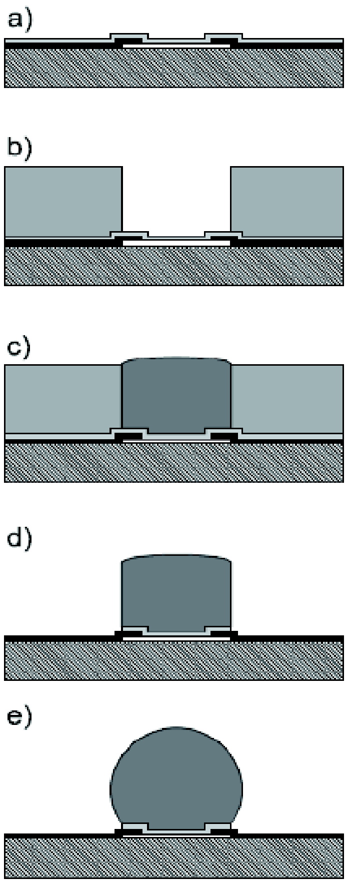
- Resist Thickness: 15 μm
- Pre-bake: 30min @ 80 °C
- Deposition rate: 0.5 μm/min
- Dep. Pressure: 9 x 10^{-7} Torr
- Temp. during Dep. < 50 °C



Challenges of interconnection

- Solder bumping & flip chip process

universitätbonn



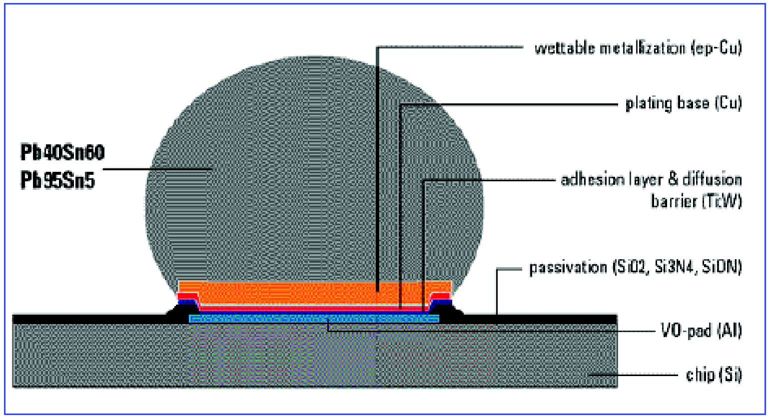
a) Sputter etching and sputtering of the plating base / UBM

b) Spin coating and printing of Photoresist

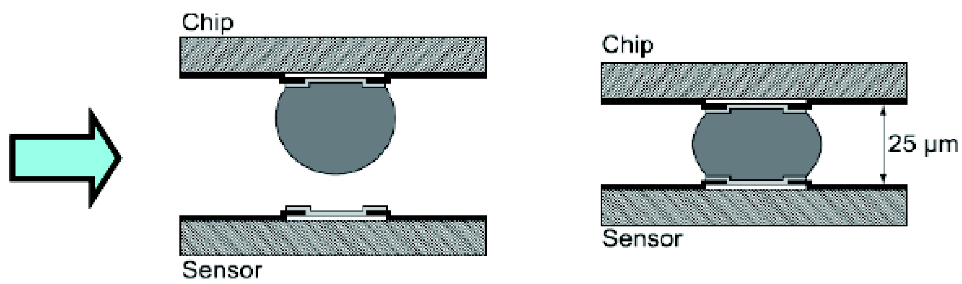
c) Electroplating of Cu and PbSn

d) Resist stripping and wet etching of the plating base

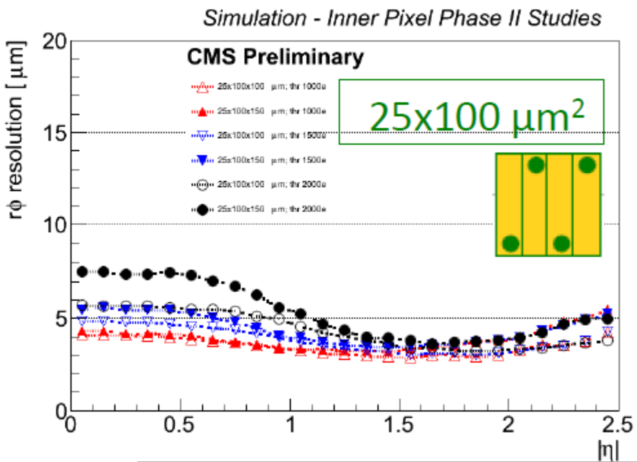
e) Reflow

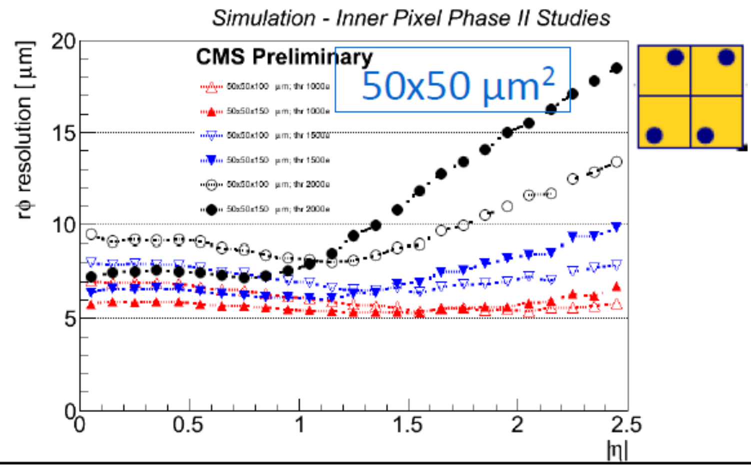


Flip-Chip

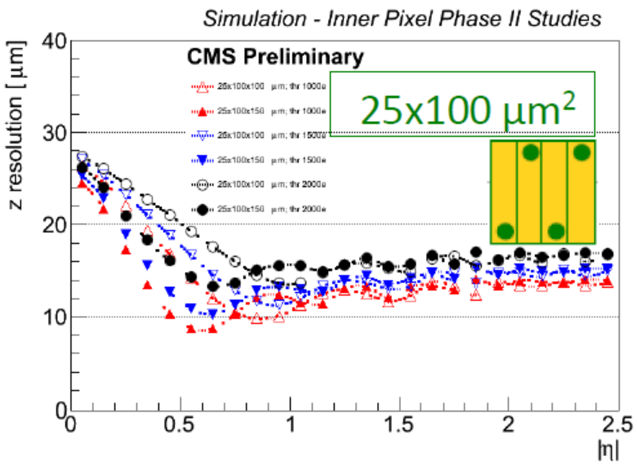


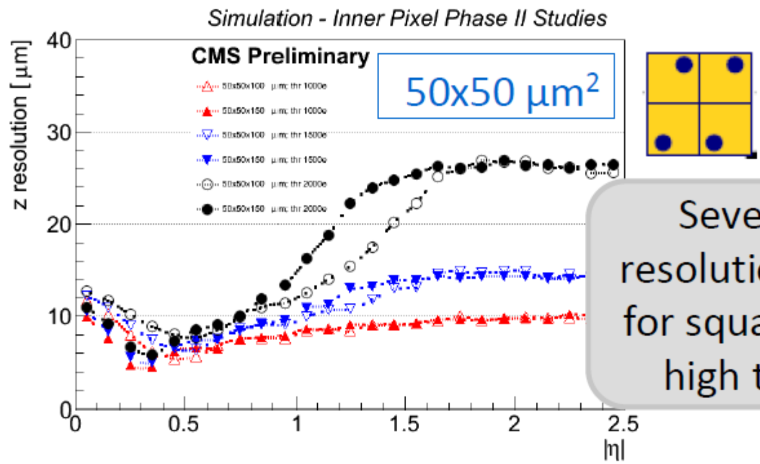
Study of pitch in CMS





thickness open=100 μm/full=150 μm threshold 1000e/1500e/2000e

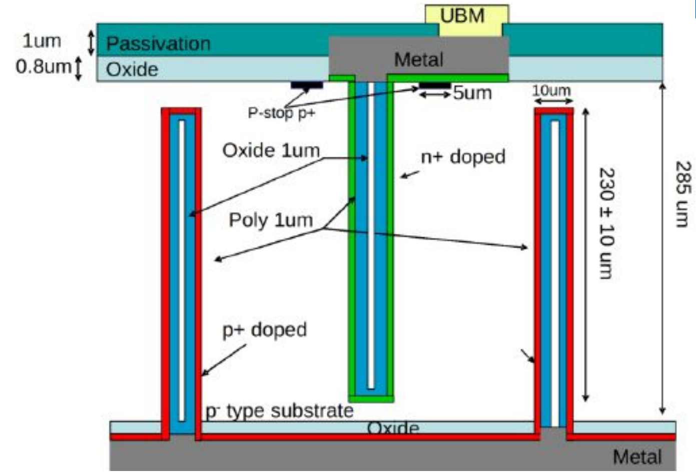


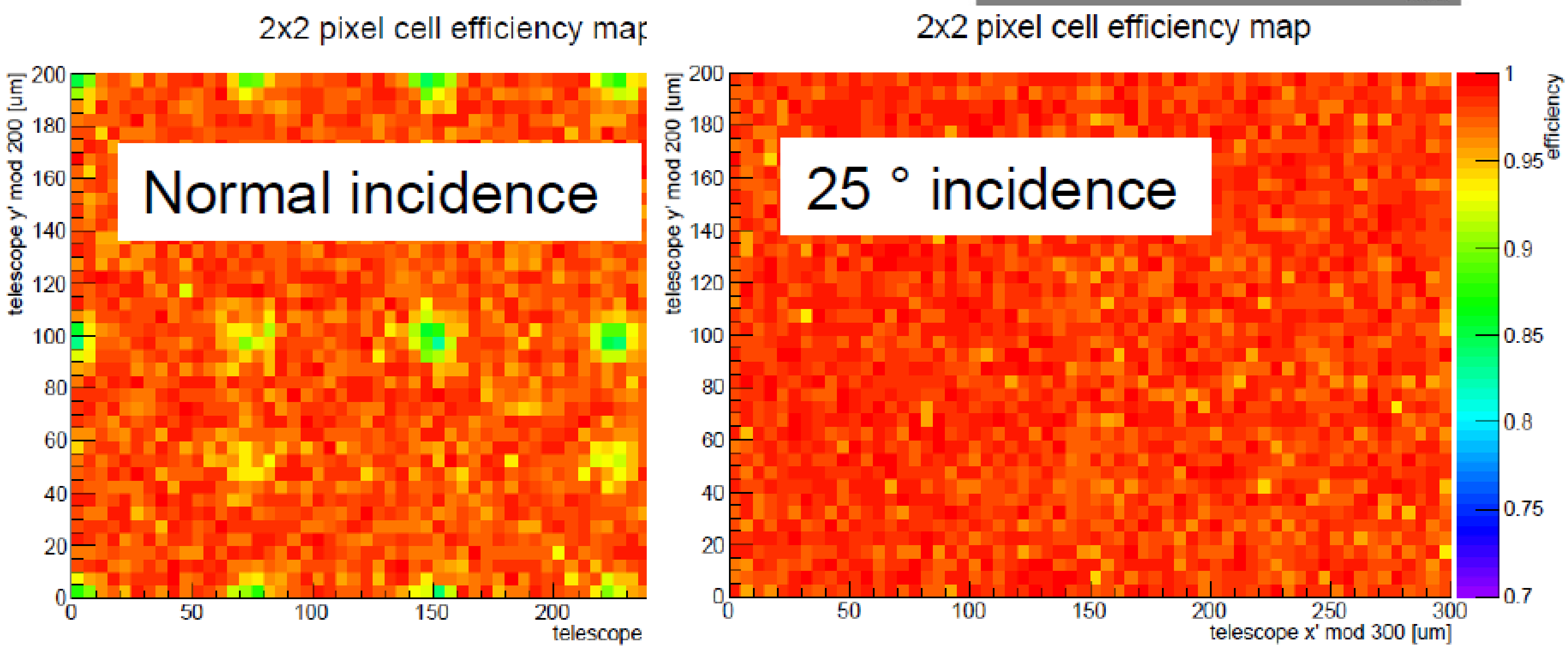


Severe loss of resolution at large η for square pixels for high thresholds

3D sensors from CNM in CMS

- 3D pixel sensors fabricated by CNM, Spain
- IBL run, read out with CMS PSI46dig ROC
- 100x150 μm²
- Double sided 3D process yields good sensors with "standard" pixel size



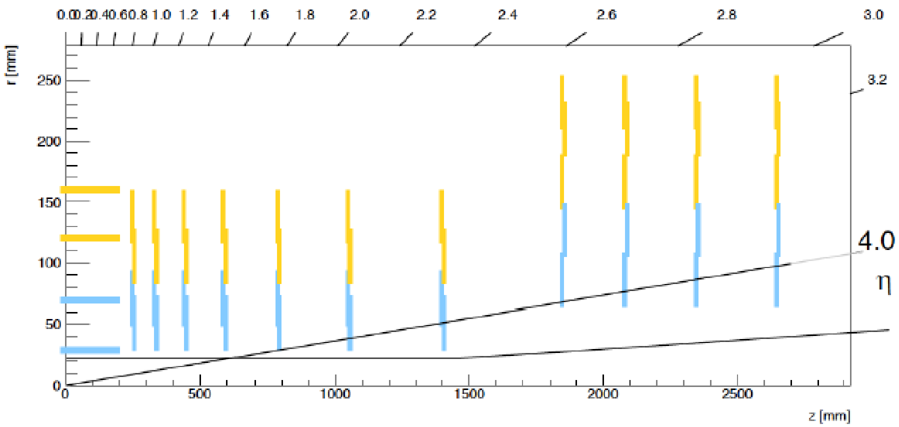


CMS Pixel detector for HL-LHC

G. Steinbrück, VERTEX 2016

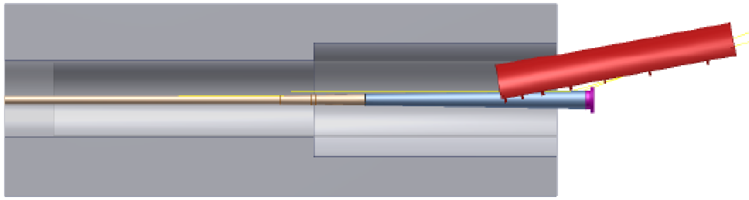
Coverage of geometrical acceptance:

- Barrel:
  - 4 layers à la phase I: $r_1 = 2.9$ cm, $r_4 = 16.0$ cm but shorter: $z_{max} = \pm 20$ cm instead of ±27 cm
- Forward:
  - coverage at large |η| obtained by increasing the number of discs (11+11) $z_1 = \pm 25$ cm $z_{11} = \pm 265$ cm



Total: ~4.5 m² of Si

- Simple mechanics:
  - no turbines/blades in the FPIX discs
- Step in the pixel envelope
  - r=20 cm → r =30 cm at z=160 cm
  - to allow the installation of the central section with beam pipe in place



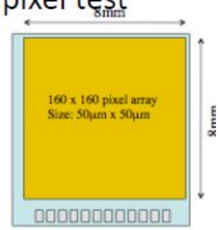
CMS options for readout chips

G. Steinbrück, VERTEX 2016

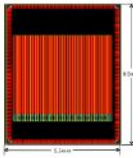
- PSI46dig and PROC600
  - **IBM 250 nm, 100 x 150 μm^2**, 80 x 52 pixels, rad hard > 5 MGy (PROC600)

PSI46dig only chip available as of today, but not as rad. hard

- ROC4Sens (PSI)
  - **IBM 250 nm, 50 x 50 μm^2** , 155 x 160 pixels, no charge threshold, rad hard > 5 MGy, operated with CMS pixel test board, **staggered BB pattern**, opening 15 µm
  - available since summer 2016 (on PROC600 wafer)



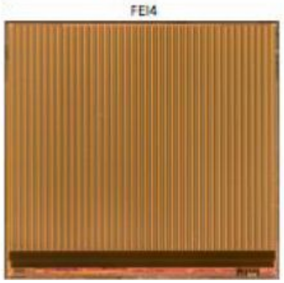
- FCP130 (FNAL)
  - **GF 130nm, 30 x 100 µm2** , 160 x 48 pixels, threshold: ~1000 e- , rad hard few MGy, DAQ under development
  - availability foreseen early 2017



- RD53A:
  - **65nm, 50 x 50 µm2** , 400 x 192 pixels, min. threshold: 600 e- , rad hard up to 10 MGy **non-staggered BB pattern**
  - availability 2017

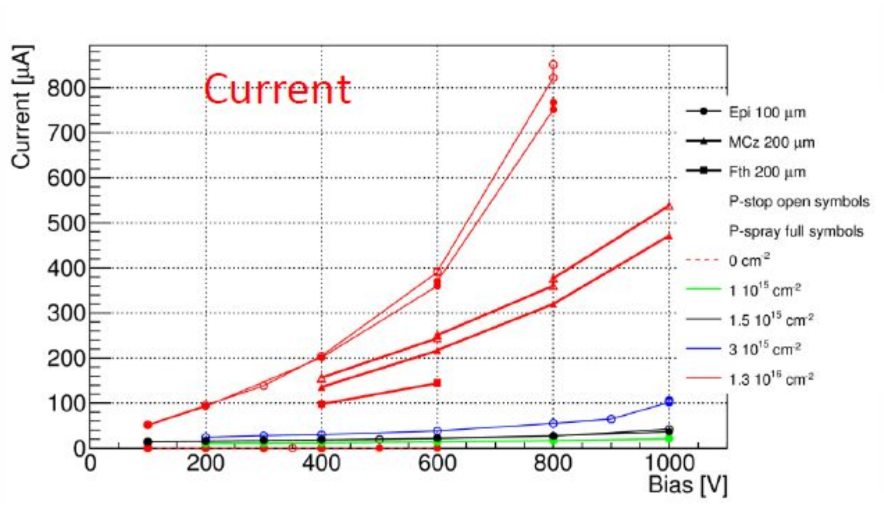
For ROC developments, see also talks on "*RD53 status and plans*" by L. Gaioni and "*Radiation Tolerance of 65nm CMOS*" by M. Menouni (Thu)

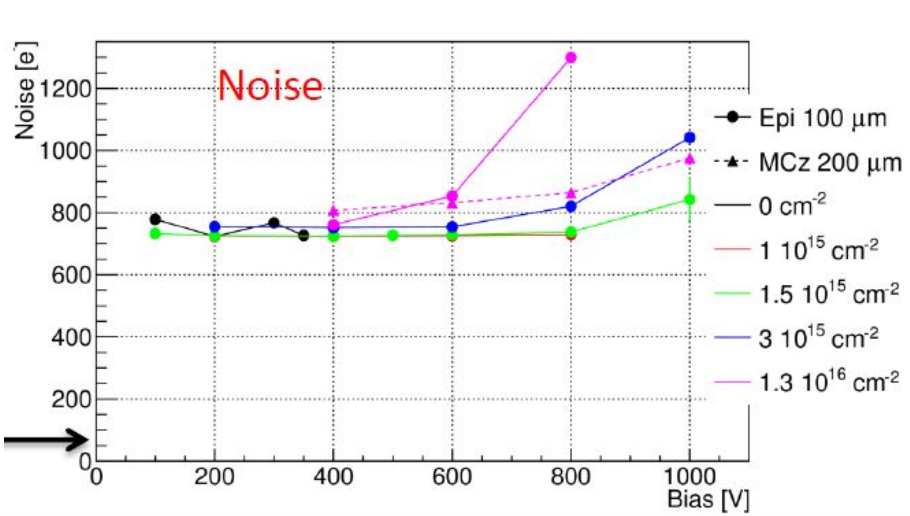
- FEI4 (ATLAS) (used for serial powering studies)
  - **GF 130 nm, 50 x 250 μm^2**, 336 x 80 pixels, threshold < 2000 e$^-$, rad hard > 5 MGy

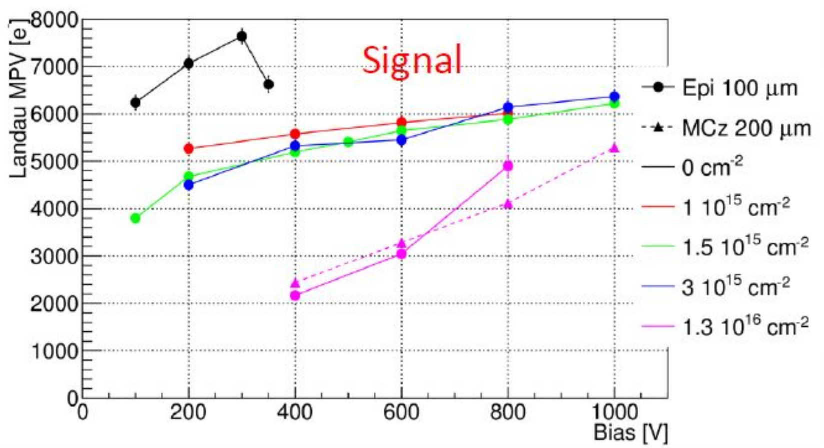


CMS planar sensor study

G. Steinbrück, VERTEX 2016







N-in-p strip sensor study, 200 μm thickness

After high fluence and at high bias voltages sign of charge multiplication and increase in noise and leakage current

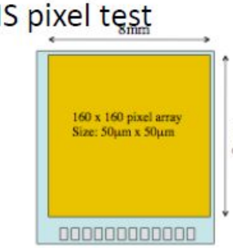
CMS options for readout chips

G. Steinbrück, VERTEX 2016

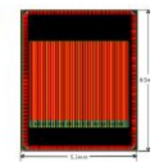
- PSI46dig and PROC600
  - **IBM 250 nm, 100 x 150 µm²**, 80 x 52 pixels, rad hard > 5 MGy (PROC600)

PSI46dig only chip available as of today, but not as rad. hard

- ROC4Sens (PSI)
  - **IBM 250 nm, 50 x 50 µm²** , 155 x 160 pixels, no charge threshold, rad hard > 5 MGy, operated with CMS pixel test board, **staggered BB pattern**, opening 15 µm
  - available since summer 2016 (on PROC600 wafer)

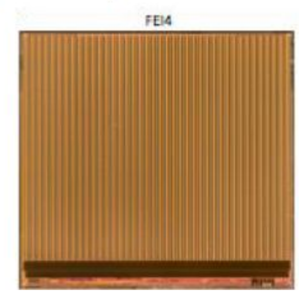


- FCP130 (FNAL)
  - **GF 130nm, 30 x 100 µm2** , 160 x 48 pixels, threshold: ~1000 e- , rad hard few MGy, DAQ under development
  - availability foreseen early 2017



- RD53A:
  - **65nm, 50 x 50 µm2** , 400 x 192 pixels, min. threshold: 600 e- , rad hard up to 10 MGy **non-staggered BB pattern**
  - availability 2017

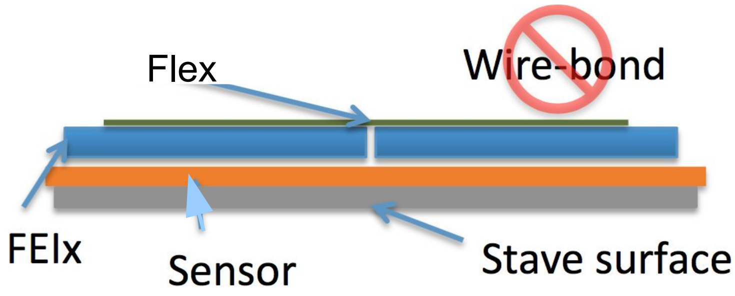
For ROC developments, see also talks on "*RD53 status and plans*" by L. Gaioni and "*Radiation Tolerance of 65nm CMOS*" by M. Menouni (Thu)



- FEI4 (ATLAS) (used for serial powering studies)
  - **GF 130 nm, 50 x 250 µm²**, 336 x 80 pixels, threshold < 2000 e^- , rad hard > 5 MGy

R&D beyond HL-LHC on compact modules

- Modules with through-silicon-vias: wire-bond less pixel module
  - Deploying TSV processes
  - Instead of wire-bonds connect flex via solder balls on back of chip
    - Less fragile module
    - Reduced interconnect inductance
  - Wire-bond pads can be removed: reduced chip edge
  - Wafer-to-wafer bonding possible: no need for flip-chipping

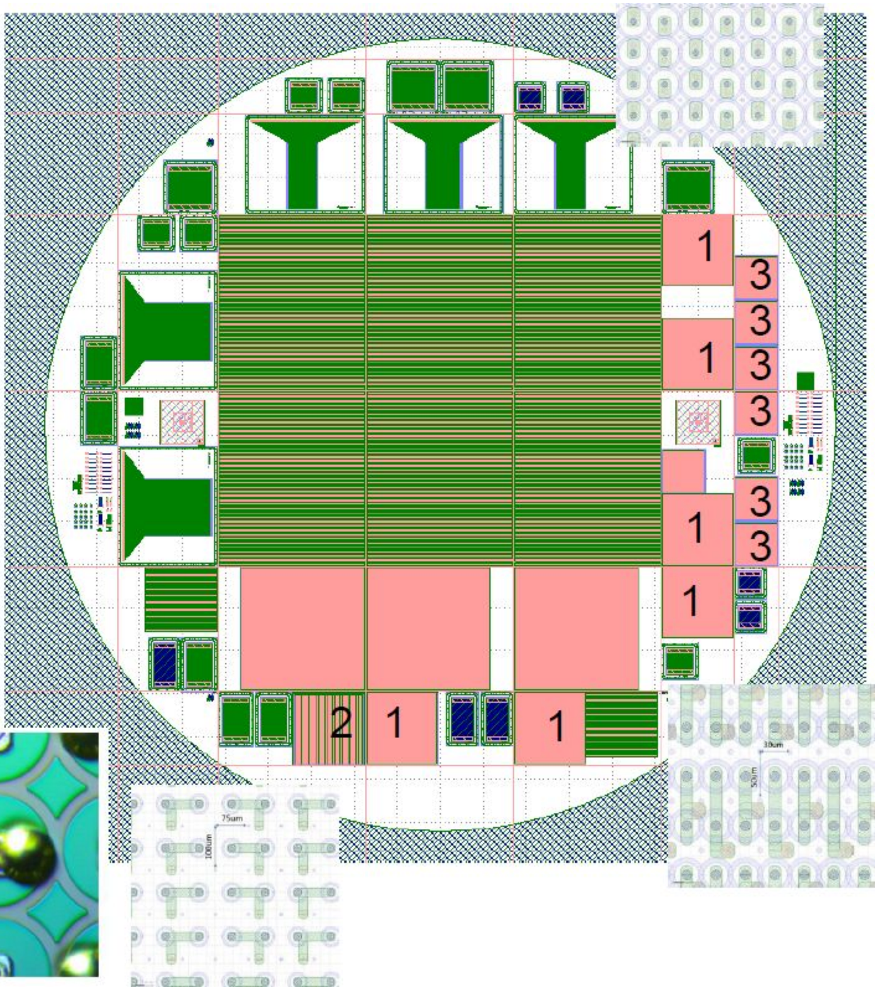


3D sensor study with small pitch with CNM

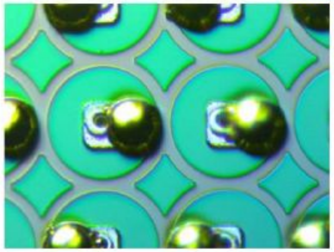
- Joint RD50 project: ATLAS, CMS, LHCb
- 230 μm wafer, n-in-p, double sided
- CMS: Sensor designs for 3 chips

1)	ROC4sens	50x50 μm^2
2)	PSI46dig	100x150 μm^2
3)	Fermilab FCP130	30x100 μm^2

- **Aims:**
  - Test small pitches (25x100 and 50x50)
  - **Aspect ratio: 8 μm holes in 230 μm (1:25)**
  - 100 μm and 200 μm slim edges
  - Radiation hardness of different layouts



5 wafers completed December 2015
All diced
Investigating Ni/Au UBM
(electroless and electroplating)
Flip-chip to FE-I4 validation in progress



CERN