# Monolithic CMOS Pixel Developments

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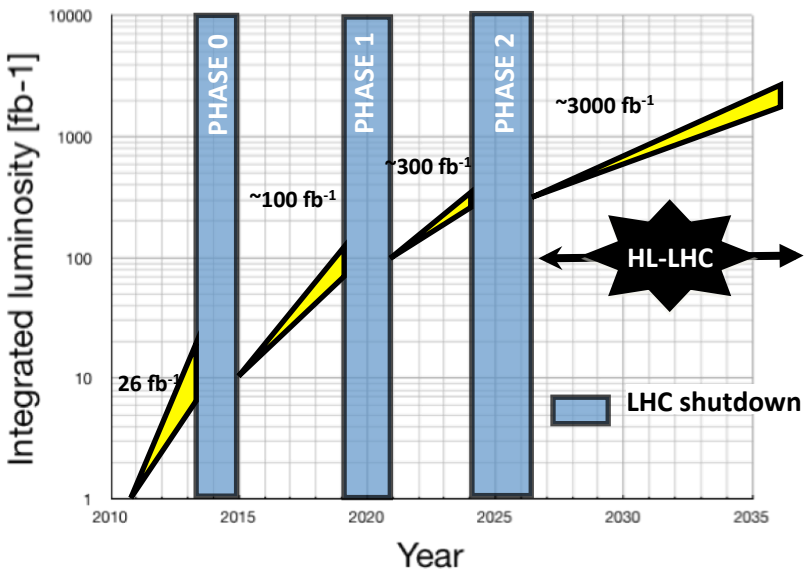
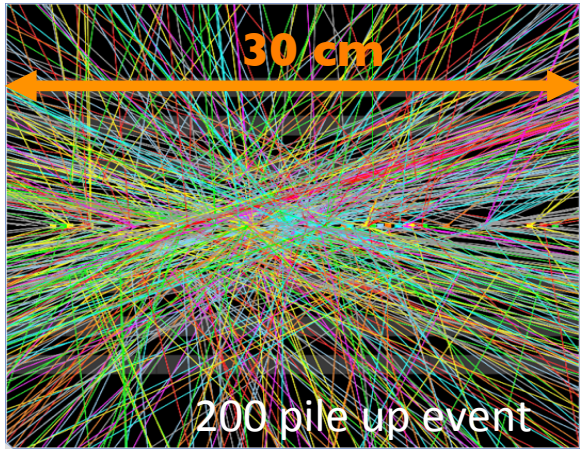
# High Luminosity - LHC



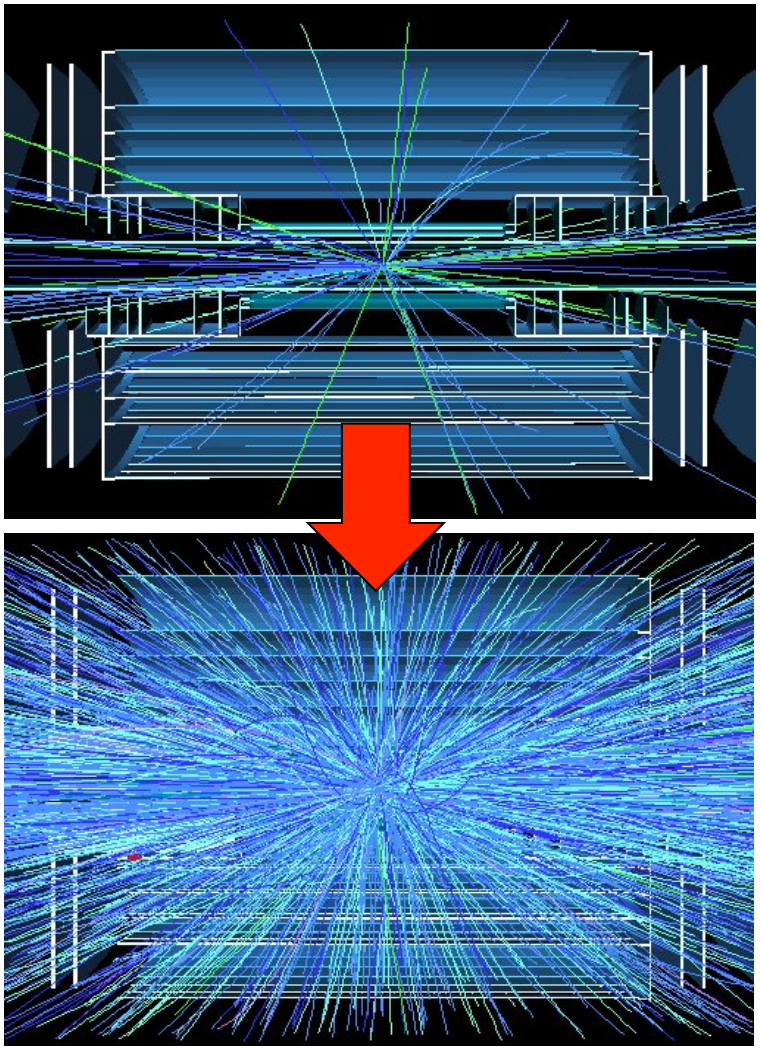




## HL-LHC (High Luminosity LHC)

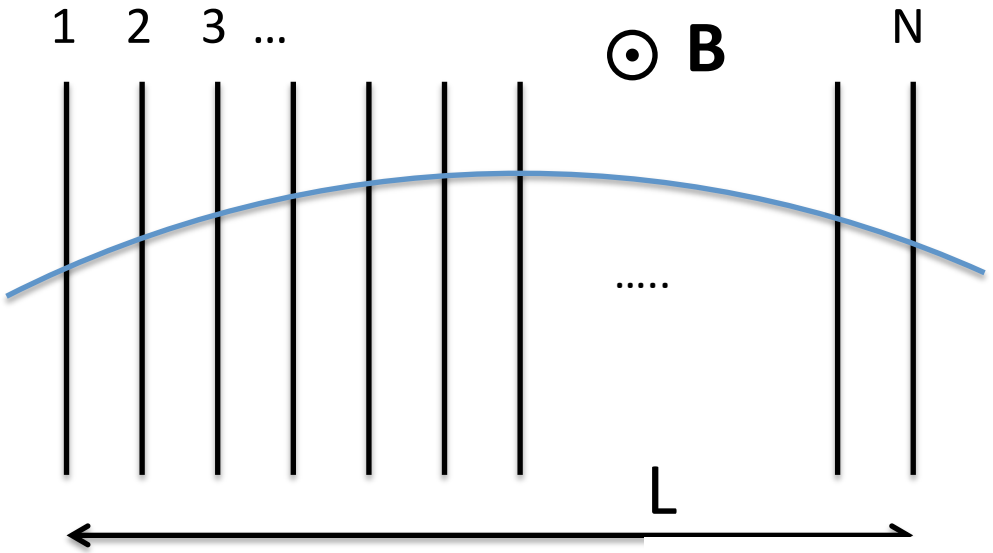
- Collisions to start mid-2026
- Maximum leveled instantaneous luminosity of 7.5 x $10^{34}$ $cm^{-2}$ $s^{-1}$
  - Currently 1 x $10^{34}$ $cm^{-2}$ $s^{-1}$
- 3000 $fb^{-1}$ Integrated luminosity to ATLAS over ten years
- 200 (mean number of) interactions per bunch crossing.
  - Original design for 25 interactions per bunch crossing

# Challenges for the future

- Increased luminosity requires
  - Higher hit-rate capability
  - Higher segmentation
  - Higher radiation hardness
  - Lighter detectors
- Radiation hardness improvement compared to now
  - IBL approx. factor 5
  - Phase-2 approx. factor 10-30



# Tracking - momentum resolution




σ … point resolution/plane

$X_{tot}/X_0$ … total material budget

## Position Resolution

**Pixel = high spatial resolution**
O(10μm) on hybrid and down to O(1-3μm) on MAPS

$$\frac{\Delta p_t}{p_t} = \frac{\sigma[m]\, p[\mathrm{GeV/c}]}{0.3\, B[T]\, L^2[m^2]} \sqrt{\frac{720\,(N-1)^3}{(N-2)\,N\,(N+1)\,(N+2)}}$$

$$\approx \frac{\sigma[m]\, p[\mathrm{GeV/c}]}{0.3\, B[T]\, L^2[m^2]} \sqrt{\frac{720}{N+4}}$$

## Multiple Scattering

**Pixel = light detectors**
Thin detectors on light carbon fibre supports O(1-2%/0.2% X/X0 per layer)

$$\frac{\Delta p_t}{p_t} = \frac{0.0136}{0.3\beta\, B[T]\, L[m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7}\frac{12+(N-1)N^2(N+1)}{(N-2)N(N+1)(N+2)}}$$

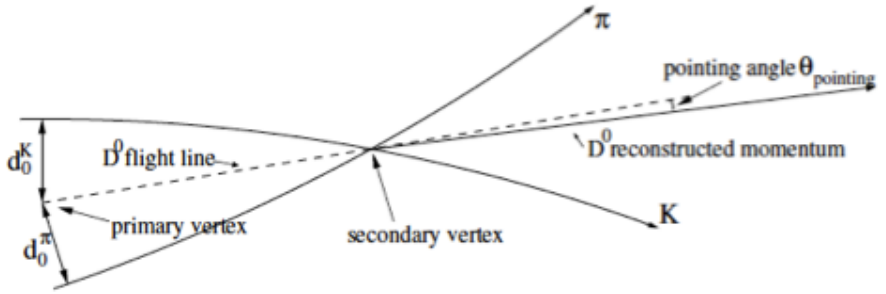
$$\approx \frac{0.0136}{0.3\beta\, B[T]\, L[m]} \sqrt{\frac{X_{tot}}{X_0}} \sqrt{\frac{10}{7}}$$

$$\approx \frac{0.0542}{\beta\, B[T]\, L[m]} \sqrt{\frac{X_{tot}}{X_0}}$$

W. Riegler FCC 2015

# Impact parameter

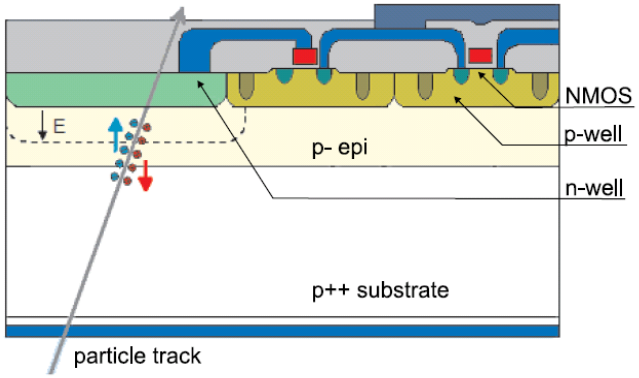
- Secondary vertices reconstruction strongly depends on impact parameter resolution
  - d0 in r/phi (bending plane)
  - Z0 alone beam direction

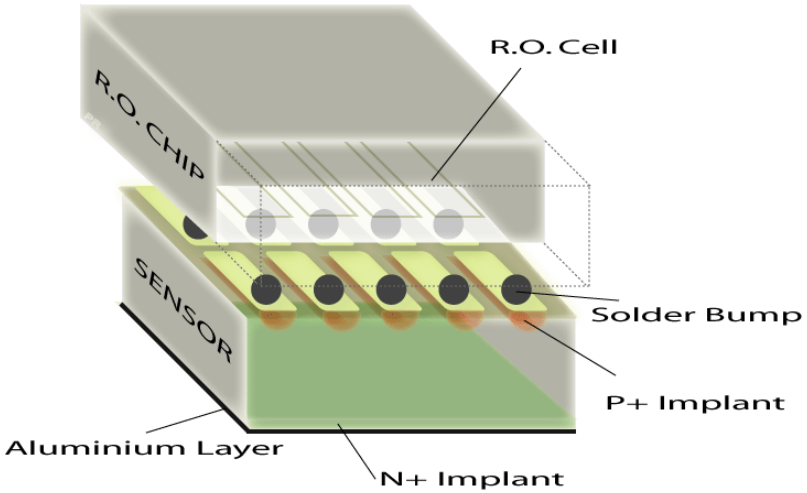



- Impact parameter resolution is strongly effected by
  - **Intrinsic point resolution** and alignment at higher momentum
  - **Multiple scattering in detector material** (in particular for low pt tracks)

- Look for tracking solutions which combine **small pixels** with **thin detectors**
- They need to be **radiation hard** and include complex readout architectures to cope with **high hit rates**

# The "World of Pixels" …




## Monolithic Pixels

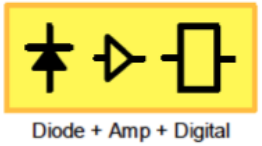
- Charge generation volume integrated into the ASIC
- **Used in ALICE ITS upgrade**

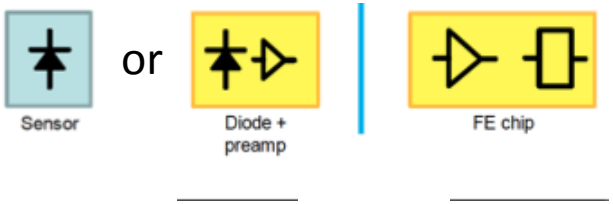
## Hybrid Pixels

- Sensor and ASIC are independent units
- **Used in ATLAS and CMS pixel detectors**

# Pixel Detector

- Monolithic CMOS sensors sofar usually target “low-radiation environments”
- Hybrid Pixel detectors at pp colliders due to high radiation/hit rate



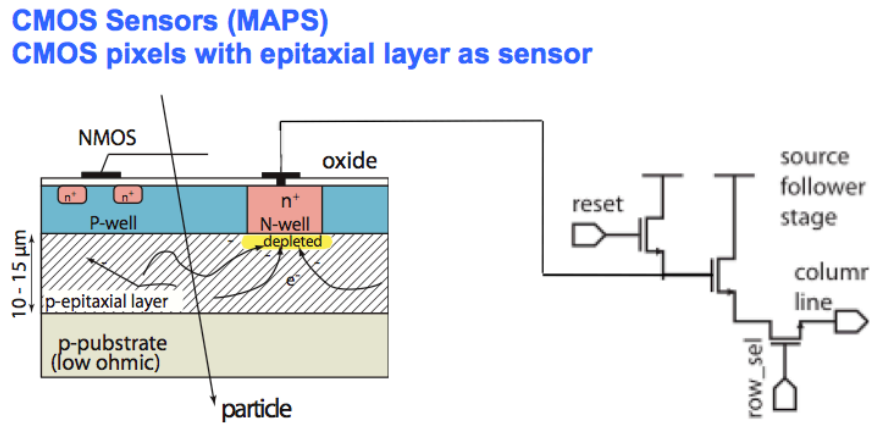

## Monolithic

- Thin monolithic CMOS sensor (DMAPS) On-chip digital readout architecture
- Advantages for larger surfaces due to assembly simplification and costs
- Small pixel and thin detectors
  - e.g. 28x28 um & 0.3%/layer in Alice ITS
- Design limits for highest hit rates
- Radiation hardness limits

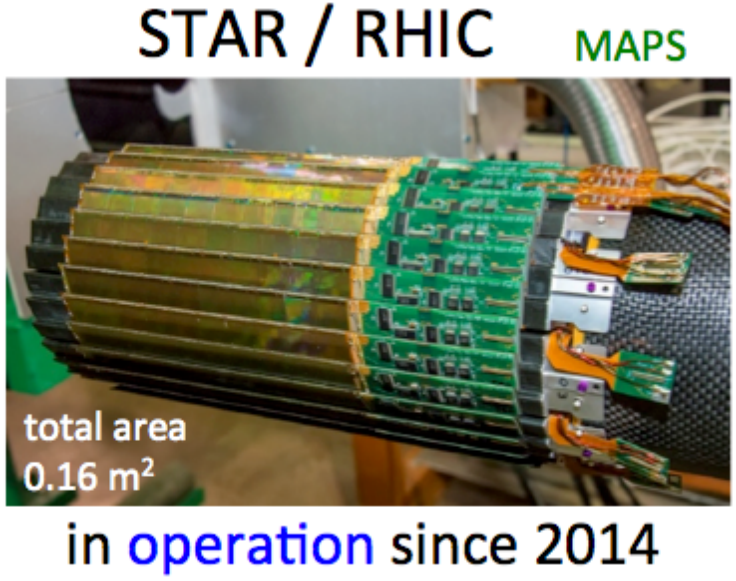
## Hybrid

- Complex readout with zero-supression on in-pixel hit buffering
- Separately optimize sensor and FE-chip for very high radiation environment
- Copes with high hit-rates
- Thick detector modules (X0 1.7-2.7%)
- Expensive through fine-pitch bump-bonding

# Monolithic Active Pixel Sensors




B. Dierickx, D. Meynants, G. Scheffer, SPIE 3410:68-76 (1998)
R. Turchetta, …, M. Winter et al, NIM A458 (2001) 677-689

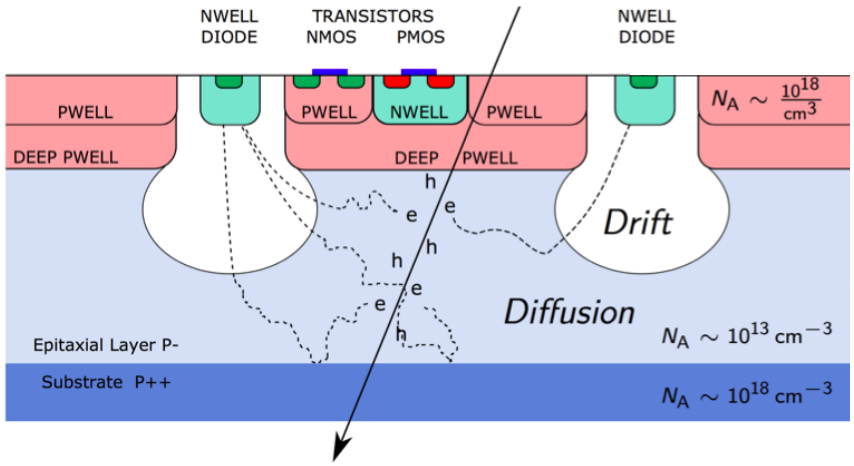



- CMOS process: use epitaxial layers as detection volume
- Limited to NMOS transistors
  - PMOS would result in competing n-well with charge collection electrode
- Sensors are fairly low power and allow e.g. air-cooling to minimize material
- Matrix typically read out with 3-transistor rolling shutter architecture

- This makes them very attractive for applications of high spatial resolution requirements but lower radiation/hit rates, e.g. experiments at heavy ion – colliders like **STAR HFT at RHIC**

# Monolithic Active Pixel Sensors

- Present state-of-art based on quadruple well allows full CMOS
- high resistivity (> 1kΩ cm) epi-layer (p-type, 20-40 µm thick) on p-substrate
- very small n-well diodes => small $C_{in}$
- moderate reverse bias => increase depletion region around Nwell collection diode



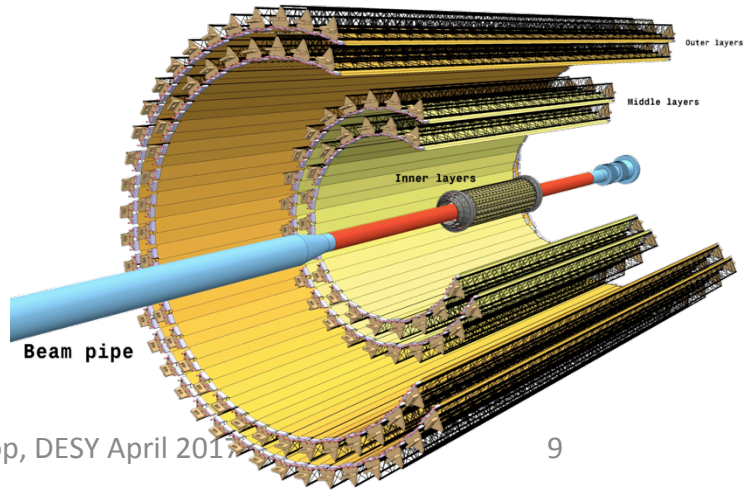

TowerJazz 0.18um full CMOS process
6 metal layers

ALICE Inner Tracker System (ITS) Upgrade

**3** Inner Barrel layers (IB)
**4** Outer Barrel layers (OB)
Radial coverage: 21-400 mm **~ 10 m²**

**0.3% $X_0$**/layer (IB)
0.8 % $X_0$/layer (OB)

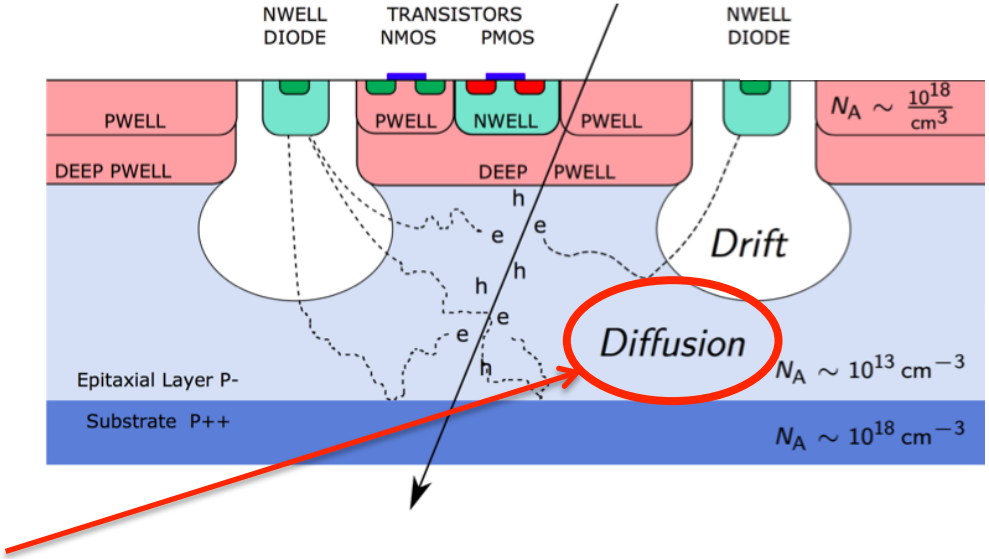
**Radiation level (L0): 700 krad/$10^{13}$ $n_{eq}$ $cm^{-2}$**




See next presentation by W. Snoeys

# Limitations

- For tracking MAPS appear to be the ideal detector
- BUT…
- **Diffusion is the limiting factor:**
- At high radiation (>$10^{16}$ neq/$cm^2$) ionization charge is trapped in non-depleted part – No more signal
- Diffusion make signal collection slower than typical requirements for pp-colliders




- Readout architectures are low power but not designed for high hit-rates like pp at LHC

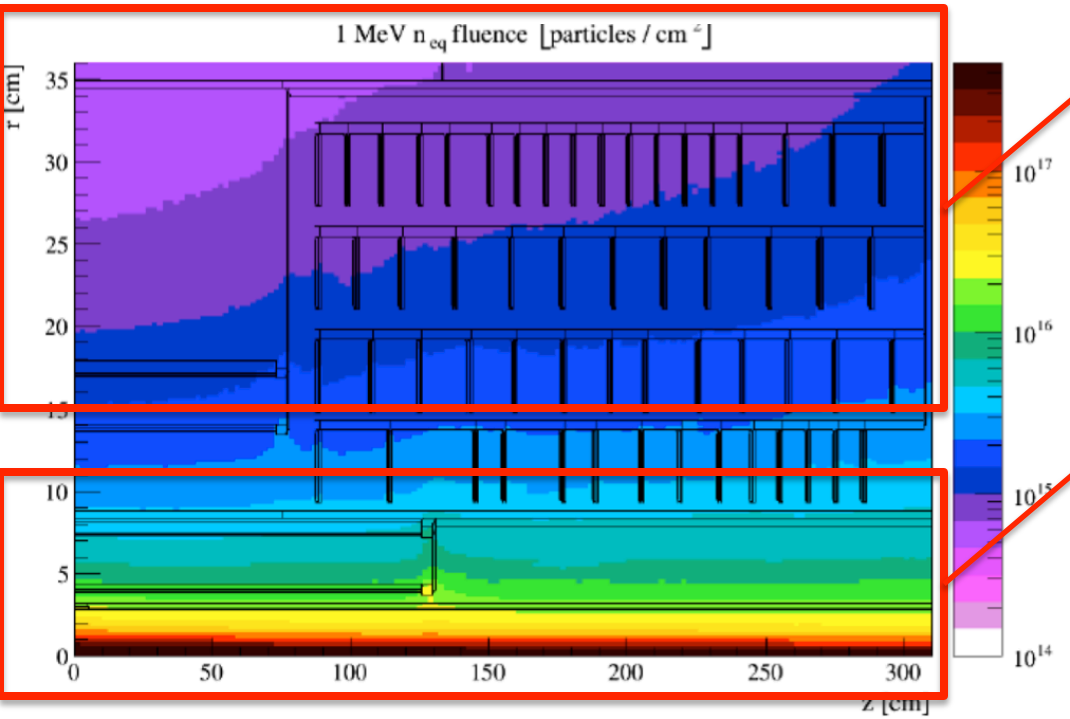
# Monolithic CMOS Pixels for pp-collisions at HL-LHC?

# CMOS Pixel Collaboration

- Collaboration of ~25 ATLAS ITK institutions

# The ATLAS environment at HL-LHC

- Given by ATLAS radiation level, hit rates and bunch structure for ITK Pixel detector
  - 25ns BC
  - L1 trigger rate 4MHz



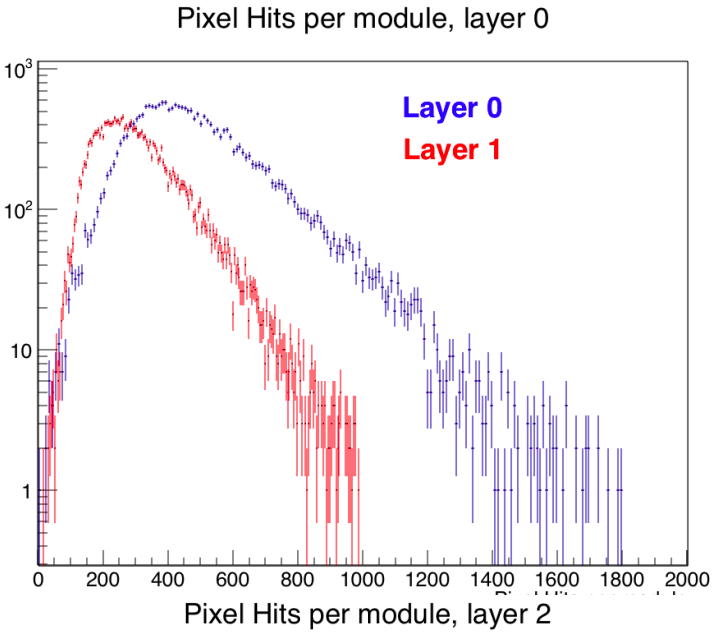

- Outer layers
  - NIEL ~ $10^{15}$ neq/cm$^2$
  - TID ~ 50Mrad
  - Larger area O(10m$^2$)
- Inner layers
  - NIEL ~ 5x$10^{15}$ to $10^{16}$ neq/cm$^2$
  - TID ~ 1Grad
  - Smaller area O(1m$^2$)

# Hitrates per module in different layers

- μ=200
- Pixel 50x50x (150μm depletion)
- Module size 33.8mm (phi) x 40.3mm (z) (or 16.9x40.3 for L0)
- Look at average number of hits per module or per column per BC

- **<hits/mod> Layer 0 = 464 and Layer 1 = 289**
- **<hits/mod> Layer 2 = 59, Layer 3=40 and Layer 4 = 29**
- **Tails up to 4x average**

| | Average channel Hit rate /mm2 per BC at μ=200 |
|---|---|
| Layer 0 | 0.68 |
| Layer 1 | 0.21 |
| Layer 2 | 0.043 |
| Layer 3 | 0.029 |
| Layer 4 | 0.021 |



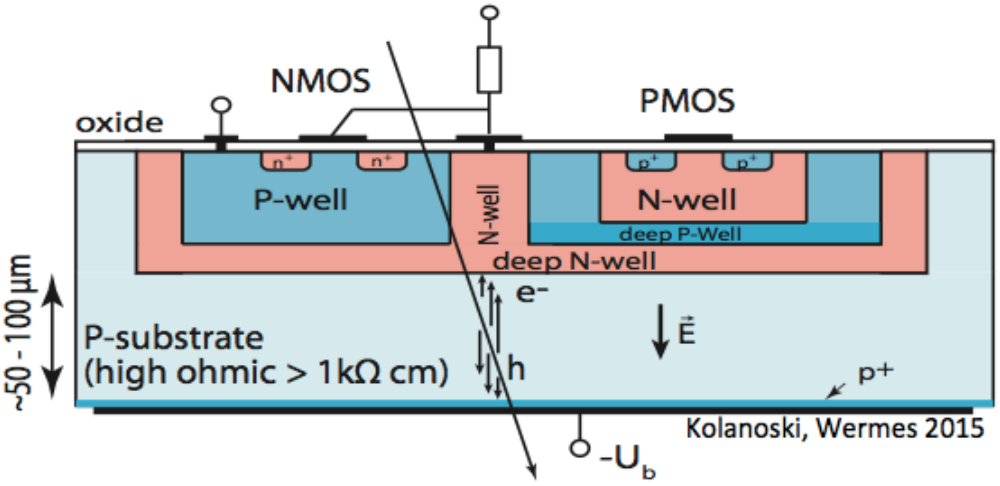

Roland Jansky (Innsbruck)

# CMOS Pixel Sensors for HL-LHC

- **Radiation hardness: develop CMOS sensors that…**
  - Collect charge by drift – not diffusion!
  - Analog designs : Demonstrated radiation hardness to ATLAS levels ($10^{14}$ to $10^{15}$ to $10^{16}$ $n_{eq}/cm^2$) and fast (25ns BC)
- **Digital integration of complex readout architectures with ATLAS specs in monolithic sensors**
  - Implementing full readout architecture into limited space of pixel (50x50um)
  - Avoid cross-talk from digital activity into sensor part/analog section
- **System Integration of CMOS sensors to modules**
  "Drop-in" Quad modules using CMOS sensors
  - Demonstrate assembly and QA on module & stave level
  - Compatible with mechanical, thermal and electrical ITK Pixel system design

# Depleted CMOS sensors

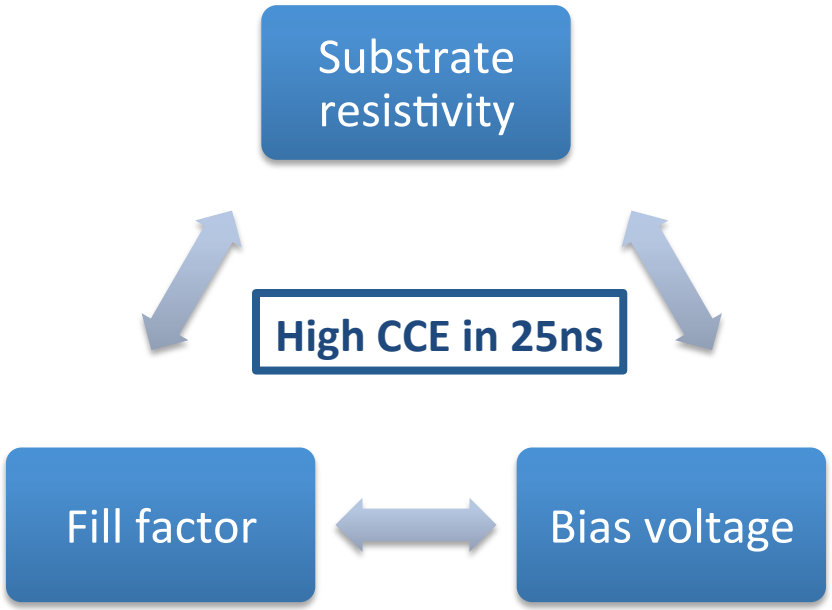
- To overcome the limitations of "classic" MAPS we need depletion
- Depletion = fast charge collection (25ns BC)
- Depletion = less charge trapping after irradiation (>$10^{15}$ $n_{eq}/cm^2$)
- **Promise for radiation hard and fast CMOS sensors**




- Create a large depleted volume under n-well -> this serves as volume for particle detection
- Electronics is include in sensor pixel -> "Smart Pixel" allows processing of information on sensor
- **Depleted Monolythic Active Pixel Sensor (DMAPS)**

# Combine high resistivity and high voltage

- We need to optimize the charge collection for
  - Fast charge collection to avoid trapping after irradiation
  - Large depletion region for high(er) signals




- **Combine HR & HV** to get large depleted volume with fast charge collection by drift
- Aim at depletion region of 40 to 80 μm (~4000 e-)

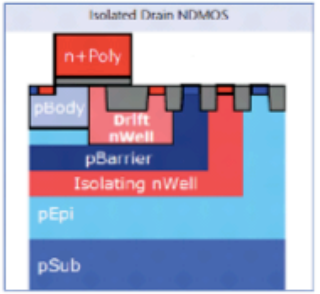
$$d \propto \sqrt{\rho V}$$

- High Q/C -> high voltage swing on input amplifier (detection of signals from thin depletion layers if C small)
- 25ns in-time efficient
- Reasonable short drift paths to avoid large trapping after irradiation

# Enabling technologies

- The design of Depleted Monolithic Active Pixel Sensors relies on several process technologies:

| | |
|---|---|
| **"High" Voltage add-ons** | Special processing add-ons (from automotive and power management applications) **increase the voltage handling capability** and create a depletion layer in a well's pn-junction of o(10-15 µm). |
| **"High" Resistive Wafers** | 8" hi/mid **resistivity** silicon wafers accepted/qualified by the foundry. Create depletion layer due the high resistivity. |
| **Technology features (130-180 nm)** | Radiation hard processes with **multiple nested wells**. Foundry must accept some process/DRC changes in order to optimize the design for HEP. |
| **Backside Processing** | Wafer thinning from backside and backside implant to fabricate a **backside contact** after CMOS processing. |

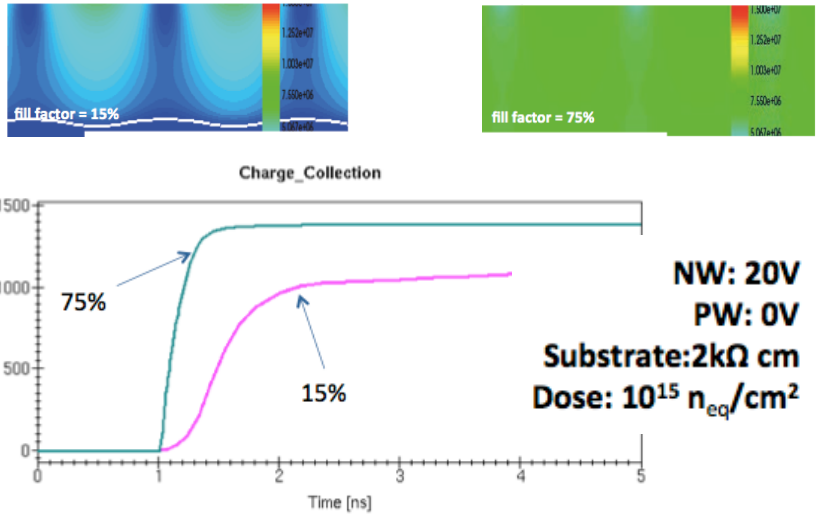



*from: www.xfab.com*

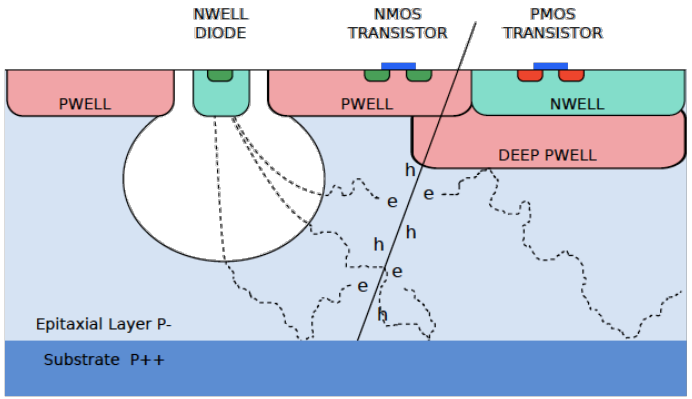
# Analog design & Fill factor

- **Large fill factor**
  - Uniform charge collection
  - Large capacitance (~50-200 fF) on CSA
  - More power necessary to achieve fast signals with reasonable amplitude

- **Small fill factor**
  - Higher gain and faster response due to smaller capacitance (2-5fF) and higher Q/C
  - Potentially lower power consumption
  - Signal collection under DPW after irradiation more difficult on edges

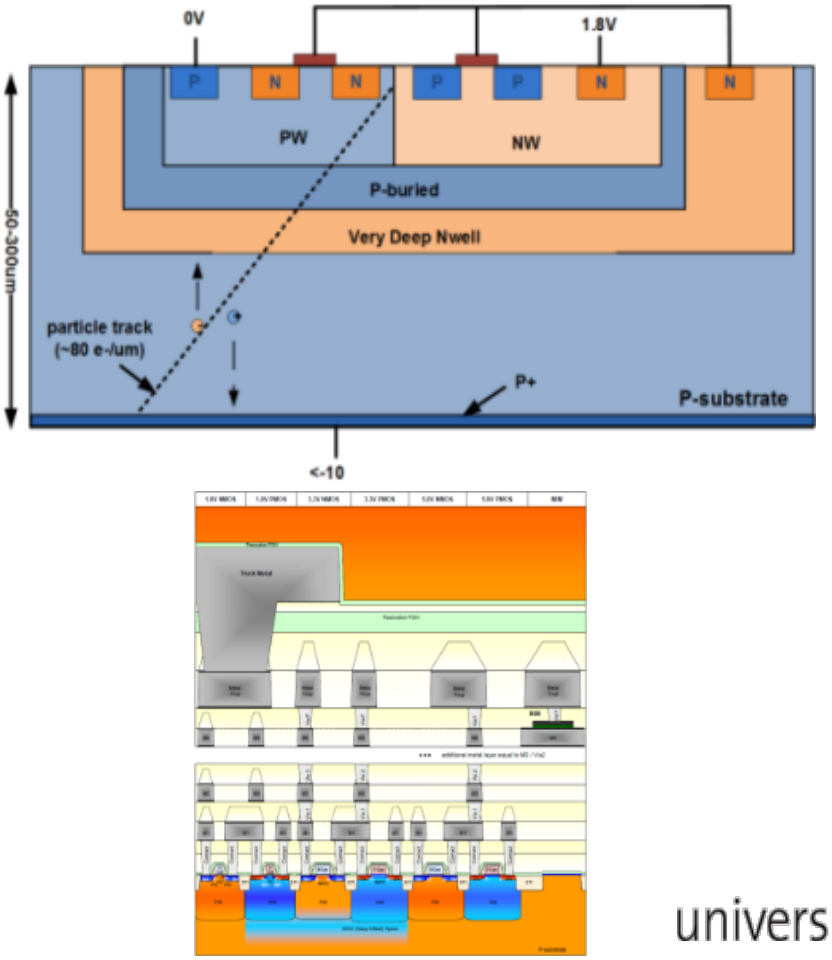



T. Hemperek, H. Krueger / Bonn




Schematic cross-section of CMOS pixel sensor (*ALICE ITS Upgrade TDR*)

# Large electrodes pixel sensors in LFoundry



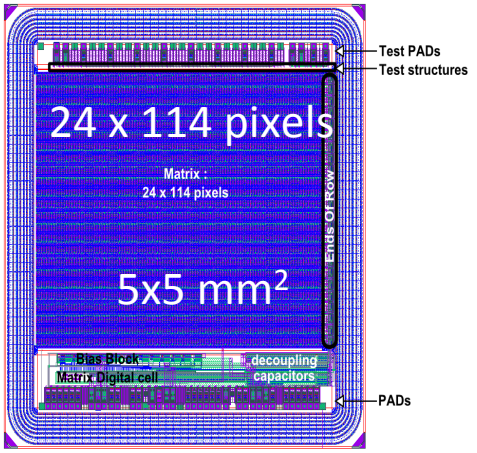

**LFA150:**

- L-Foundry 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- Resistivity of wafer: **>2000 Ω·cm**
- Small implant customization
- Backside processing

**CCPD_LF prototype:**

- Pixel size: 33um x 125 µm (6 pix =2 pix of FEI4)
- Chip size: 5 mm x 5 mm (24 x 114 pix)
- Bondable to FEI4 (+pixel encoding)
- **300um and 100um** version
- Bonn + CCPM +KIT

universitätbonn

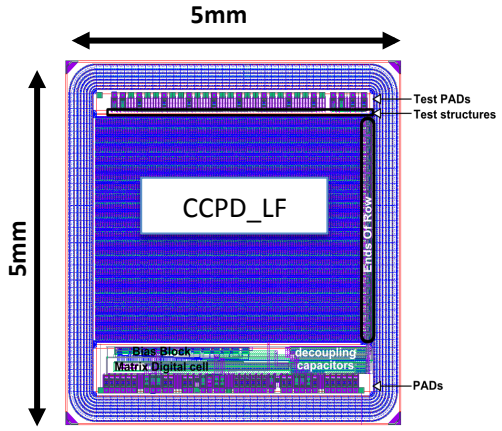



P. Rymaszewski et al., JINST 11 (2016) 02 C02045
T. Hirono et al., doi:10.1016/j.nima.2016.01.088

# LFoundry development line

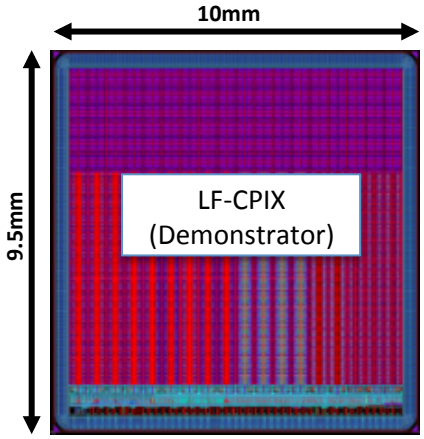
## CCPD_LF

- Subm. in Sep. 2014
- 33 x 125 µm$^2$ pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test
- ***(Almost) Fully characterized***



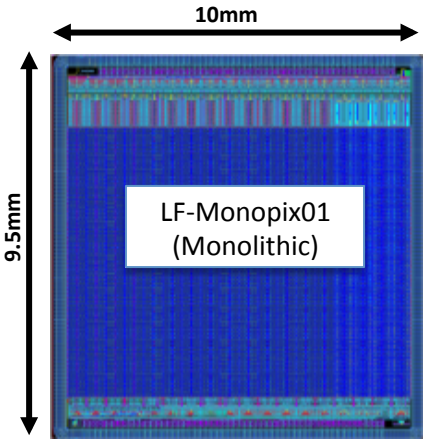

## LF-CPIX (DEMO)

- Subm. in Mar. 2016
- ***CPIX demonstrator in LF***
- 50 x 250 µm$^2$ pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test
- ***First meas. available***




## LF-Monopix01 (monolithic)

- Subm. in Aug. 2016
- "Demonstrator size"
- 50 x 250 µm$^2$ pixels
- ***Fast standalone R/O***
- Standalone R/O like LF-CPIX



# 3.2GeV electrons beam tests

## Large Fill Factor Cell

- **Version A**
  - Bias: 110V (4nA)
  - Pixel: CSA ELT
  - Source: $^{55}$Fe

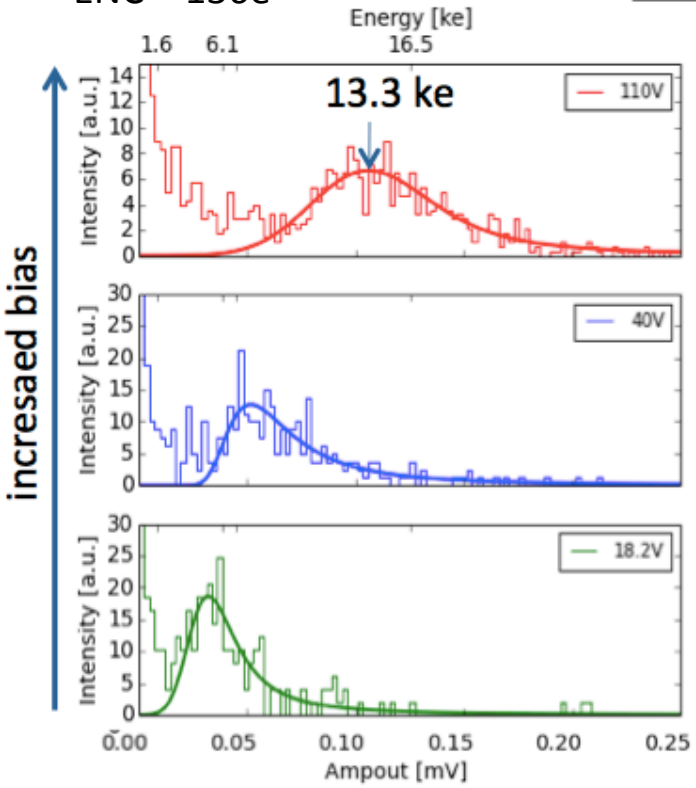

## Medium Fill Factor Cell

- **Version B**
  - Bias: 20V (39nA)
  - Pixel: HV connection Diode, CSA ELT, PSUB everywhere
  - Source: $^{55}$Fe

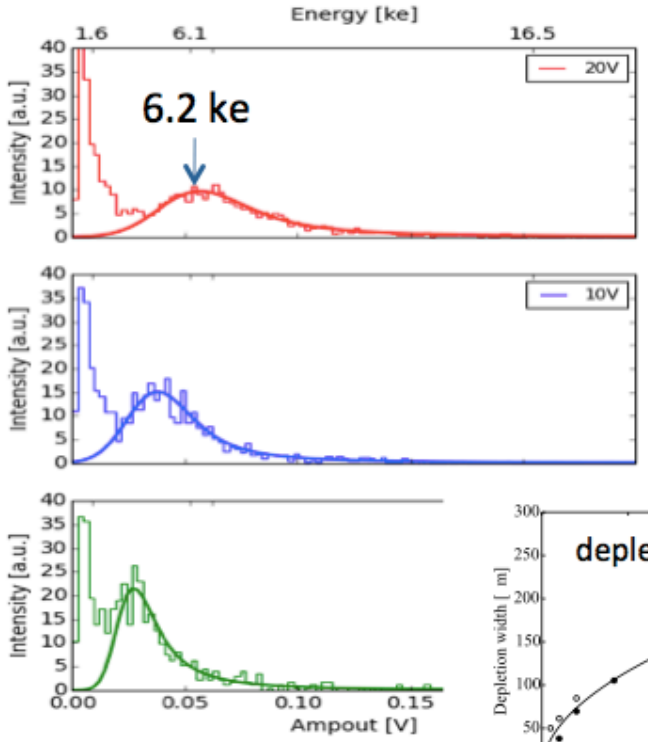

ENC ~ 136e-

before thinning: ~700 µm

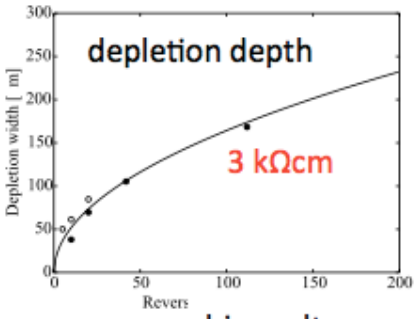
ENC ~ 100e-




i.e. ~166 µm depl. depth




i.e. ~86 µm depl. depth



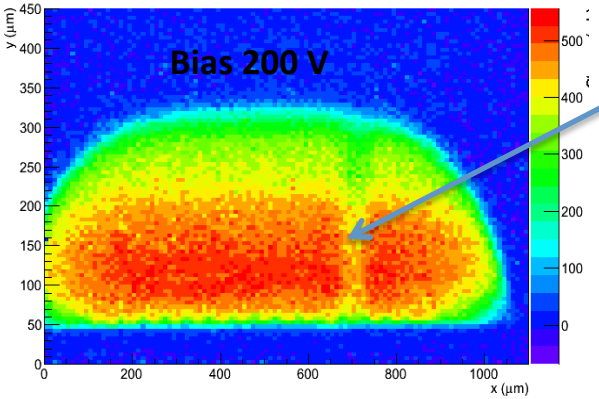

T. Hirono

test beam @ ELSA/Bonn

# Edge-TCT measurements on LFounrdy CPIX

Institut "Jožef Stefan" Ljubljana, Slovenija

I. Mandic, B. Hiti (Ljubljana)

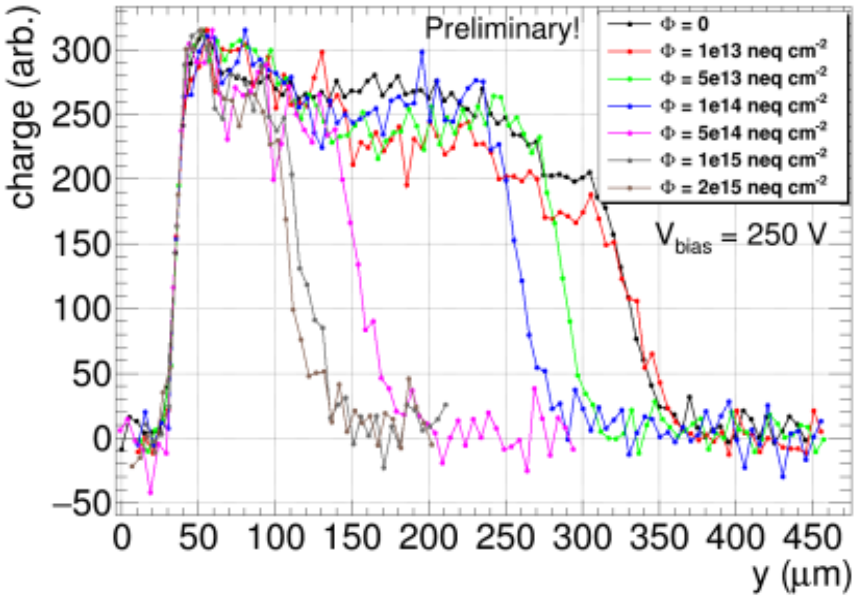


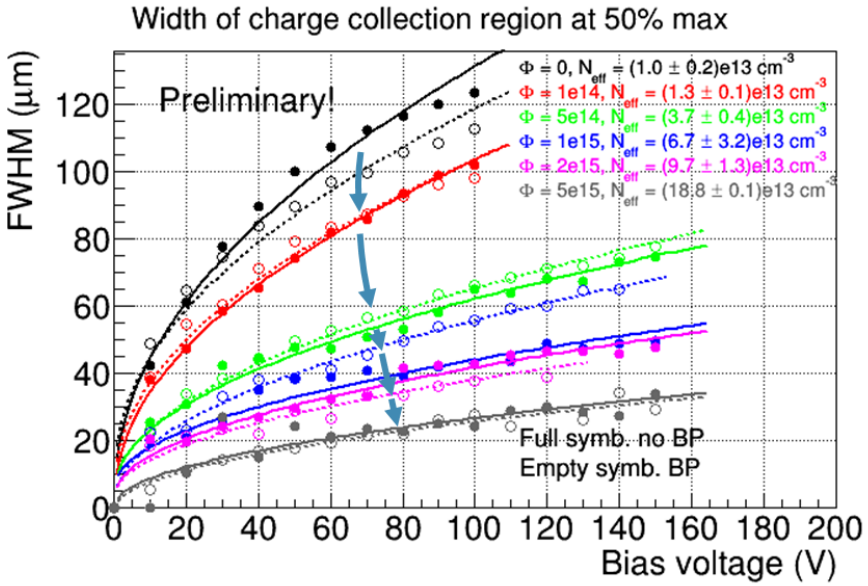

***Unconnected pixel***

**Charge profile width vs. bias voltage**

**Neutron irradiated CPIX sensors up to 2x10$^{15}$ neq/cm$^2$**

$w_0$ and ***$N_{eff}$*** free parameters $Width(V_{bias}) = w_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{e_0 N_{eff}} V_{bias}}$

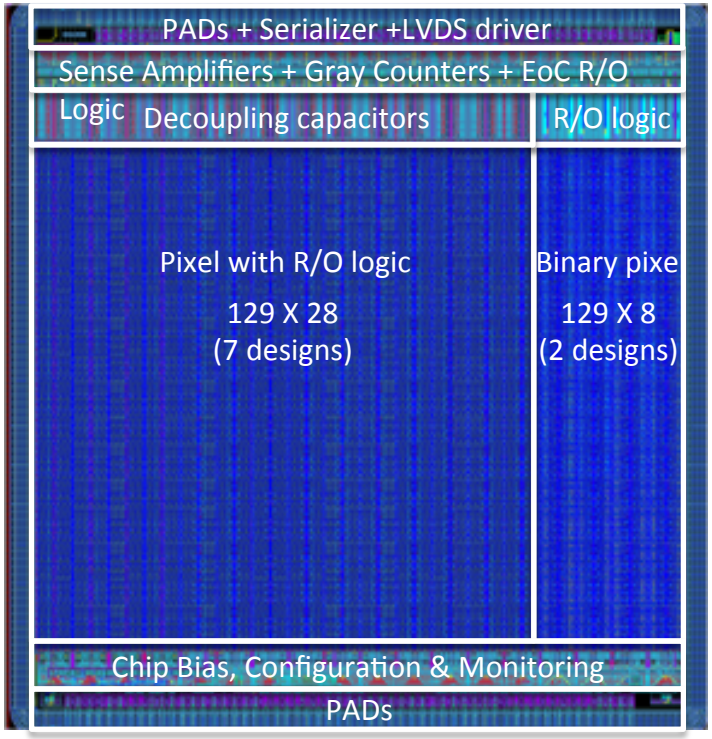


# DMAPS in LFoundry - LF-Monopix01

## Chip overview

- Large input from LF-CPIX: pixel, floor plan…
- 9 flavors for comparative studies **=>**
- **each 4 col.**
  - Pixel with R/O logic (FE-I3 like pixel)
    - ❑ NMOS/CMOS pre-amp.
    - ❑ Different power domains for discri.
    - ❑ CS /CMOS token transmission
  - Binary pixel with R/O logic at column end
    - ❑ faster pre-amp. & discriminator

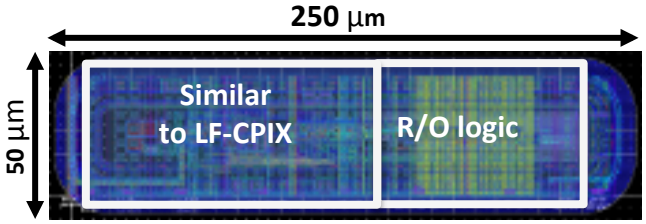


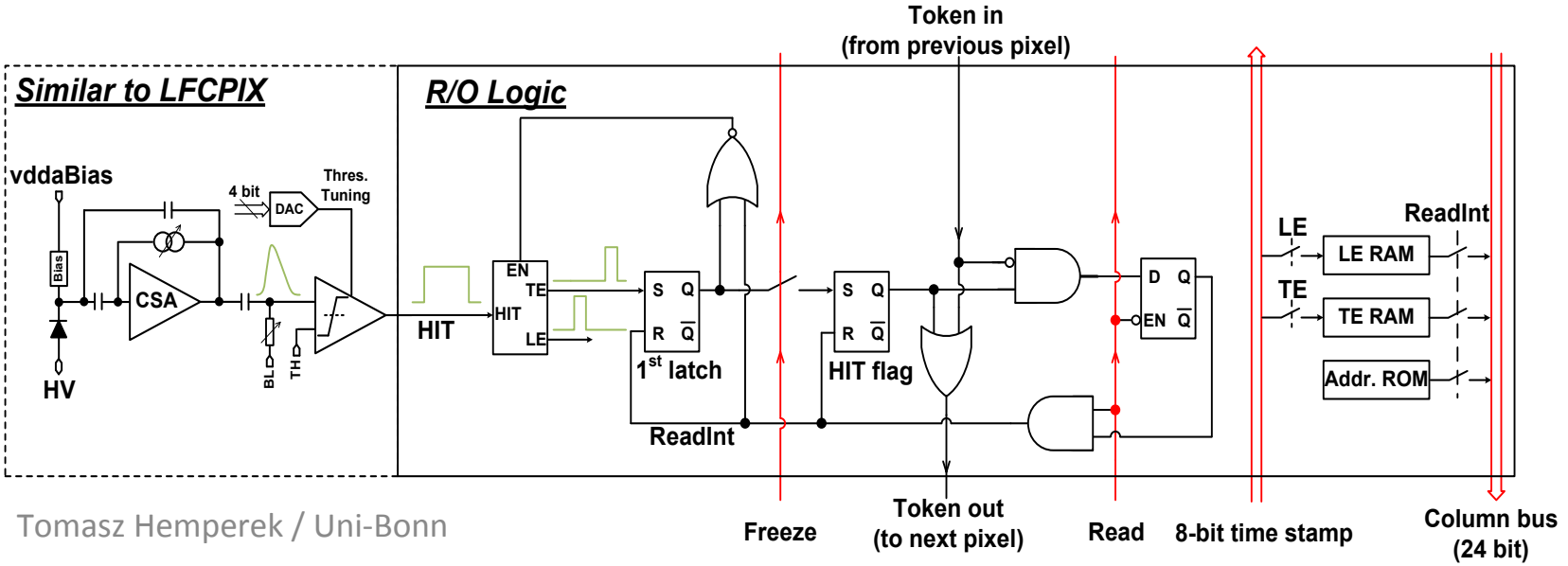

Tomasz Hemperek / Uni-Bonn

- Many design efforts to meet the challenges in terms of **noise and timing**
  - ❑ full-custom in-pixel digital circuit & low noise digital block

# LF-Monopix01: key design ingredients

- **Pixel design**
  - Pixel with R/O logic **=> FE-I3 like pixel**



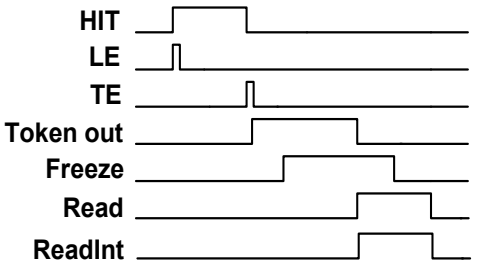

Tomasz Hemperek / Uni-Bonn

- R/O logic fitted inside the LF-CPIX pixel
- Larger detector capacitance & More cross talk

  **=> full-custom dig. circuit**

  **=> low noise circuit for critical dig. Blocks**

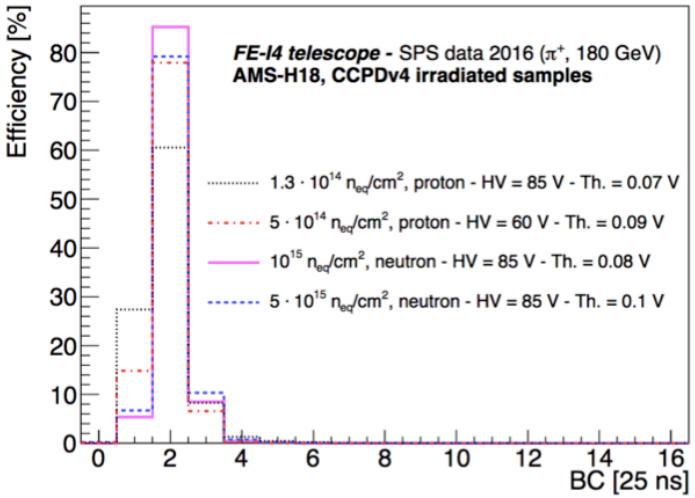
  **=> Very careful layout needed**



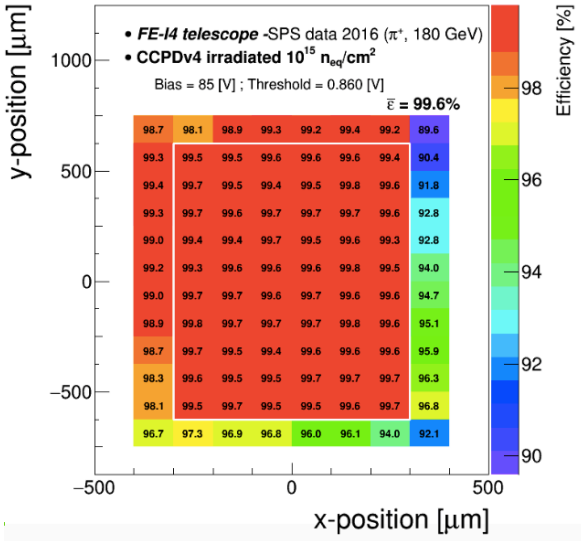
# Large electrodes pixel sensors in AMS

T. Weston/ Uni Bern @ TREDI 2017

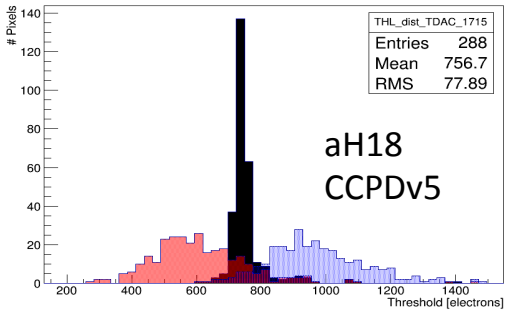
- **Capacitively Coupled Pixel Detectors (H18 AMS process)**
  - Capacitive-Coupling of CMOS sensor to ATLAS FEI4 (sensor pixel size 33x 125um2)
  - Blocks for monolithic design implemented and studied (DAC,Amplifier, Discriminators, Configuration)
  - Efficiency of > 99.5%
  - Signal collected in 3BC




- **H18 CCPDv5**
  - First prototype in aH18 process (Hi-Resistivity wafer processing)
  - Many beam tests carried out to test operation, tuning, achievable threshold and efficiency
    - 600-650e Threshold

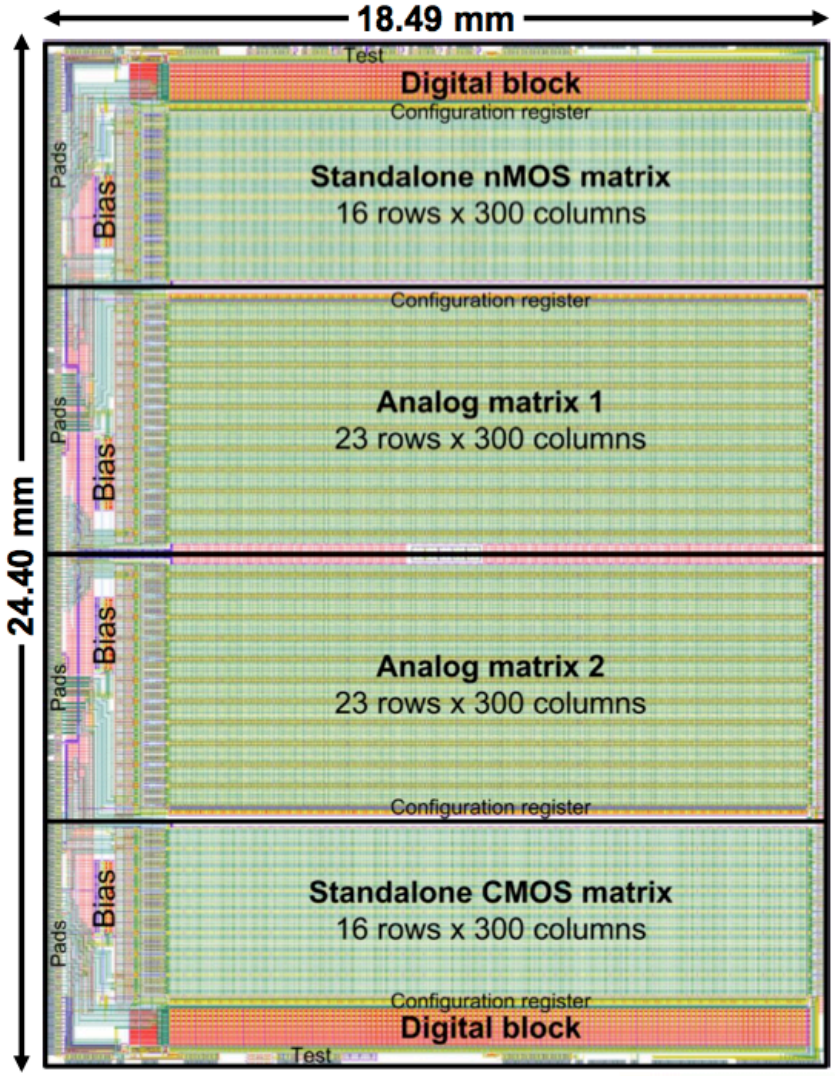



Mathieu Benoit / Uni Geneve




**Threshold before and after equalization**

# AMS H35DEMO sensor




**Main features:**

- ams 0.35 µm HV-CMOS (H35)
- submission through an engineering run
  - submission in October 2015
  - wafer production finished in December 2015
- different substrate resistivities to improve SNR
  - 20 Ω·cm (standard), 80 Ω·cm, 200 Ω·cm, 1k Ω·cm

**Areas (from top to bottom):**

- standalone nMOS matrix
  - digital pixels with in-pixel nMOS comparator
  - standalone readout
- analog matrix (2 identical arrays)
  - different flavours
- standalone CMOS matrix
  - analog pixels with off-pixel CMOS comparator
  - standalone readout
- All pixels are 50 µm x 250 µm for compatibility with FEI4

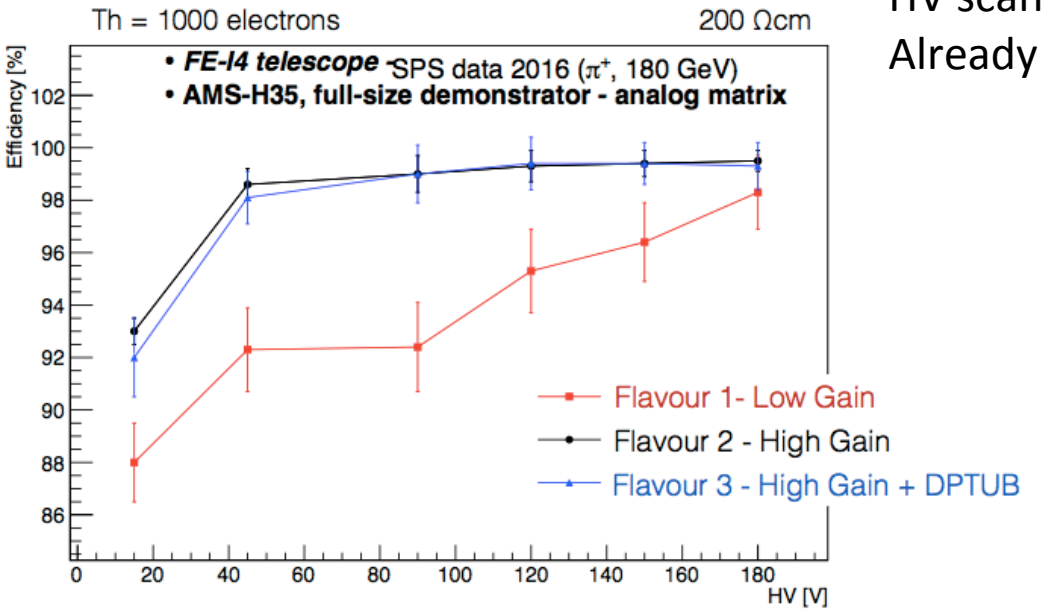
Eva Vilella / Uni Liverpool

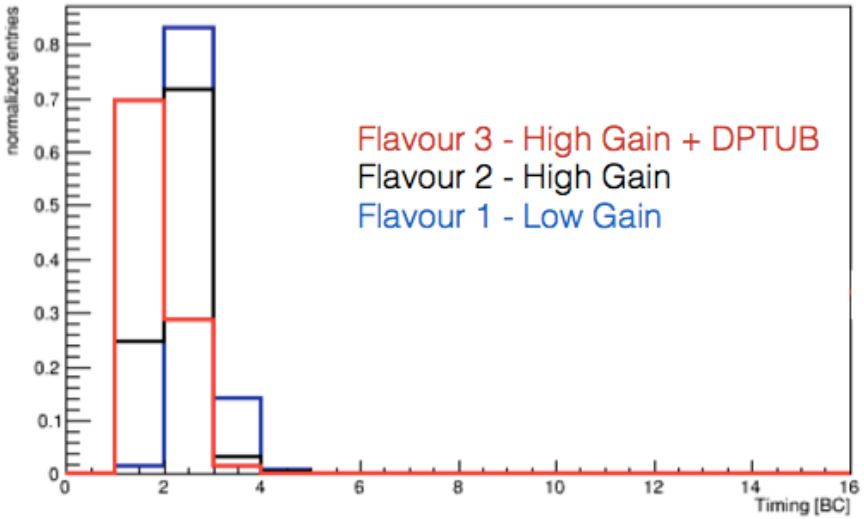
# AMS H35 Demonstrator

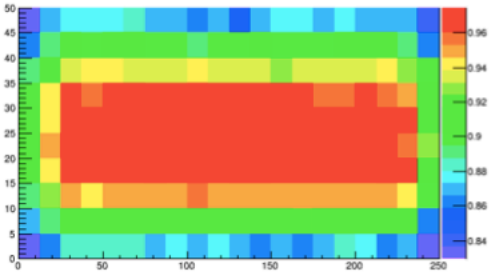


- Beam test results

200 Ω · cm, non-irradiated
HV scan for 3 pixel flavours of Analog matrix
Already from 90V bias, **efficiency of 99%**

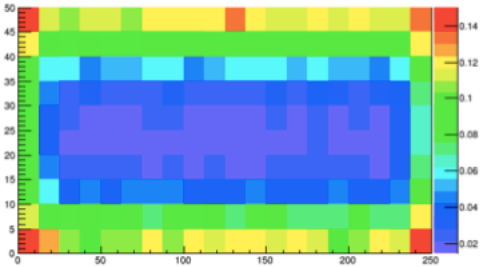


Cluster Size = 1

- Events where 1 pixel fired
- Most collected in centre



Cluster Size = 2

- Events where 2 pixels fired
- Most collected at edges

200 Ω · cm, non-irradiated
**99% of charge collected within 2 BC**
Observe differences in characteristics of each of the pixel flavours

# Changes of Neff in CMOS sensors

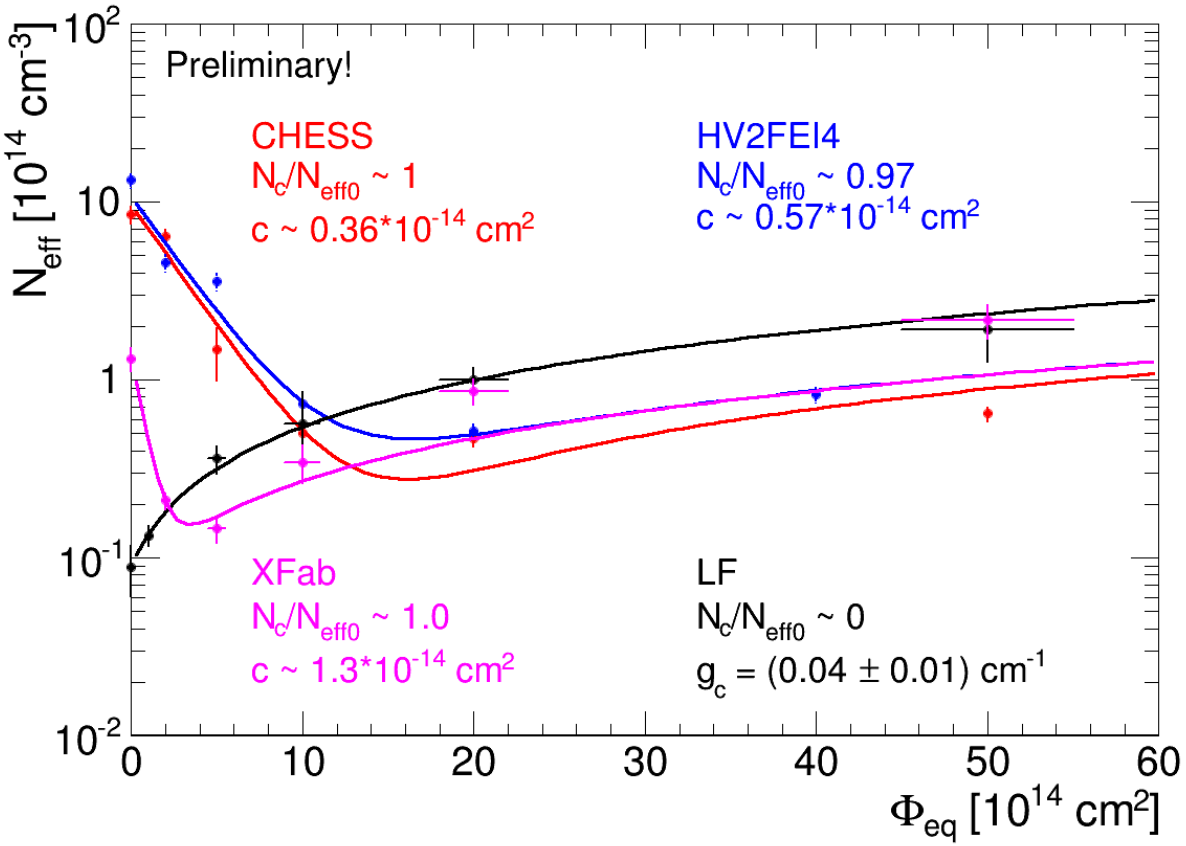
**$N_{eff}$ vs fluence**

acceptor removal

Radiation introduced deep acceptors: $g \sim 0.02$ cm$^{-1}$

AMS and XFab: $N_{eff} = N_{eff\,0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g \cdot \Phi_{eq}$ $N_c$, $N_{eff0}$ and $c$ free parameters, $g$ fixed

LFoundry: no removal ($N_c \sim 0$), fit: $N_{eff} = N_{eff\,0} + g \cdot \Phi_{eq}$ $N_{eff0}$ and $g$ free




AMS
(CHESS and HV2FEI4)
G. Kramberger et al., 2016 *JINST11 P04007*

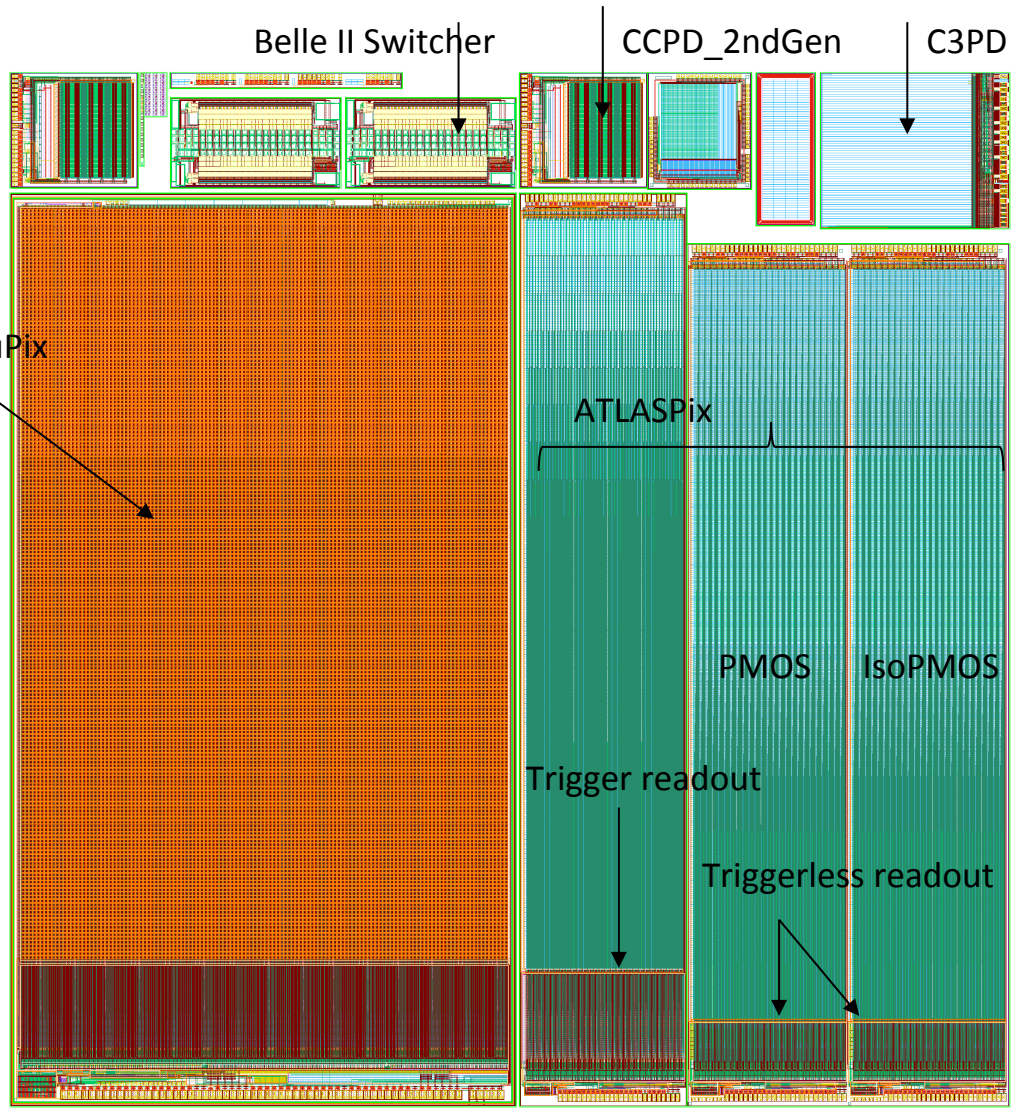
I. Mandic (IJS Ljubljana)

# Monolithic submission in AMS H18

- Combined submission between Mu3e and Atlas
- See presentation about MuPix by F. Meier-

- Project MuPix8/ ATLASPix (2016)
- Technology AMS aH18 (180nm)
- Substrates: 20, 50-100, 100-400, 600-1100 Ωcm
- 4-well HVCMOS process

- Main features (Atlas part):
- Pixel pitch 56x56um
- Asynchronous readout to periphery
- Buffering of hits in pixel (-groups)

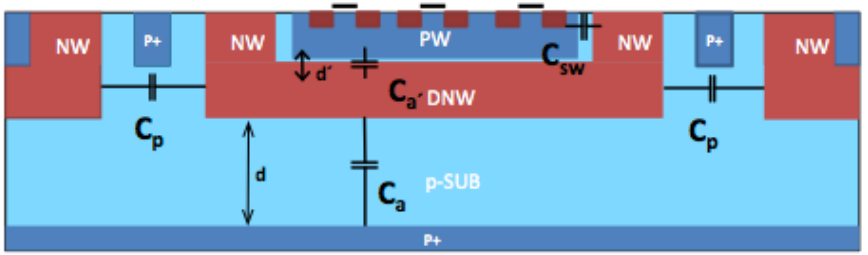



MuPix, ATLASPIX

# Input capacitance is critical

- On sensors described so-fare, the **analog & digitial circuit is placed inside collection well**
- Input capacitance is dominated by additional capacitance between n-well and p-well

hybrid planar pixels (e.g. ATLAS IBL): **Cin = 109 fF**
(Havranek et al, NIMA 714 (2013) 83-89
CMOS pixel extrapolation: **Cin ≈ 200 fF**



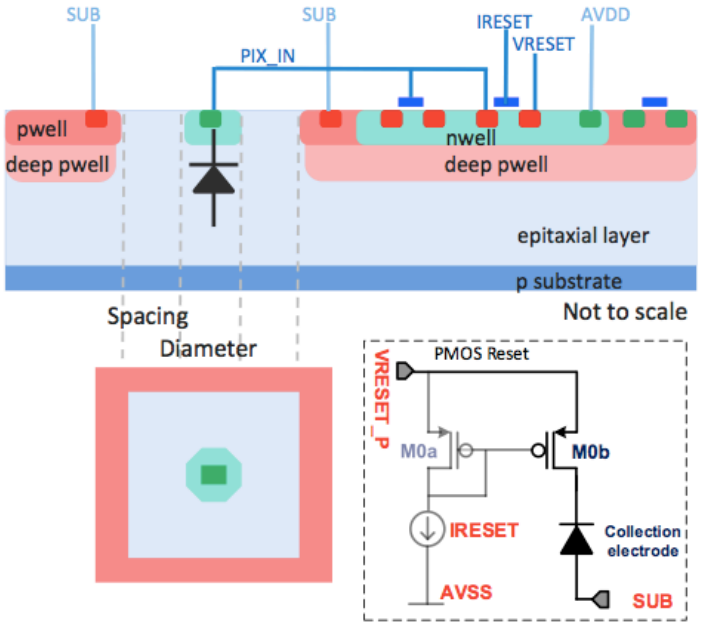

H. Krüger / Bonn

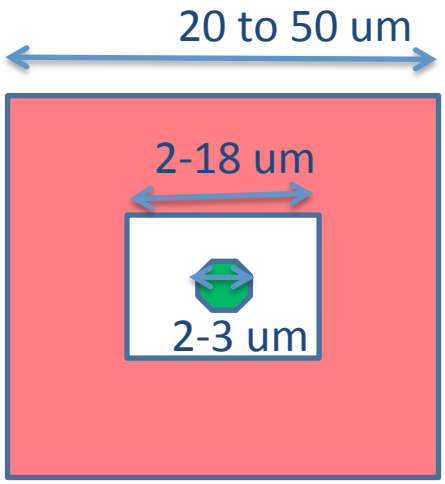
- Response time: $\tau_{OSA} \propto \frac{1}{g_m} \frac{\mathbf{C_d}}{C_f}$
- Noise: $ENC^2_{thermal} \propto \frac{4}{3} \frac{kT}{g_m} \frac{\mathbf{C_d^2}}{\tau}$

Total input capacitance drives peaking time and ENC
Counteract by increasing transconductance – but this increases power consumption significantly

- Additionally digital signals are contained in collection well – hence risk of severe cross-talk of digital signals to collection well
  - Can be minimzed by special source follower (P. Rymaszewski / Bonn)

# TowerJazz 180nm Investigator




- **Pixel dimensions for these measurements:**
- 20x20 to 50x50um pixel size
- **3 um diameter electrodes** 25um EPI layer

**Designed as part of the ALPIDE development for the ALICE ITS upgrade**

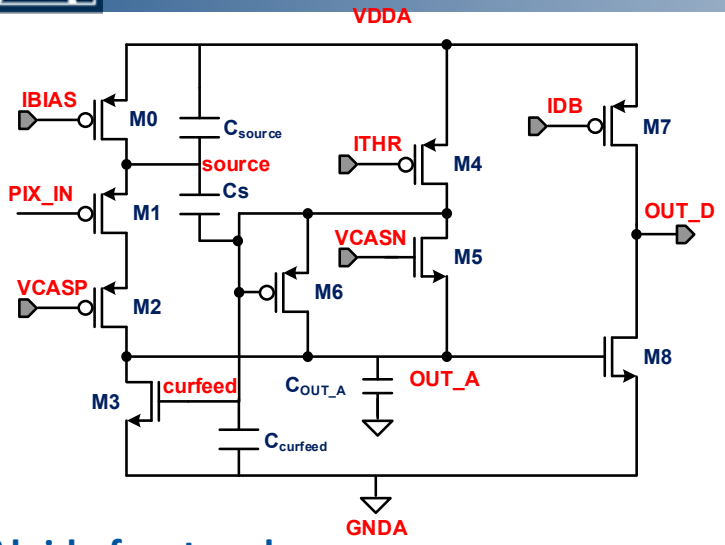
**Emphasis on small fill factor and small capacitance enables low analog power designs** (and material reduction in consequence)

C. Gao et al., NIM A (2016) 831
http://www.sciencedirect.com/science/article/pii/S0168900216300985

**Produced in TowerJazz 180nm on 25-30um thick epi layer**

Design: C. Gao, P. Yang, C. Marin Tobon, J. Rousset, T. Kugathasan and W. Snoeys

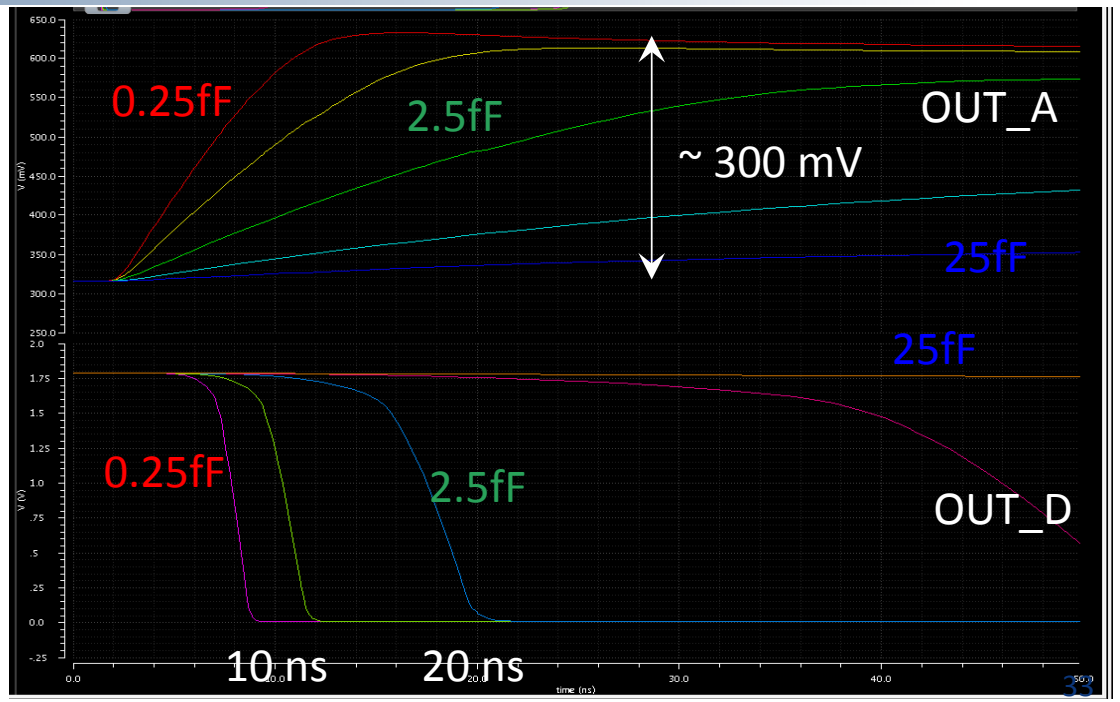
# Smaller capacitance => better Q/C




**Alpide front end**

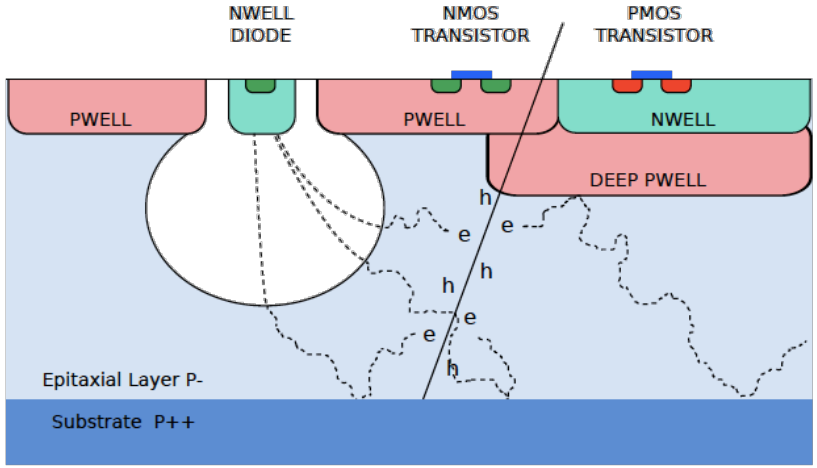
D. Kim et al. TWEPP 2015

T. Kugathasan, W. Snoeys / CERN




- Reducing the detector capacitance **increases the signal amplitude at the input (Q/C) and therefore yields better S/N and faster signal**
- Can be used to **reduce power consumption** (and therefore services and cooling material).
- Simulated a very similar front end increasing power consumption ~ To match ATLAS ITK requirements we use up to 500nA nA (= 70 mW/cm$^2$ for 36 µm pitch) aiming at timewalk of less than 15ns

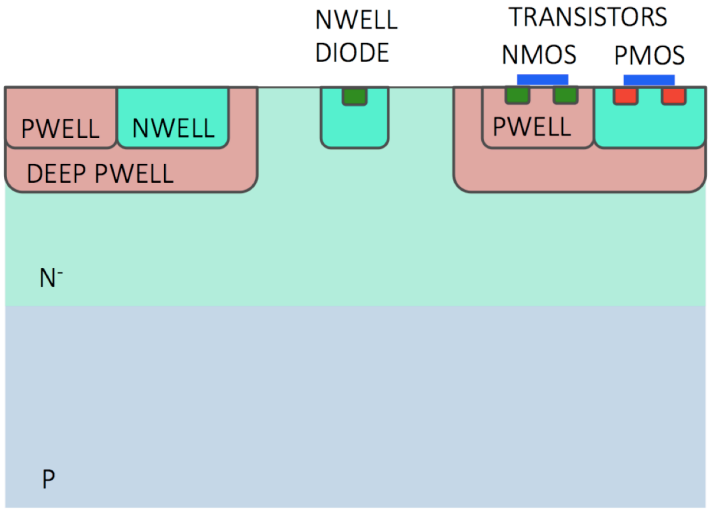
# Small collection electrodes




Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

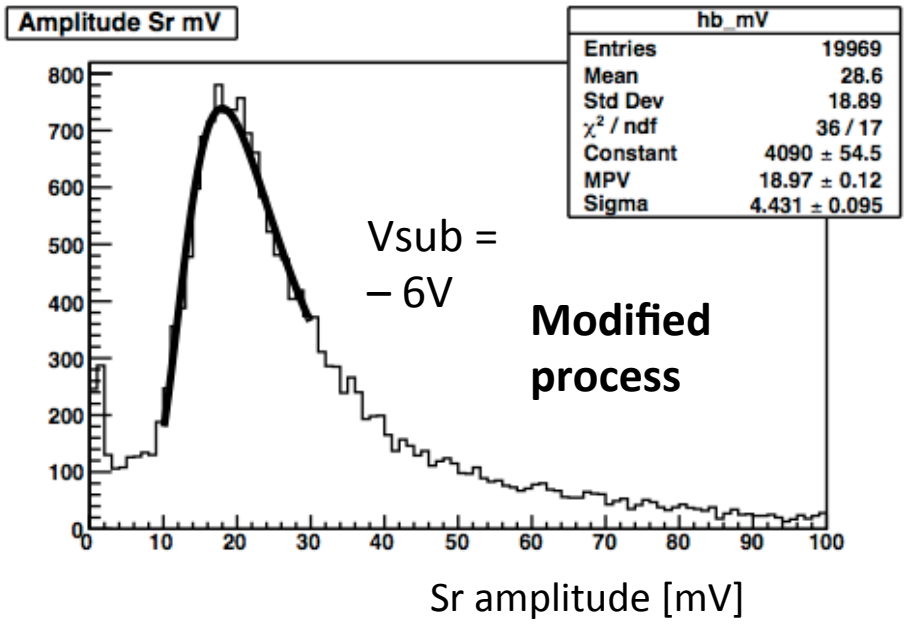
- **Small collection electrodes**
  - Higher gain and faster response due to smaller capacitance (~5fF) and higher Q/C
  - Potentially lower power consumption
  - Signal collection under DPW after irradiation more difficult on edges

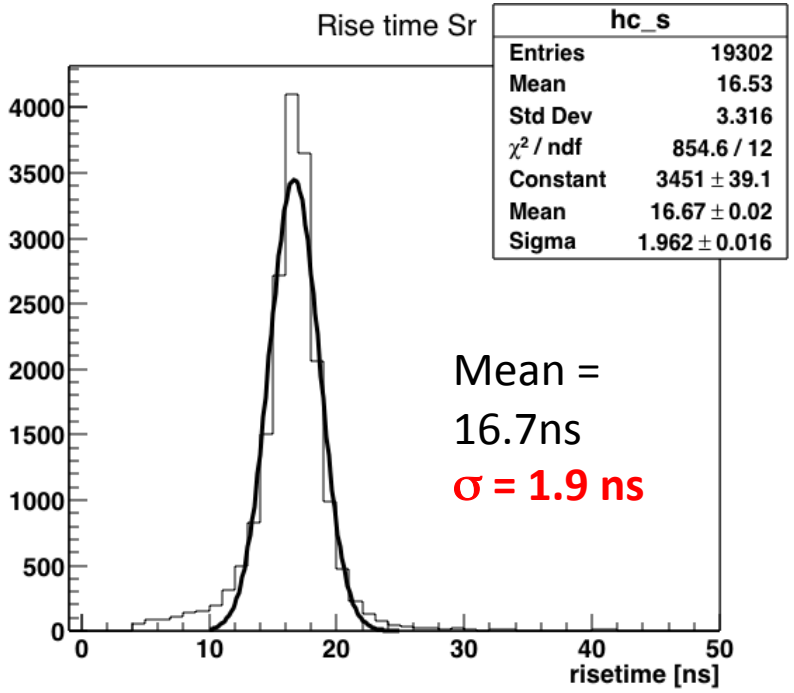
- **Modified Process**
  - Add planar n-type layer
  - Significantly improves depletion under p-well with deep junction
  - Does not require significant circuit or layout changes



# Signal collection for small electrodes

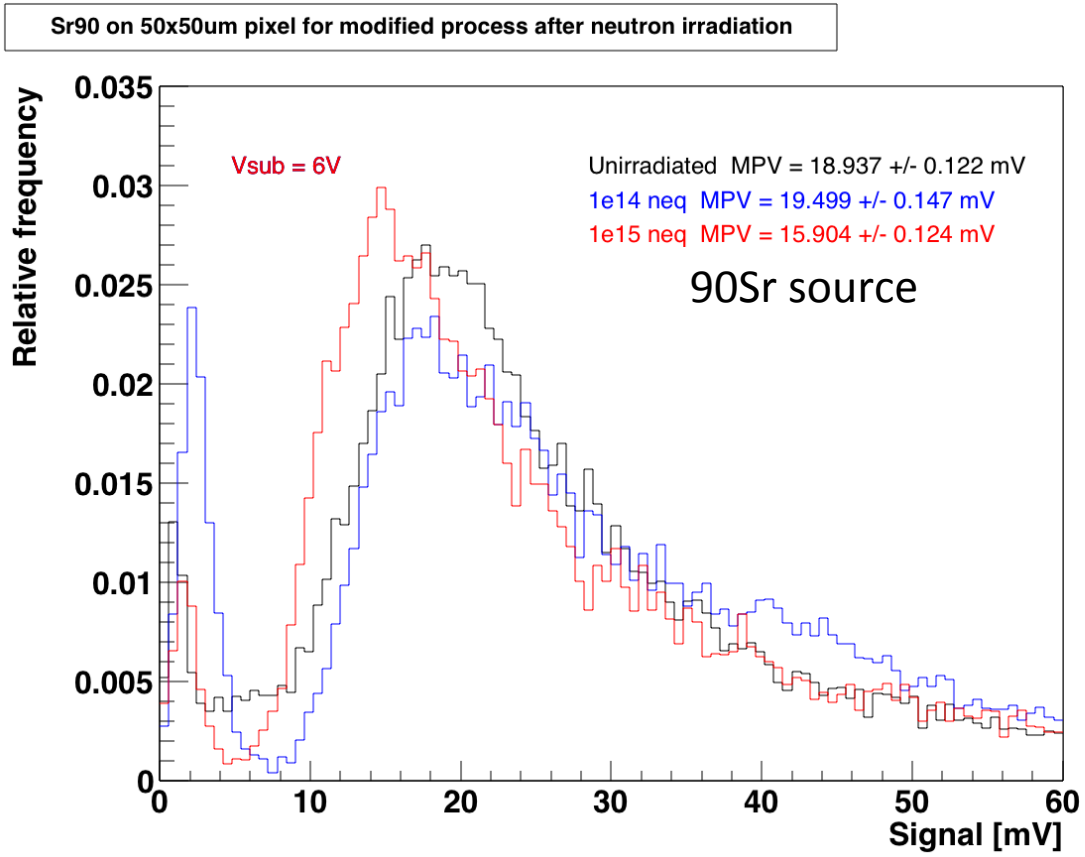
- Normally small electrodes produce weak fields under p-well and charge gets lost after irradiation
- This usually means that efficiency drops significantly towards pixel edges
- **Modified process allows to improve the efficiency after irradiation on pixel edges while keeping small capacitance** which makes this in particular interesting for fast charge collection after irradiation



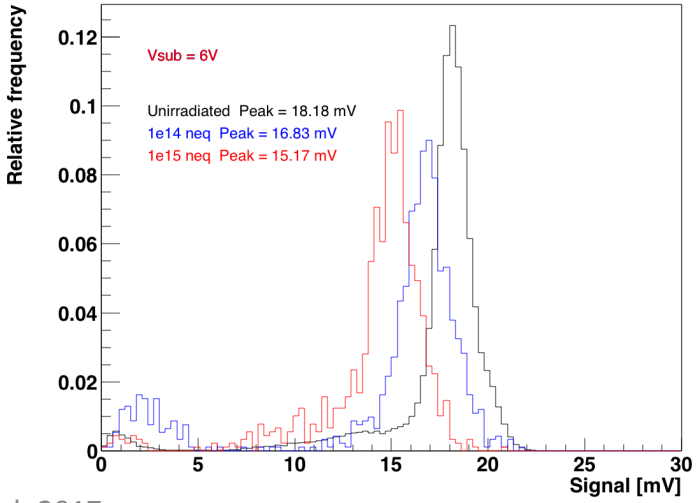
# TJ Neutron irradiation to $10^{14}$ and $10^{15}$ n/cm$^2$

- Investigator irradiated by IJS Ljubljana in several steps up to $10^{15}$
- Measurements up to $10^{16}$ ongoing
- This detector has received NIEL $10^{15}$ n/cm2 and 1Mrad TID



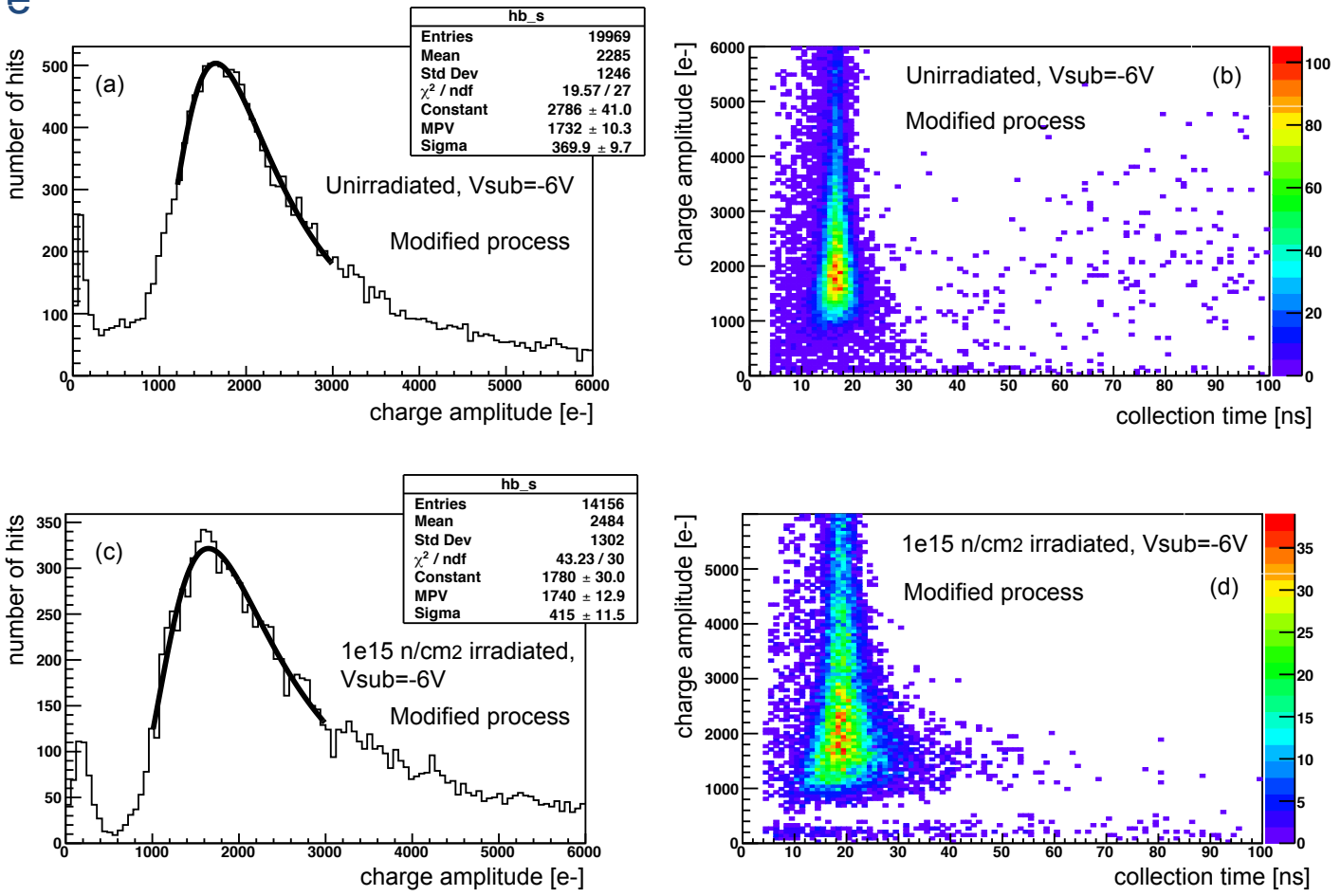

- Little change to signal after irradiation
- Signal well separated from noise

55Fe source



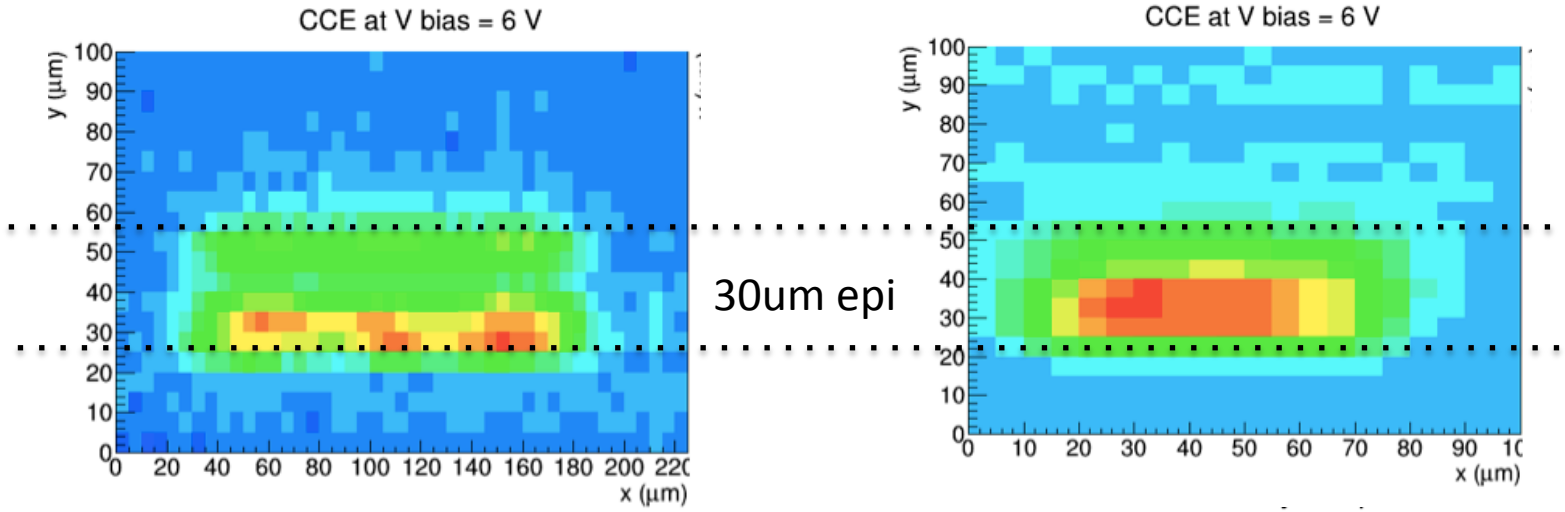
# TJ - Neutron irradiation $10^{15}$ n/cm$^2$

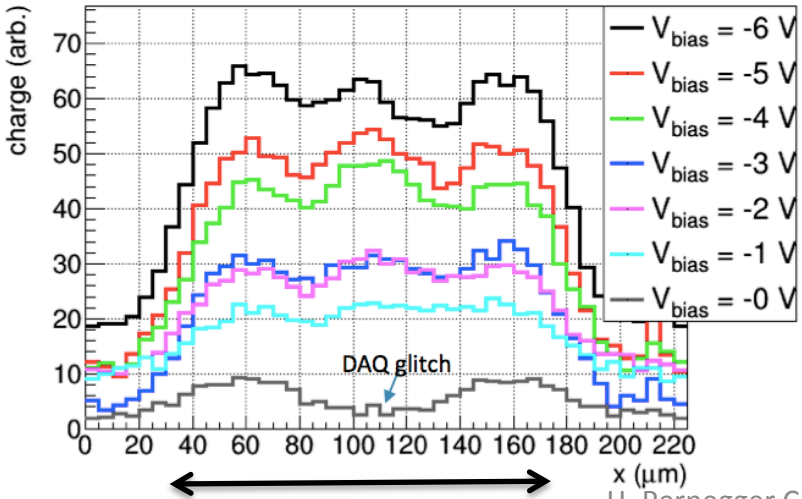
- Plot calibrated signal versus charge collection time on 50x50um pixel pitch
- Very little change is signal response after $10^{15}$ n/cm$^2$
- Standard process after $10^{15}$ n/cm$^2$ does not give measureable signals anymore



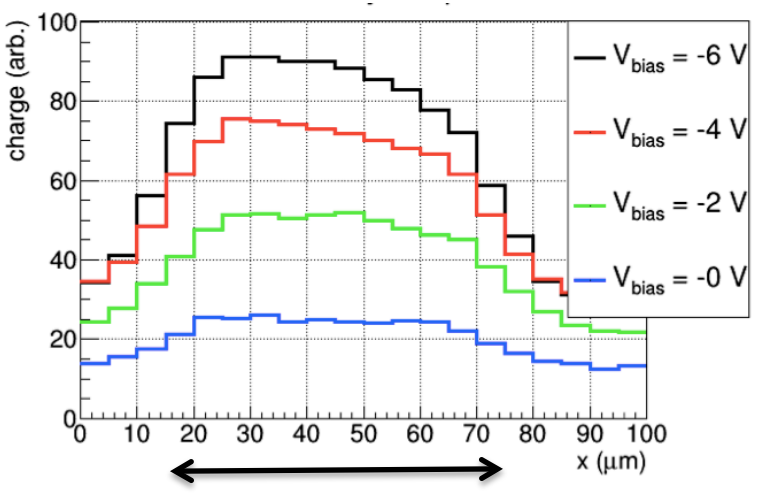
# TJ - Depleted volume after $10^{15}$ n/cm$^2$

- **First preliminary e-TCT measurements** on 20x20 and 50x50um pitch shows depletion of epi even after $10^{15}$ n/cm2 at -6V




3x50um pitch

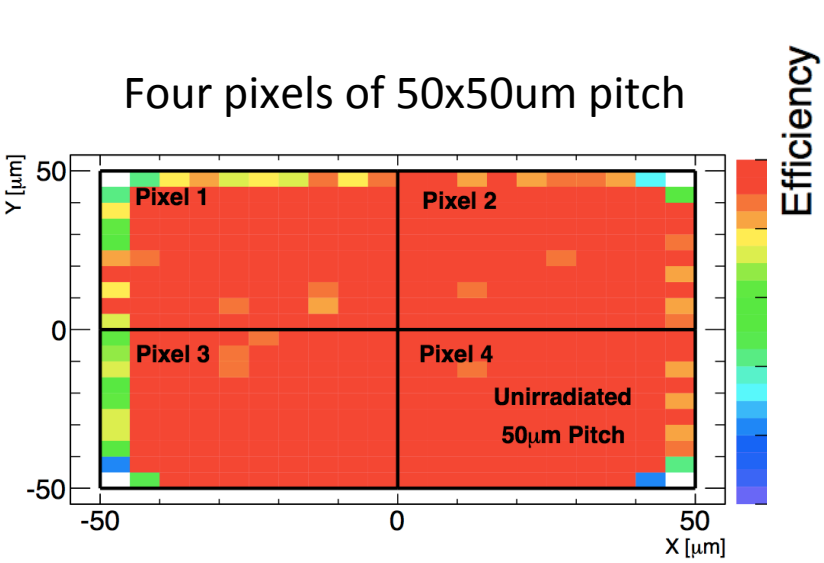


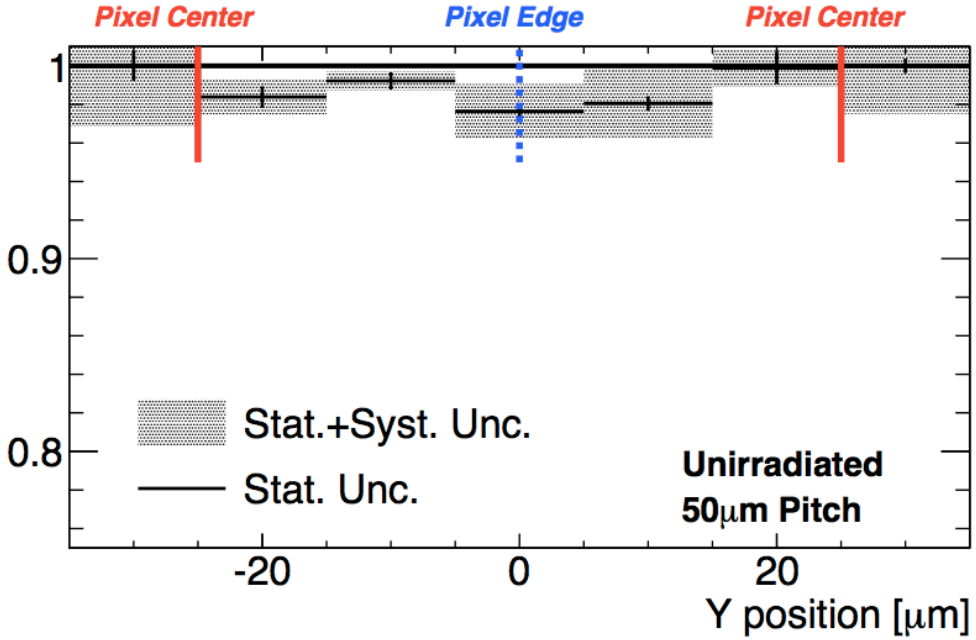

3x20um pitch

Bojan Hiti, Igor Mandic /IJS Ljubljana

# TJ Investigator efficiency

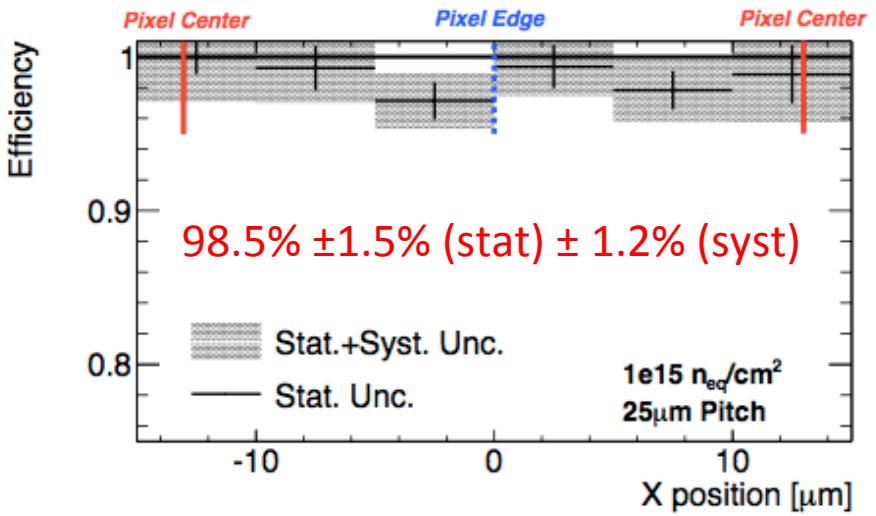
- Unirradiated sensor efficiency 98.5% ± 0.5% (stat) ± 0.5% (syst)
  - slightly reduced efficiency due to high threshold in testbeam (~640e- needed because of common mode noise during measurements)

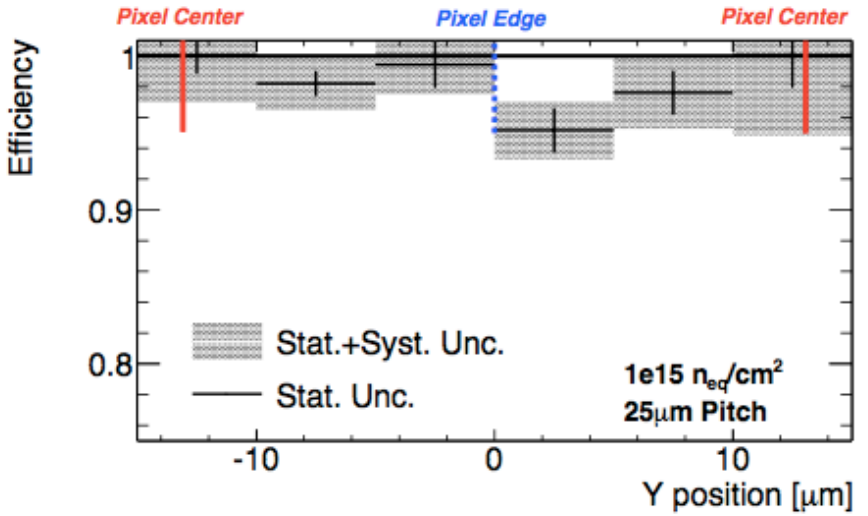


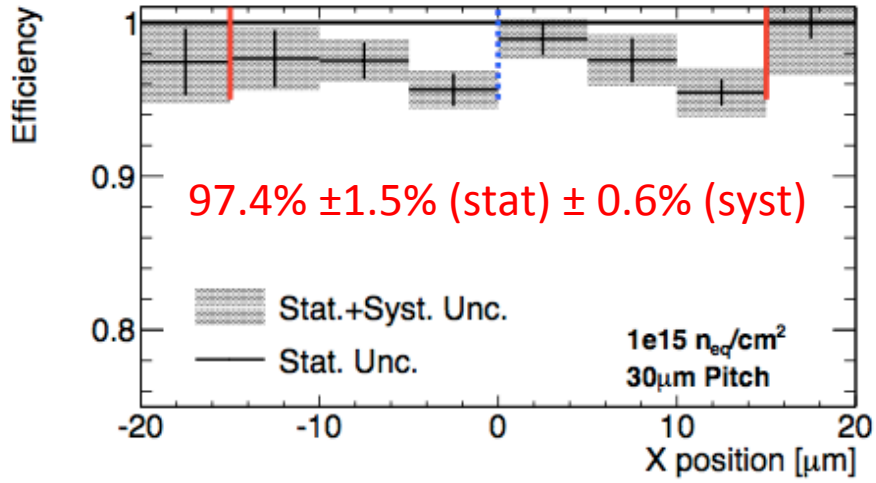



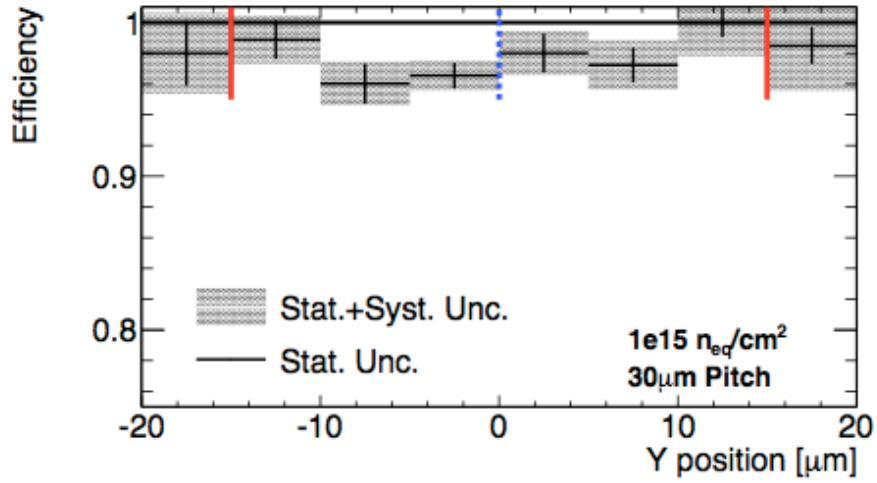
# TJ Efficiency after $10^{15}$ n/cm$^2$

- Irradiated sensor of 25x25 and 30x30um pitch show uniform efficiency across pixel



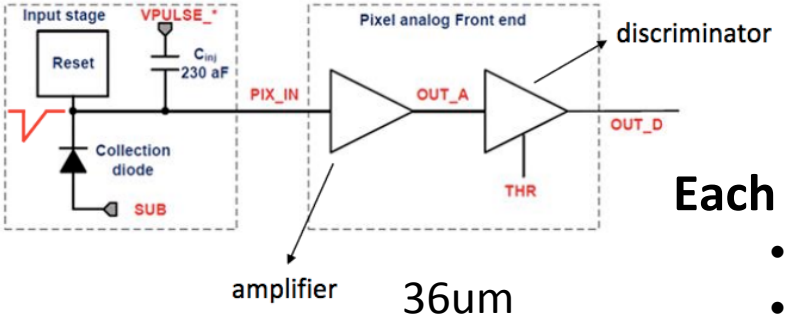
# Full-size ATLAS CMOS Sensor in TJ180

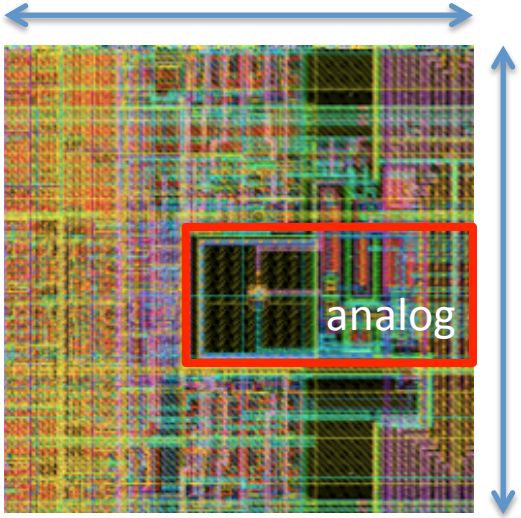
- Measurements show that a **low capacitance and radiation hard** design towards Atlas Outer Layers is possible using a **small-fill factor collection well in the modified TowerJazz 180nm process**

- We have moved now towards a **dedicated full-size monolithic sensor chip design** which matches ATLAS specs
  - Analog front-end with CSA+discriminator tuned optimized for 25ns in-time efficiency and low threshold operation
  - 2x2cm chip size with <50x50um pixels
  - Monolithic design includes readout architecture which copes with ATLAS outer layer hit rate requirement

# Front-end for Atlas

- Prepared two large chips based on Atlas-optimized Front-end design for small fill factor
- **MALTA** chip and **MonoPix** chip




**Each pixel = CSA + discriminator + Flip/flop**

- 36.4 x 36.4 um pixel pitch
- Including analog test pulse
- Including pixel mask
- Diode & PMOS reset implemented
- Discriminator Leading edge output injected to double column pixel logic
- Analog measurement through ToT (LE/TE) or LE time difference to ref signal on periphery
- Bias current 200nA to 500nA can be used to adjust TW range

# Full-size chip Matrix: Two Architectures

- **TJ MALTA**

Full matrix = 512x512 pixels

Design/CERN

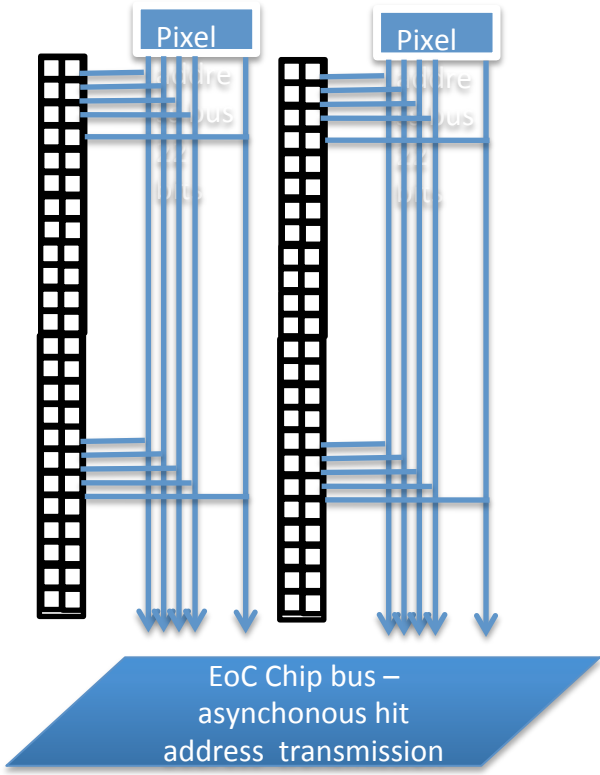
- Active area 18 x 18 $mm^2$
- Hit memory in active matrix
- All hits are **Asynchronously transmitted over high-speed bus** to EoC logic
- **No clock distribution over active matrix** to minimize power and digital-analog cross-talk

- **TJ MonoPix**

512x256 pixels

Design/Bonn

- Active area 18 x 10 $mm^2$
- Hit memory in active matrix (2 flip-flop per pixel)
- **Synchronous column drain architecture**
- Hit address asserted to bus with 40MHz token
- 6 bit ToT coding at end of column

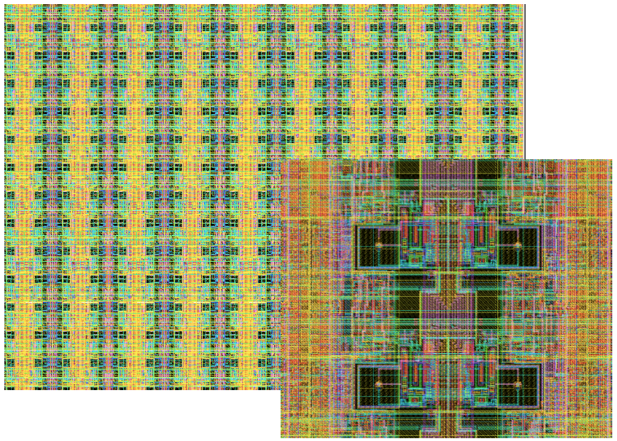



Design Team: W. Snoeys, T. Kugathansan, C. Marin Tobon, I. Berdalovic, R. Cardella, N. Egidos (CERN) J. Rousset, B. Blochet (MIND), K. Moustakas, T. Wang (Bonn)

# Current CMOS RD in ATLAS (2017-18)

## TowerJazz

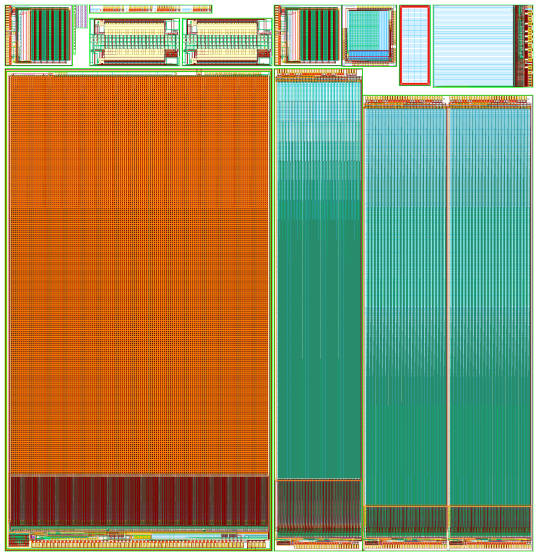
- Subm. in **May. 2017**
- Two large scale demon-strators MALTA and Monopix:
  - 20x20mm and 20x10mm
  - Focus on small FF pixel
  - Asynchronous matrix readout (no clock distribution over the matrix)
  - Column Drain Read-Out (based on Monopix)



## AMS H180

Mu3E + ATLAS (monolithic)

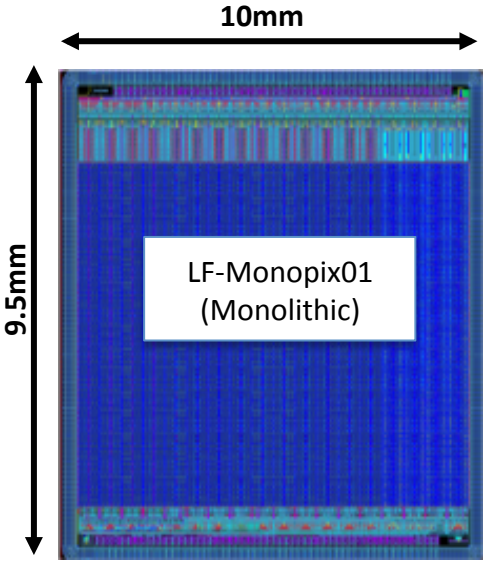
- Subm. In **Jan. 2017**
- Additional production step – isolated PMOS
- 80 and 200 Ohm.cm wafers
- Reticle Size about 21mm x 23mm



## LFoundry

Monopix01, LF2 and Coolpix1

- Received **Apr. 2017**
- "Demonstrator size"
- 50 x 250 μm$^2$ pixels
- Fast standalone R/O



# The Matrix (Pixel Level)

- **All of our present CMOS sensor designs** include for **Each pixel = CSA + discriminator + Hit Memory**
  - Including analog test pulse
  - Including pixel mask
  - Diode or PMOS reset
  - Discriminator with edge output injected to double column pixel logic
  - Hit memory in active matrix
  - Control of bias current (individual or on chip level)
- **Full matrix needs = <512x512 pixels**
  - Cover active area ~18 x 20 $mm^2$ (assuming FEI4-like coverage – tbc by ITK Module)
  - Coarse analog measurement (LE/TE time difference and bunch crossing ref signal on periphery)
  - All pixel addresses with hits are (a)synchronously transmitted over high-speed bus to EoC logic

| CMOS chip | Fill Factor | Pitch [um x um] |
|---|---|---|
| AMS 180 | Large | 56x56 |
| TJ Malta | Small | 36x36 |
| TJ Monopix | Small | 36x40 |
| LF Monopix and Coolpix | Large | 50x250 |
| LF2 | Large | 50x50 |

| CMOS RO | Architecture |
|---|---|
| AMS 180 | Asynchronous |
| TJ Malta | Asynchronous |
| TJ Monopix | Synchronous |
| LF Monopix and Coolpix | Synchronous |
| LF2 | Synchronous |

# ATLAS CMOS monolithic sensor

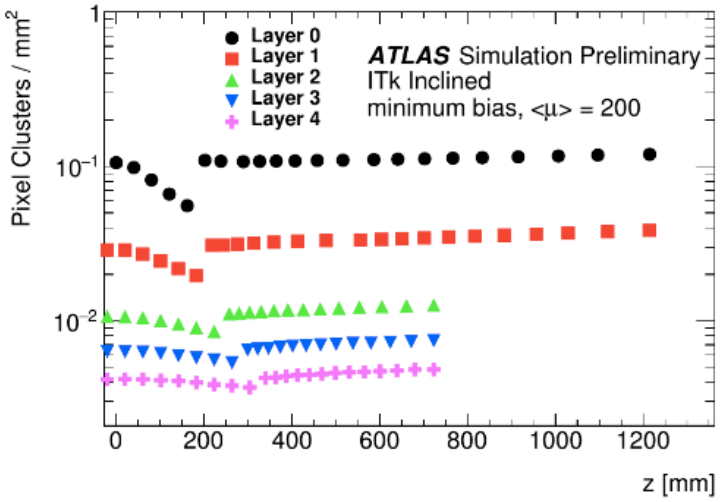
- Follow two main concepts for pixel matrix readout with ATLAS ITK specs for outer layers

1. **Column drain architecture**
   - Token distribution through column, synchronous readout of pixel buffers
   - Include hit buffering (leading edge, trailing edge) in pixel
   - Submission now back: LF MonoPix1 , LF2 and Coolpix 1
2. **Asynchronous hit direct to periphery**
   - Comparator output directly to periphery
   - Buffering and time-stamp at periphery
   - Two submissions in preparation: AMS180/LF150 and TJ180

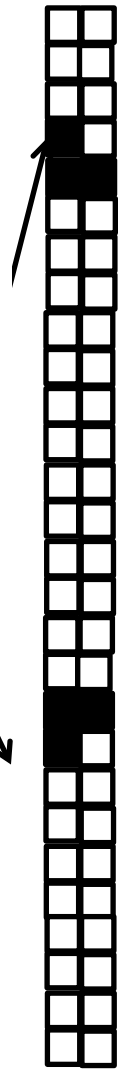
- Main performance criteria that are addressed with these prototyping chips towards ATLAS specifications
  - Hit rate capability
  - Matrix “noise and threshold” performance ( cross talk between sensor analog and digital part)
  - In-time efficiency and time-walk measurements
  - Minimize power consumption in active matrix part
- Provide CMOS sensors for ITK Module Prototypes and System Integration tests

# DC Data transmission – hit loss

- Multiple hits per cluster taken care of by architecture
- **Is there a limitation through th number of clusters in DC?**
  - Average cluster rate 0.003 (L4) to 0.1 (L0) clusters/mm2 per BC
  - Note: results will depend on pixel pitch and buffer logic or pixel sub-grouping
- Check probability to have >1 cluster in DC logic (number e.g. of MALTA)
  - Layer peak cluster rates ~ x5 average rate
  - To accommodate peak rate in outer barrels assume e.g. 2Mclusters/mm2s) anywhere in the half-double-column
  - P(x>1, $\lambda$=0.66mm2*0.05 cluster/ BC*mm2 ) = 0.05%

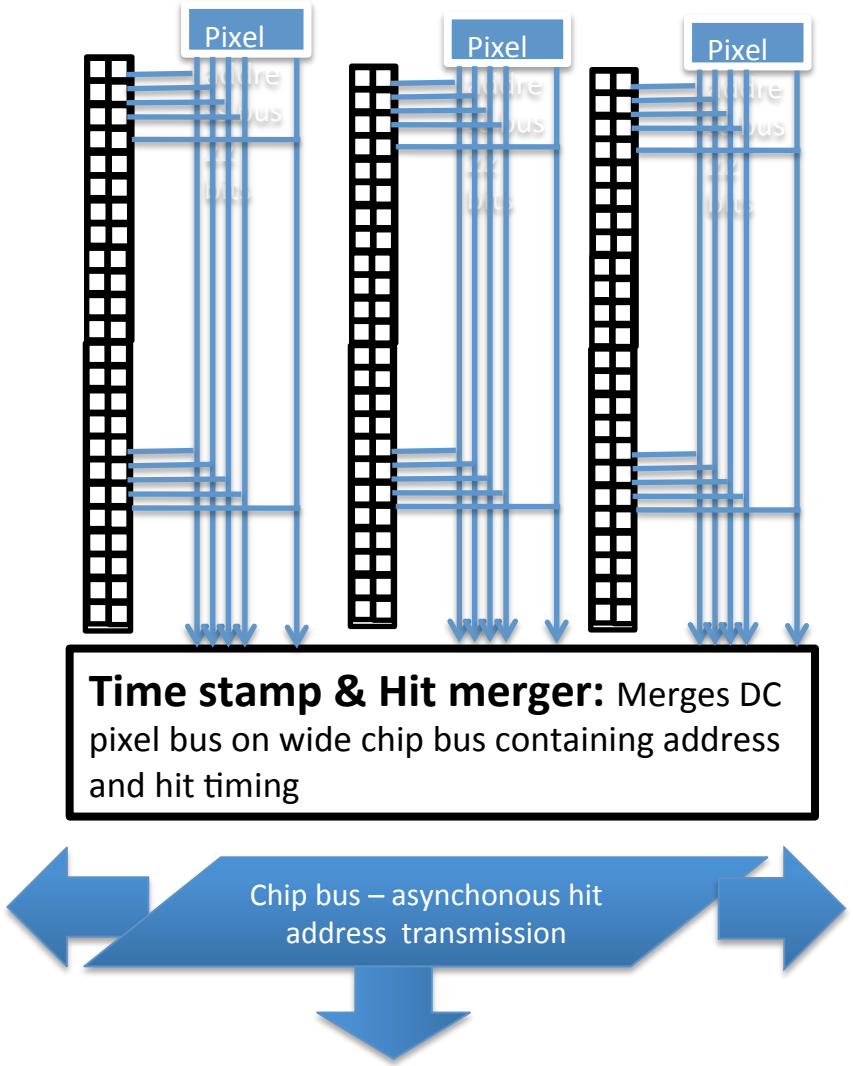



**Hit loss because of too many clusters in DC per bunch crossing at peak rates of outer layers: <0.05% @ 2Mclusters/mm2s .**



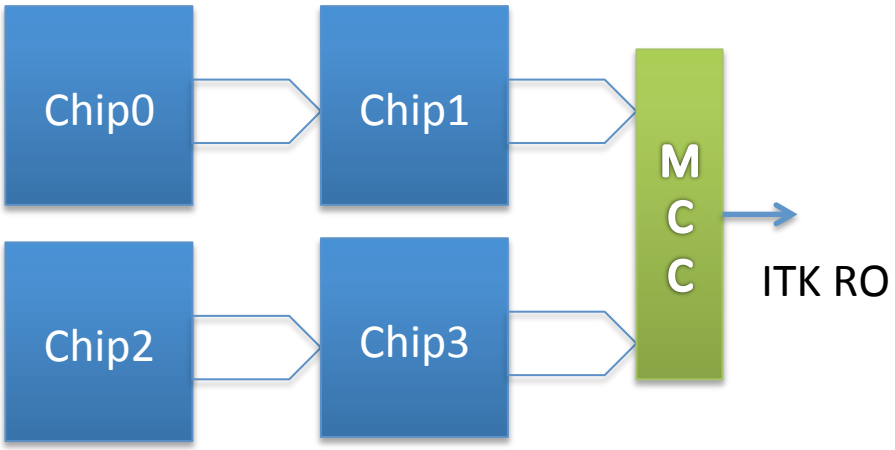
# End of Column - Periphery

- End of Column
  - Merges hit pixel address signals on wide chip data bus
  - Adds time stamping to identify bunch crossing
- Chip data bus
  - Contains hit/time information of all hits in the chip
  - Data output can be switched to output stage either as parallal bus or serializer
  - Contains output driver
  - Additional Config input & SR
  - Contains biasing network & DACs



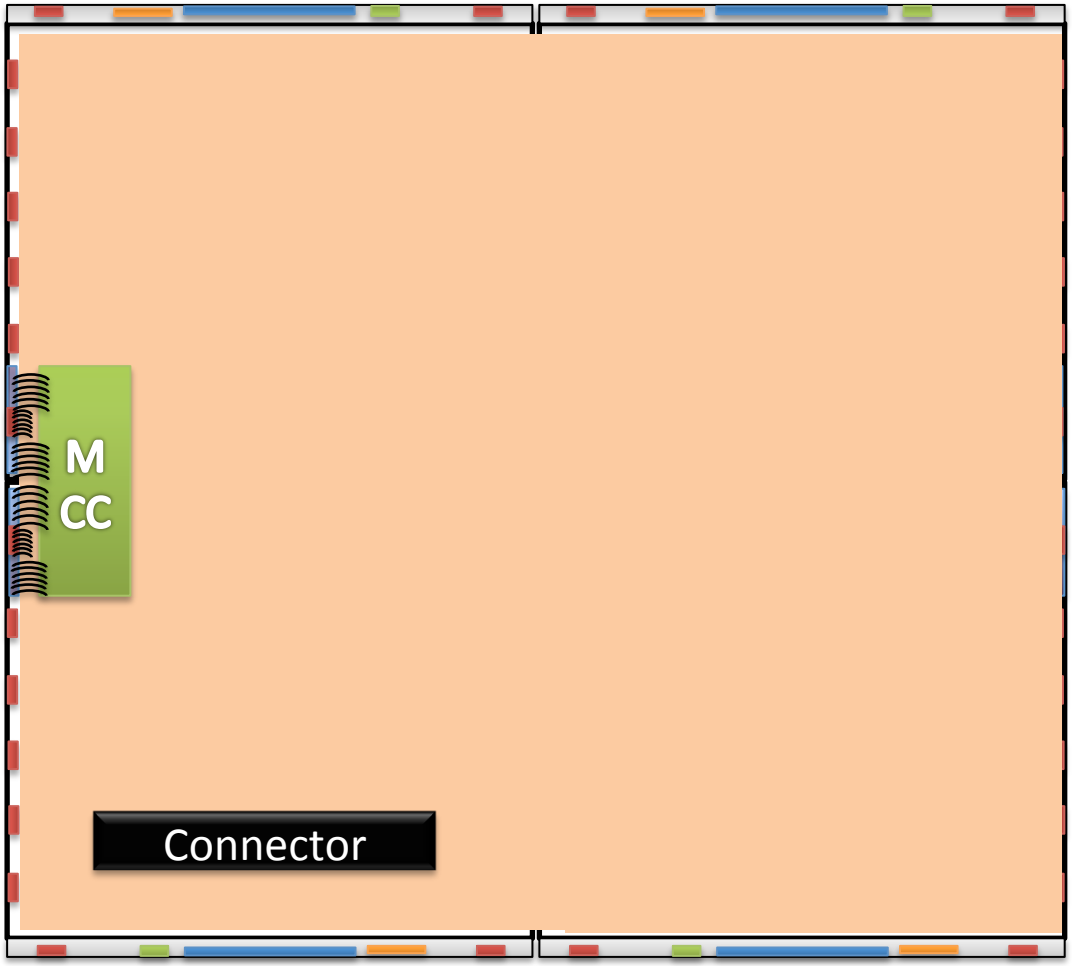
# ITK Hybrid Baseline for Outer layers

- **Hybrid Baseline for Outer layers require 4 chips per module onto single data output**
- Baseline requires a **Multi-Chip Controller (now called Data Concentrator)** like present pixel on outermost layer
- ITK pixel requirement to this MCC
  - Trigger rate 4MHz with latency up to 12.5 or 20 us
  - IO compatible to RD53 (ATLAS-1) to use same readout on inner and outer layers
- Chip-chain to "**Multi-Chip Controller" (MCC)**
  - Chip0 Chip1, Chip2, Chip3 data sent to MCC

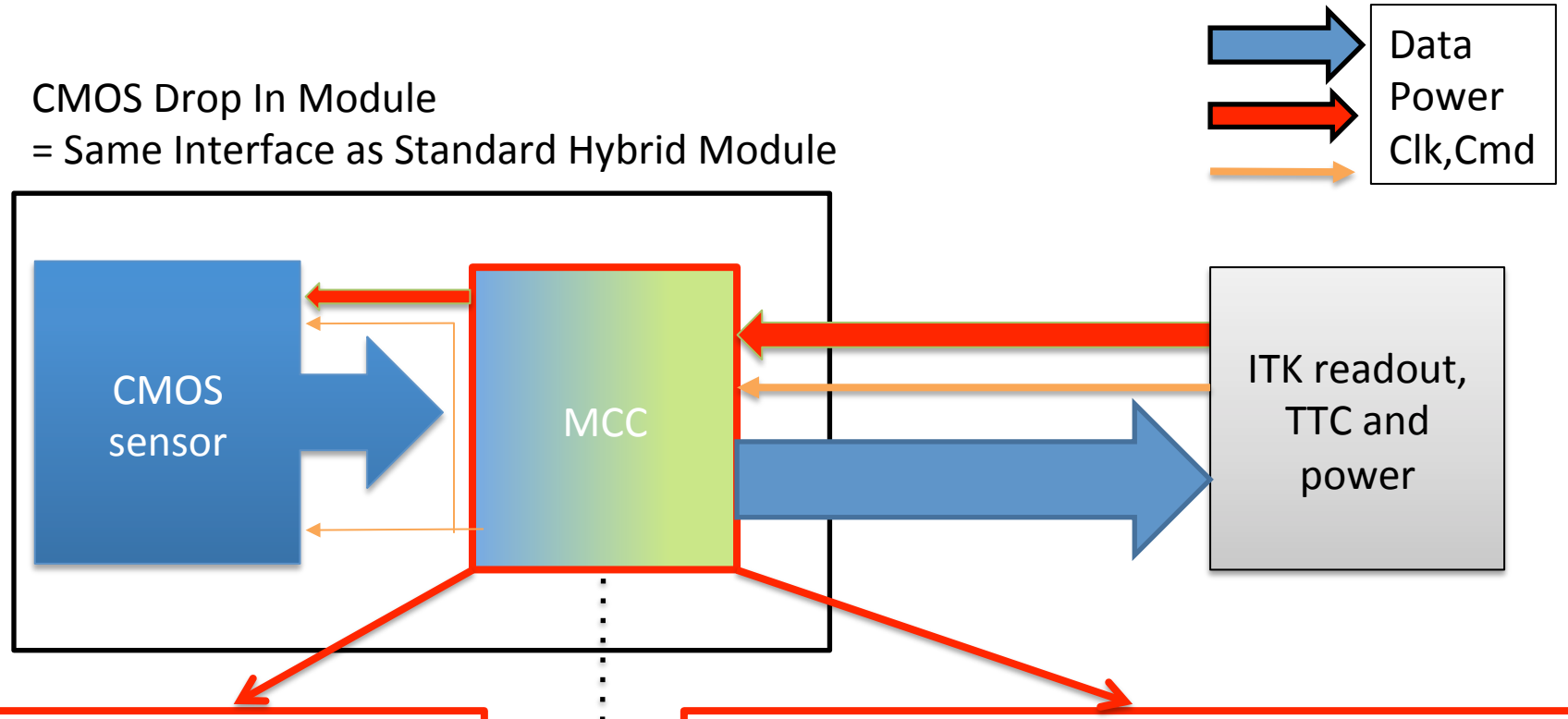


# CMOS Quad Module: Corner A

- Module flex
  - 4 CMOS sensor chips (each ~19x20mm$^2$)
  - Carries MCC
  - Power routing to CMOS chips
  - Module IO connector identical to Hybrid Quad module



# Integration to readout and controls




**CMOS periphery to MCC**

- Raw data handling
- Configuration
- TTC signals
- Parallel power

**ITK Hybrid Module Interface = RD53 periphery**

- RD53 data interface
- RD53 control interface
- Standard Trigger
- Serial power regulator

# Summary

- There is a large momentum in R&D for CMOS active monolithic pixels sensors as an attractive direction for LHC experiments, even pp-experiments
- CMOS sensors are pursued as promising option for the pixel (outer) layers of the HL-LHC Atlas ITK Pixel Detector
- Through combination of **high-resistivity** wafers and/or **HV process** options combined with **dedicated pixel cell** designs, we have achieved radiation hardness of CMOS sensors beyond $10^{15}$ neq/cm$^2$ with several different designs and foundries
- We currently develop a large set of **readout architectures** to cope with hit rates of (outer) pixel layers in Depleted Monolithic Active Pixel Sensors
- This development of **fast – thin – radiation hard CMOS sensors** may provide very interesting sensors for tracking detector at future colliders

# Many thanks

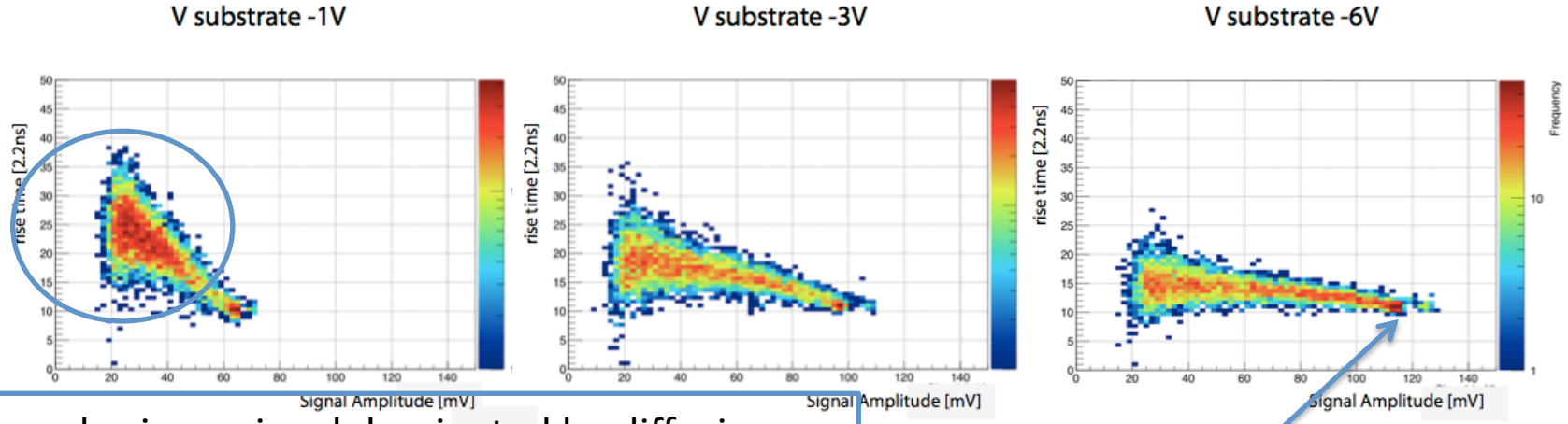
- … to the organizers for the possibility to participate this nice workshop!

- … to my colleagues contributing to this presentation
  - N. Wermes
  - W. Snoeys
  - P. Riedler
  - T. Hemperek
  - H. Krüger
  - E. Vilella
  - I. Peric
  - T. Weston
  - M. Benoit
  - B. Hiti

# Backup

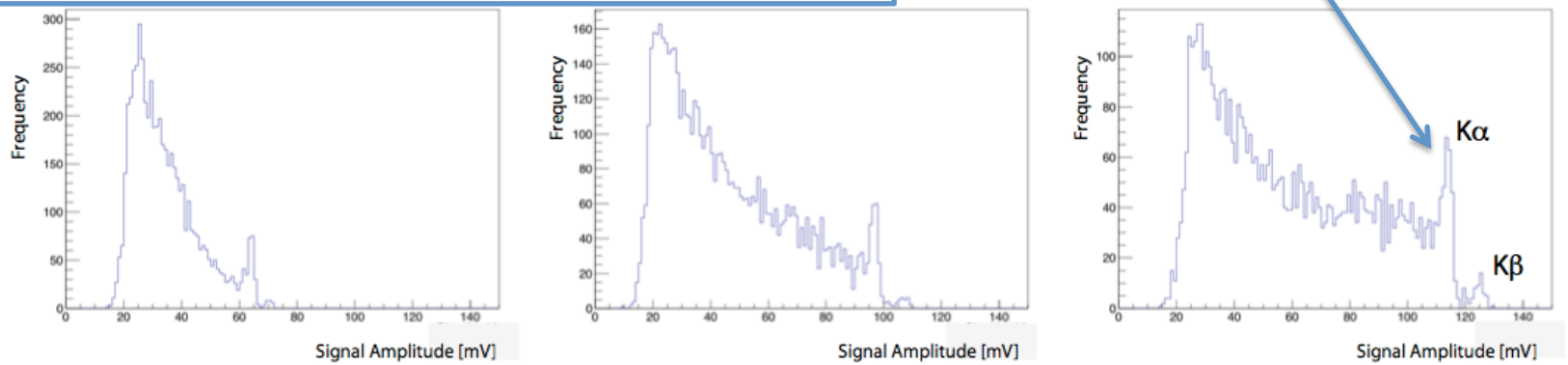
# 55Fe signal - standard process

- Rise time versus amplitude shows significant fraction of "diffusion" signals
  - Signal collection speed increases with substrate voltage for shared hits




Charge sharing – signal dominated by diffusion then by drift

Calibration peak – drift signal

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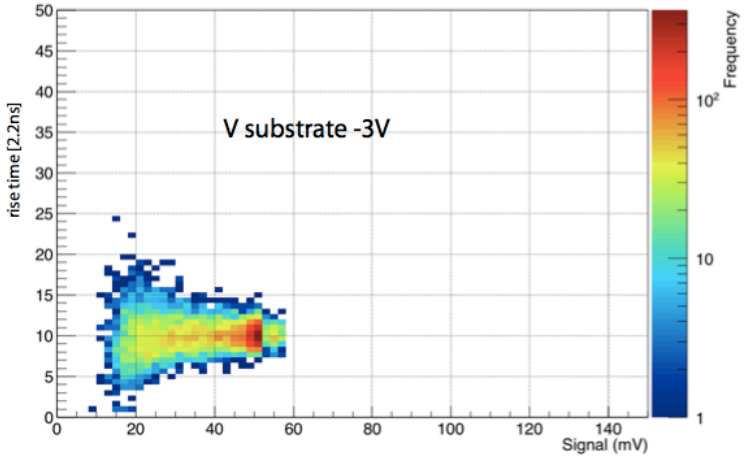
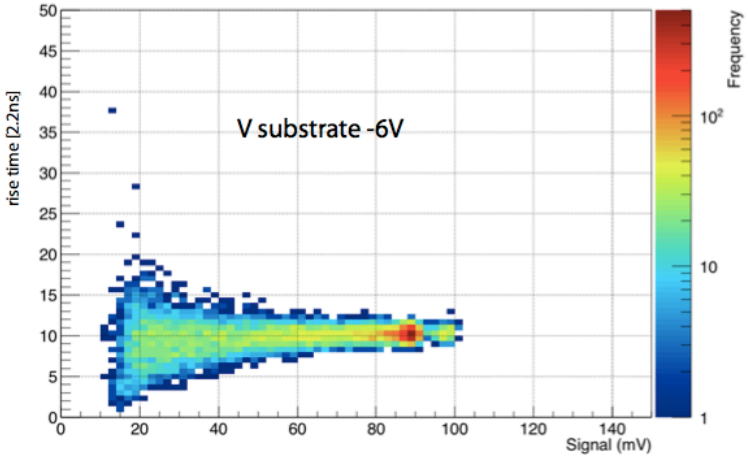
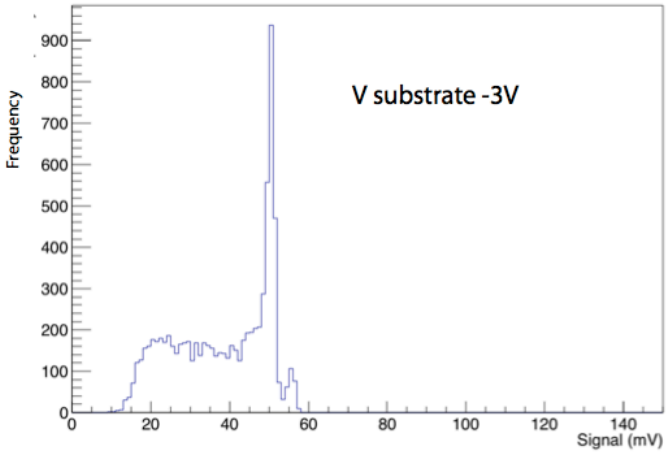
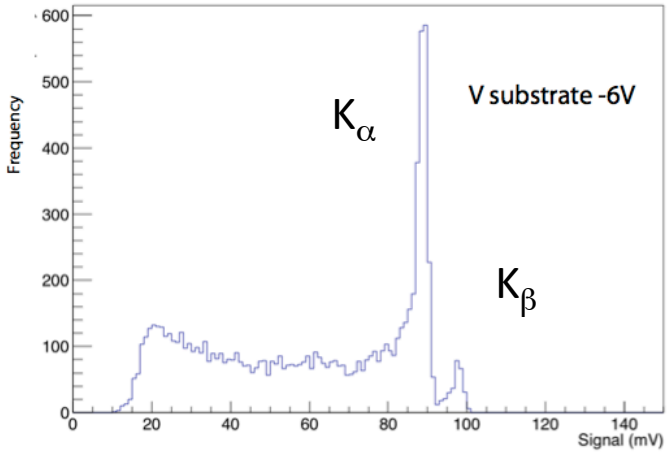
# 55Fe signal – Modified process

- No change in rise time with or without sharing
- Charge collected purely by drift




Note good energy resolution of ~100-150e-

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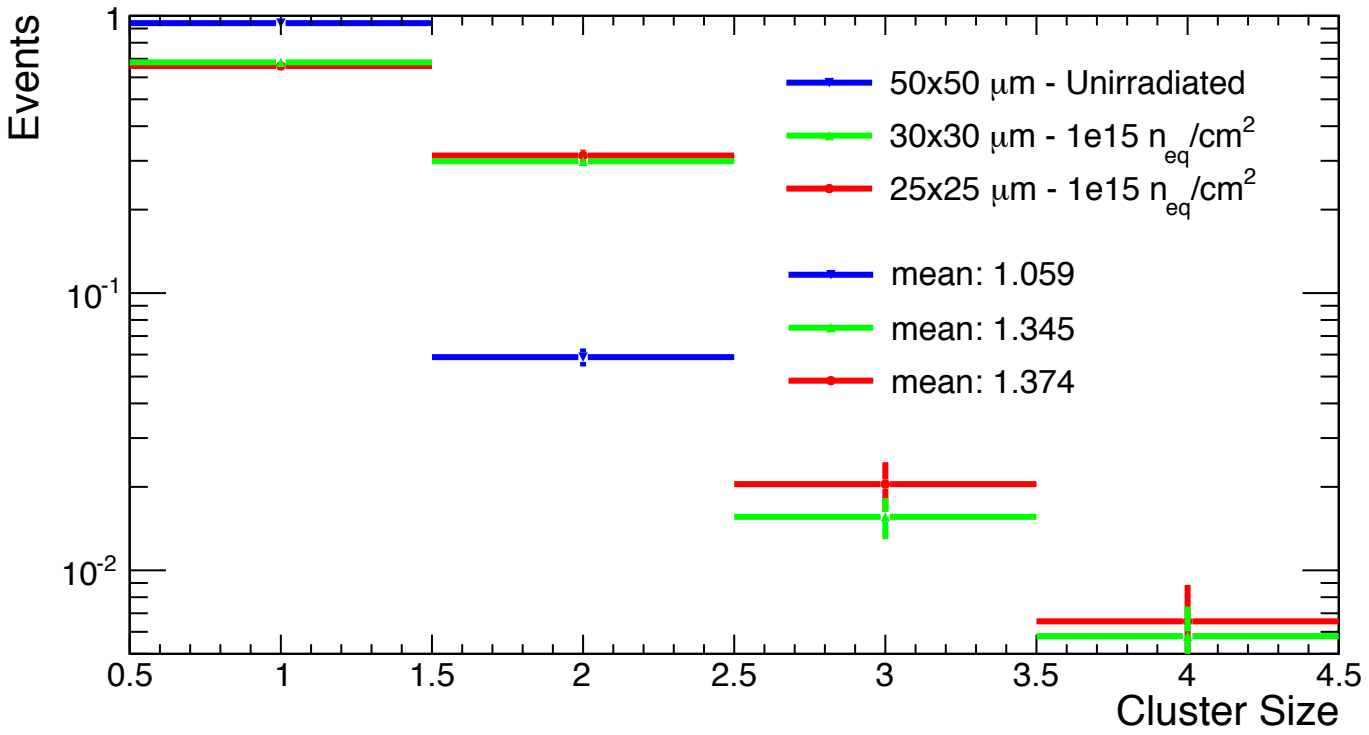
# Cluster size in beam tests

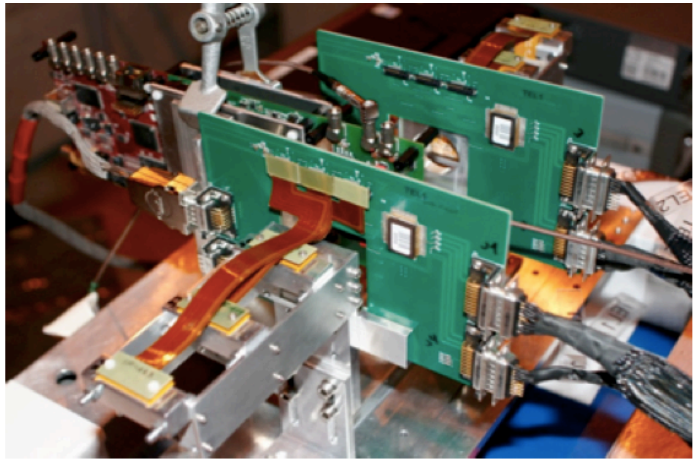
- Unirradiated 50x50um and $10^{15}$ n/cm$^2$ irradiated 25x25 and 30x30um pixel sensors




- Spacing between DNW and DPW also influences charge sharing
- 25x25 and 30x30um have spacing 3um
- 50x50 has spacing 18.5um

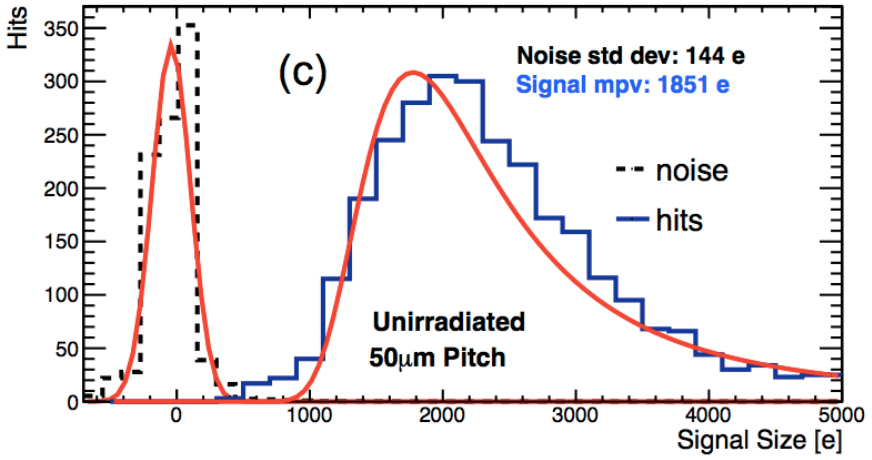
# Testbeam SPS

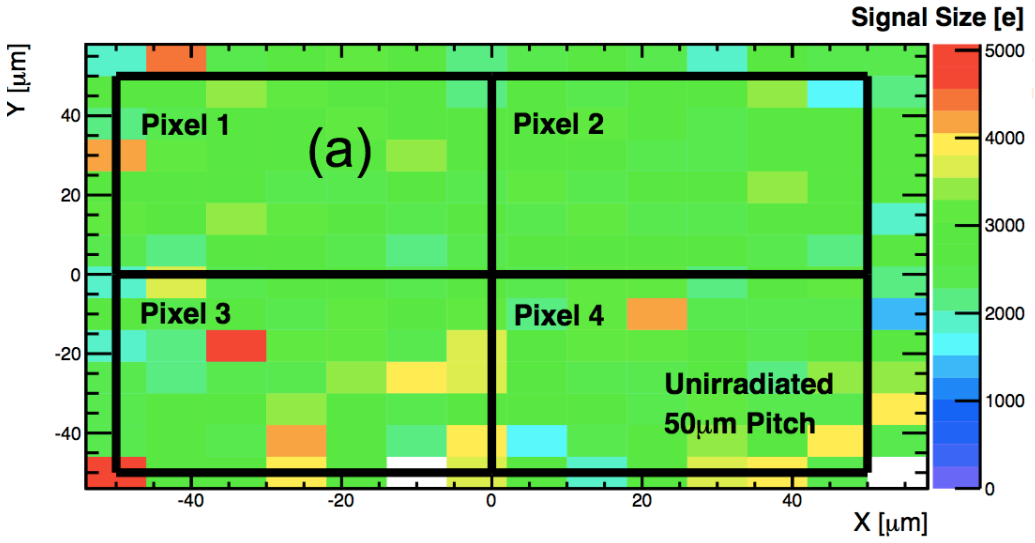
- Beamtests at SPS with 180GeV pions on unirradiated and irradiated after $10^{15}$ n/cm$^2$ sensor



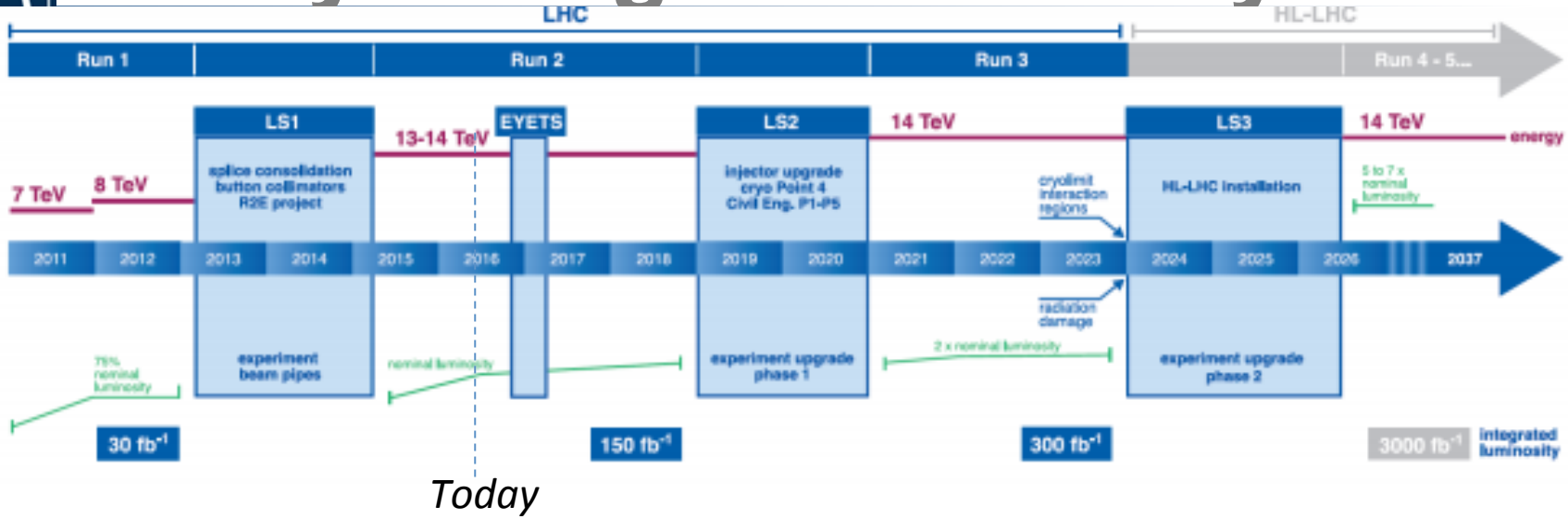
- Unirradiated 50x50um pitch sensor with large spacing (18.5um)

Signal versus position on four 50x50um pixels



# Way to High Luminosity




- Upgrade of Accelerator System to achieve high beam intensity
- Upgrade of Experiments:
  - Tracker will be replaced for better precision and high rates & radiation
  - New Trigger systems are essential to select rare events & new physics
  - New DAQ system & Reconstruction software to cope with enormous data volume

# ATLAS IBL in Run 2

**A true 4-hit pixel system!**
important for b-quark tagging

13 TeV pp collision, 2 interactions