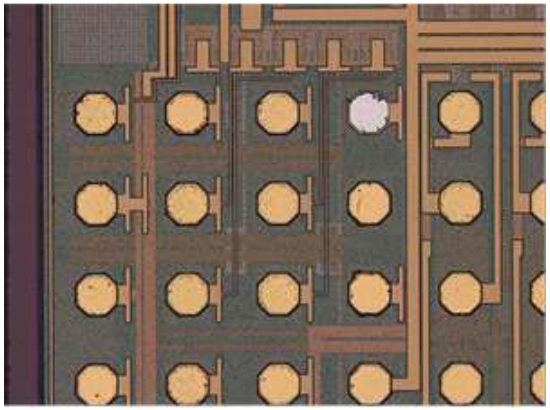
Switcher bumping and module situation

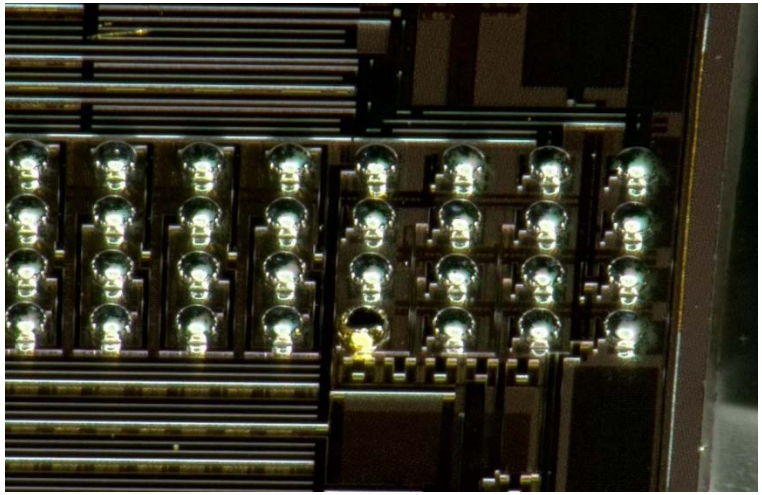
SwitcherBv2.1

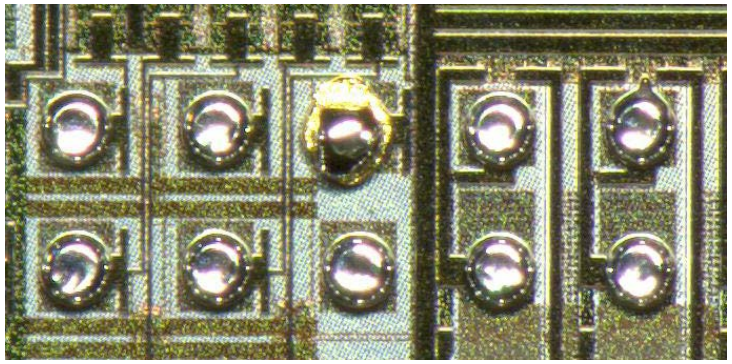
- Bumping (UBM process) causes problems with the new Switcher
- On one pad – the substrate pad – and only on this pad
  - ↳ Very little or no UBM deposition



- Main difference to old Switcher
  - ↳ Different passivation (1µm Nitride/Oxide <-> PI)
  - ↳ Guard ring of the chip exposed, connected to bulk

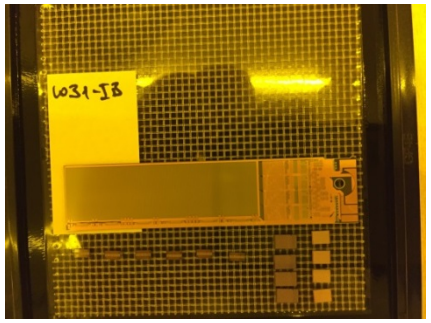
→ Different electrochemical potential causes reduced UBM growth on substrate

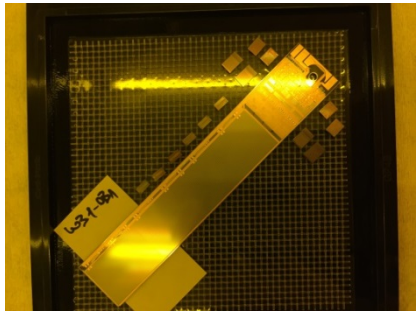
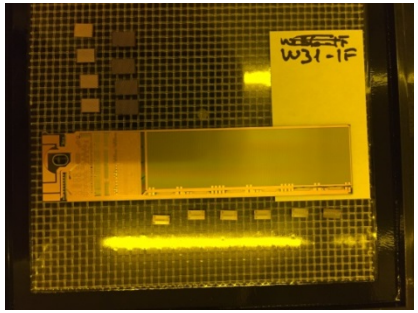


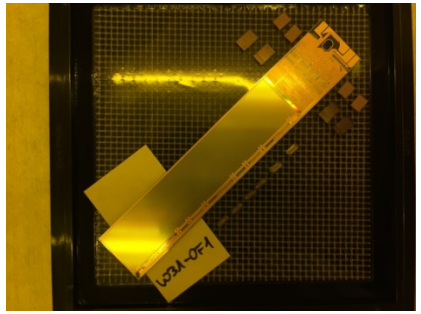


4 modules assembled

- W31-IB, W31-OB, W31-IF
  - DCDB4.2 (final), SWB2.1 (final, repaired bump), DHPT1.1
- W31-OF
  - DCDB4.2 (final), SWB2.0 (last samples of the old version), DHPT1.1

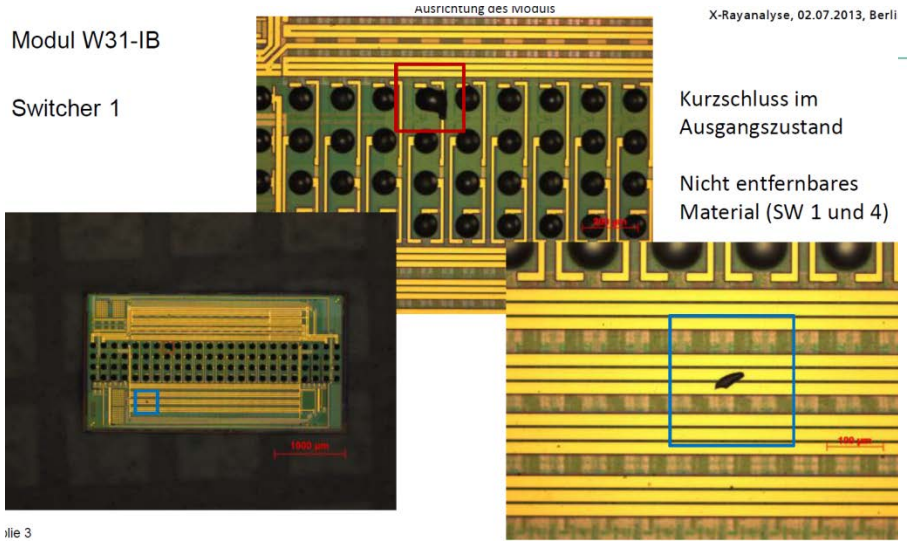


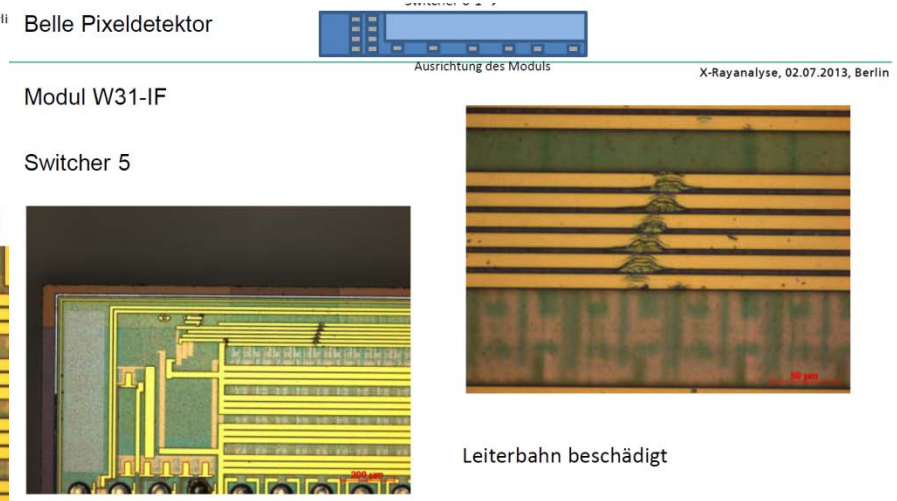



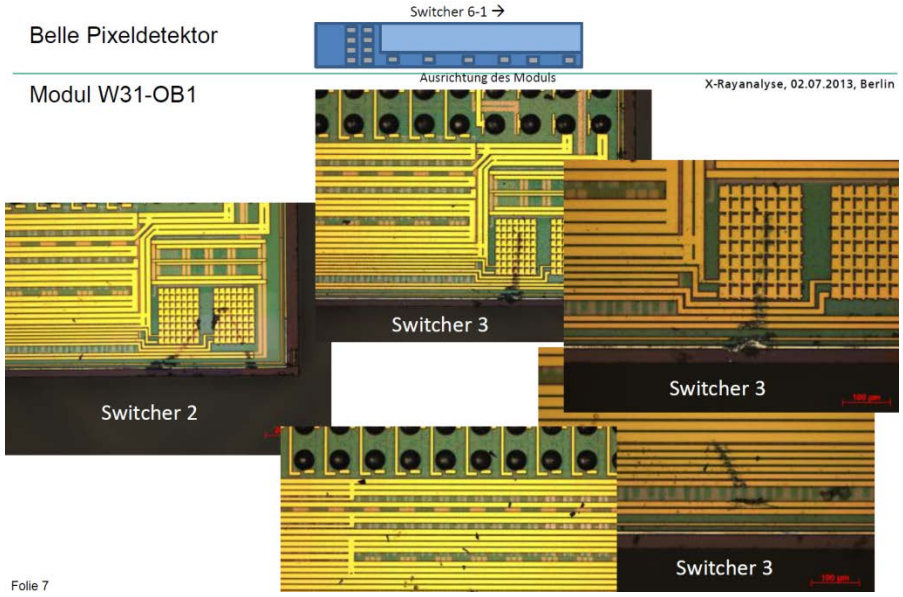


- Flip Chip without any anomalies
  - Switcher generally not prime grade due to problems with bumping (see next slide)
- SMD, Kapton attachment as usual

“fishy” Switchers, though tested okay





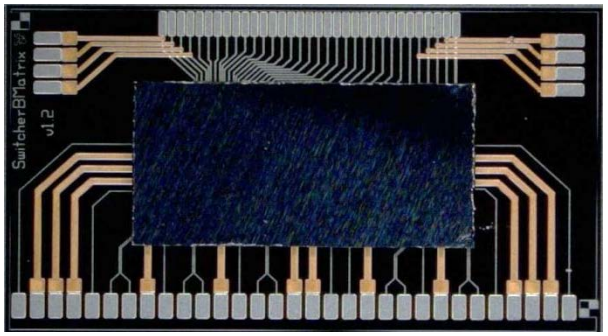


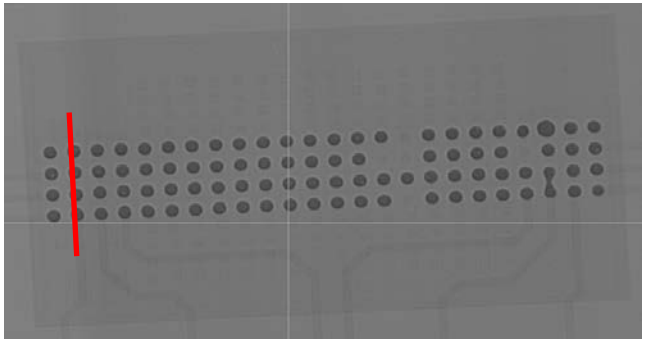
:- SWBs show imperfections, scratches
:- flip chip was done, since the tests on chip level were positive

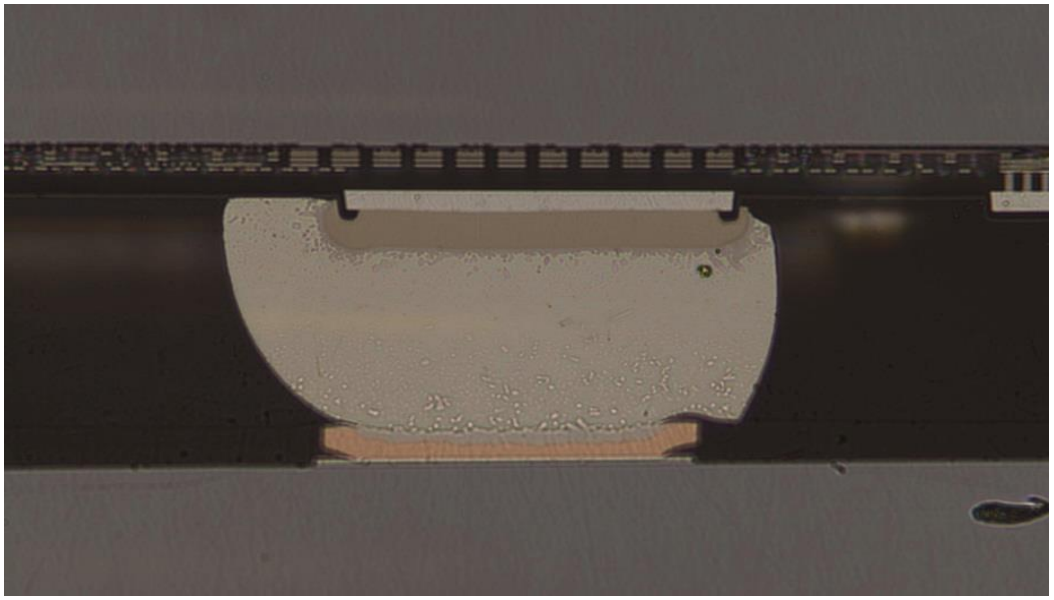
:- detailed xray inspection after FC showed no anomalies (apart from the Au stud bump)

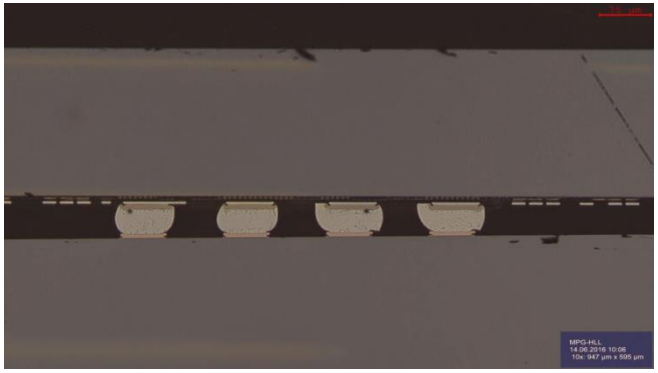
Test Assembly of SWBs to bond adapter

- Adapters assembled for SWB testing on hybrid level
  - Three adapters assembled
  - One assembly done with bad chip (bumping problems)
- Cross-section





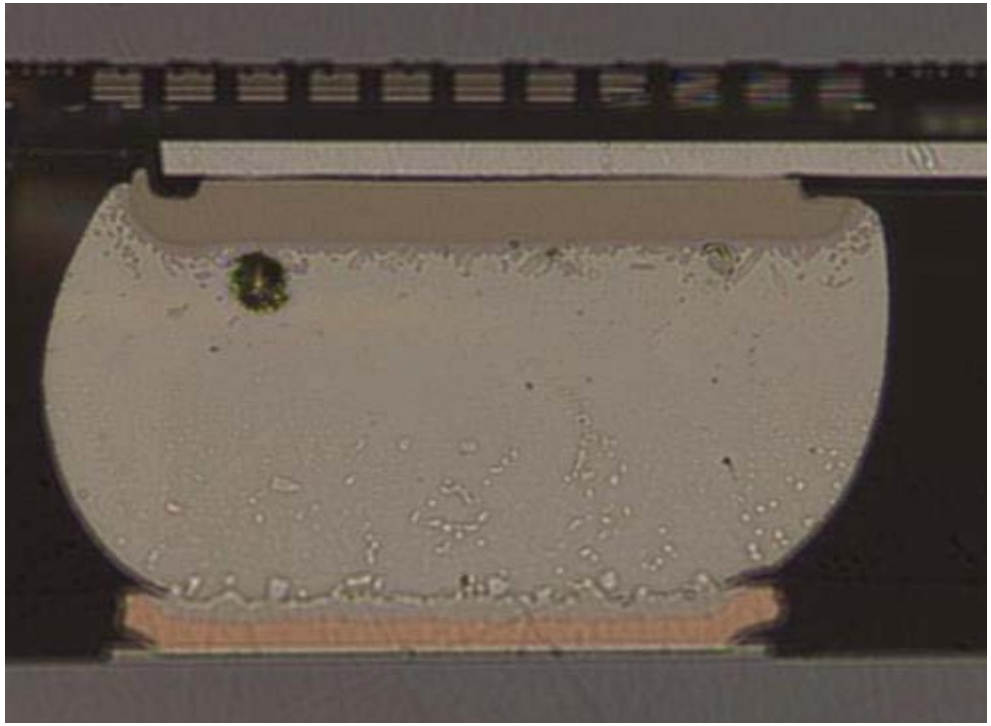


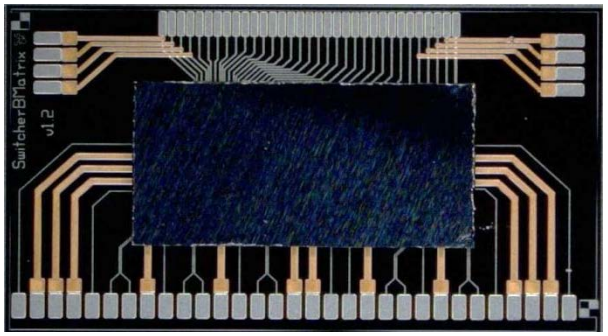


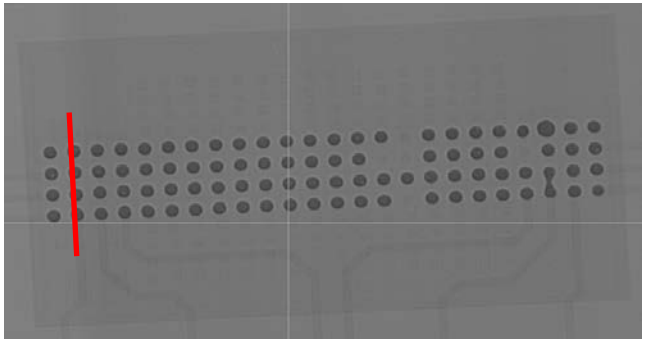
- 80µm balls → too much solder ….
  - Ongoing balling with 60 and 70µm balls

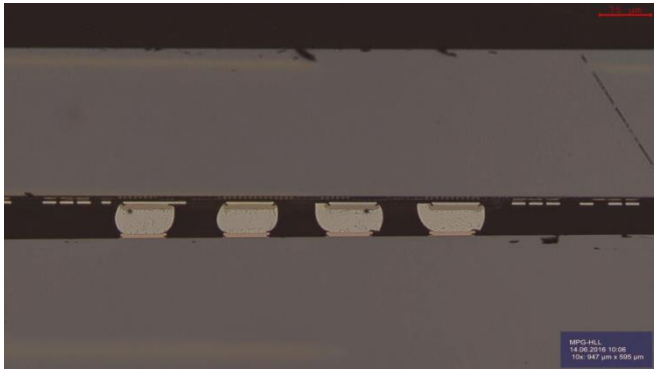
Test Assembly of SWBs to bond adapter

- Adapters assembled for SWB testing on hybrid level
  - Three adapters assembled
  - One assembly done with bad chip (bumping problems)
- Cross-section









- Delamination between SWB Alu and Ni?
  - Not certain if is this real
  - Could be due to contamination before UBM….

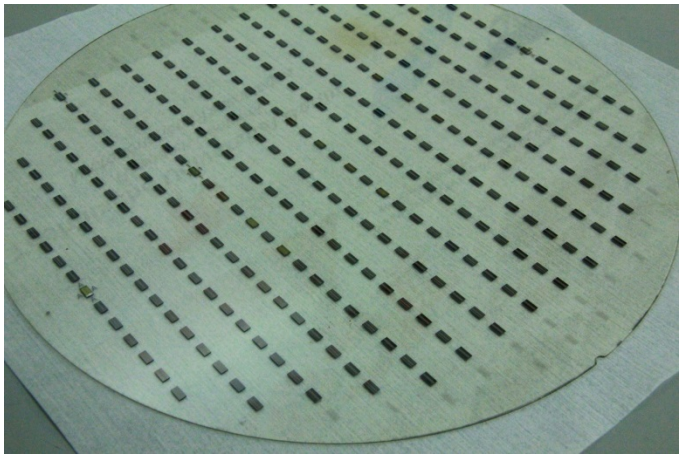
Status of the modules as of today

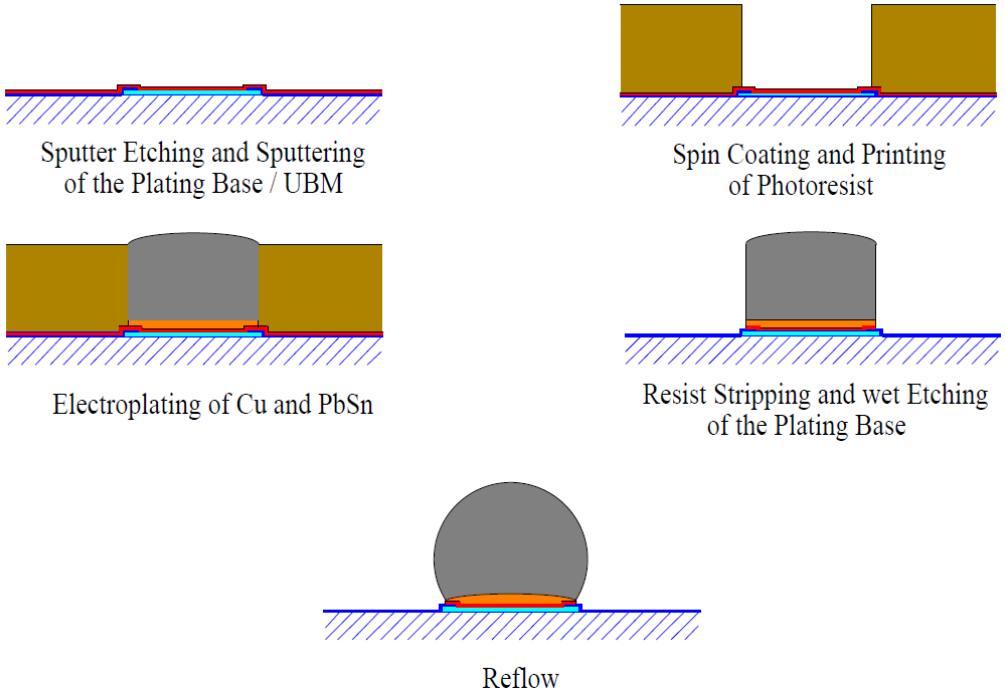
Batch „Persy1“: DCDB4.2, SWB2.1 (Pactech bumps), DHPT1.1

- W31-IB and W31-OB:
  - JTAG configuration fails as soon as the Switchers are in the chain
  - DCD, DHPT okay
- W31-IF:
  - JTAG configuration okay
  - See effect of bad substrate bump on the Switchers (3/6 SWBs not functional)
- W31-OF: **(SWB2.0)**
  - JTAG okay
  - → Philipp’s report

Bumping on “wafer level” at IZM

- Assemble a “wafer” (glass) by pick-and-place of Switchers to support with alignment marks
  - Accuracy good enough for 150µm pitch, subsequent wafer level lithography possible
  - Possibility to apply standard technology bumping by electro-plating

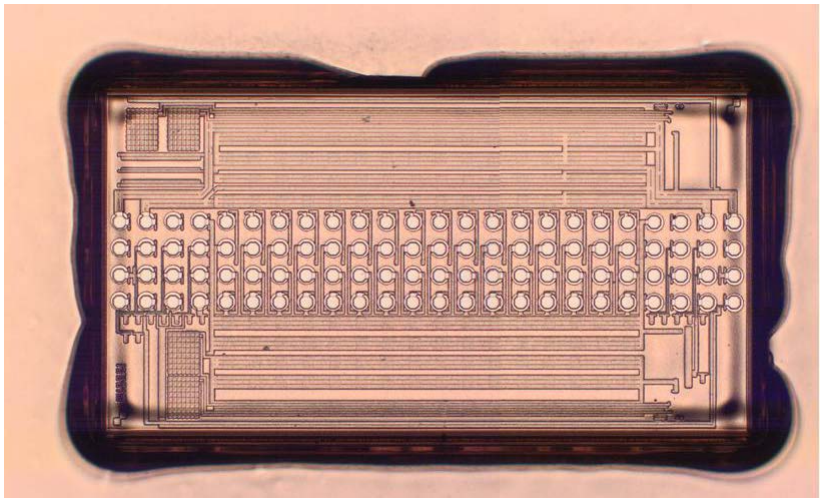


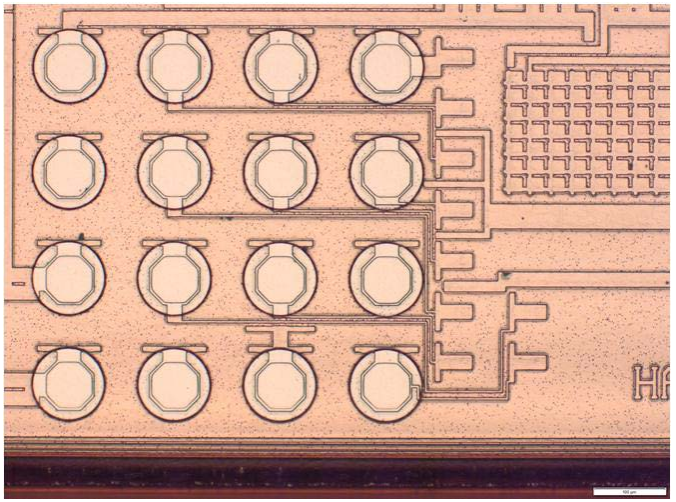


- Tests run at IZM was positive, 24 bumped chips delivered

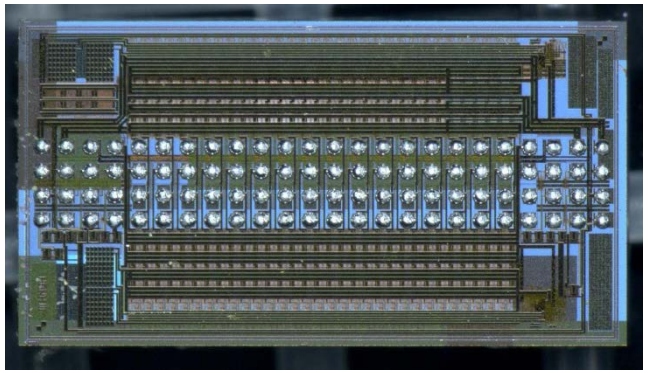
SwitcherBv2.1 bumped at IZM

- After seed layer deposition and lithography



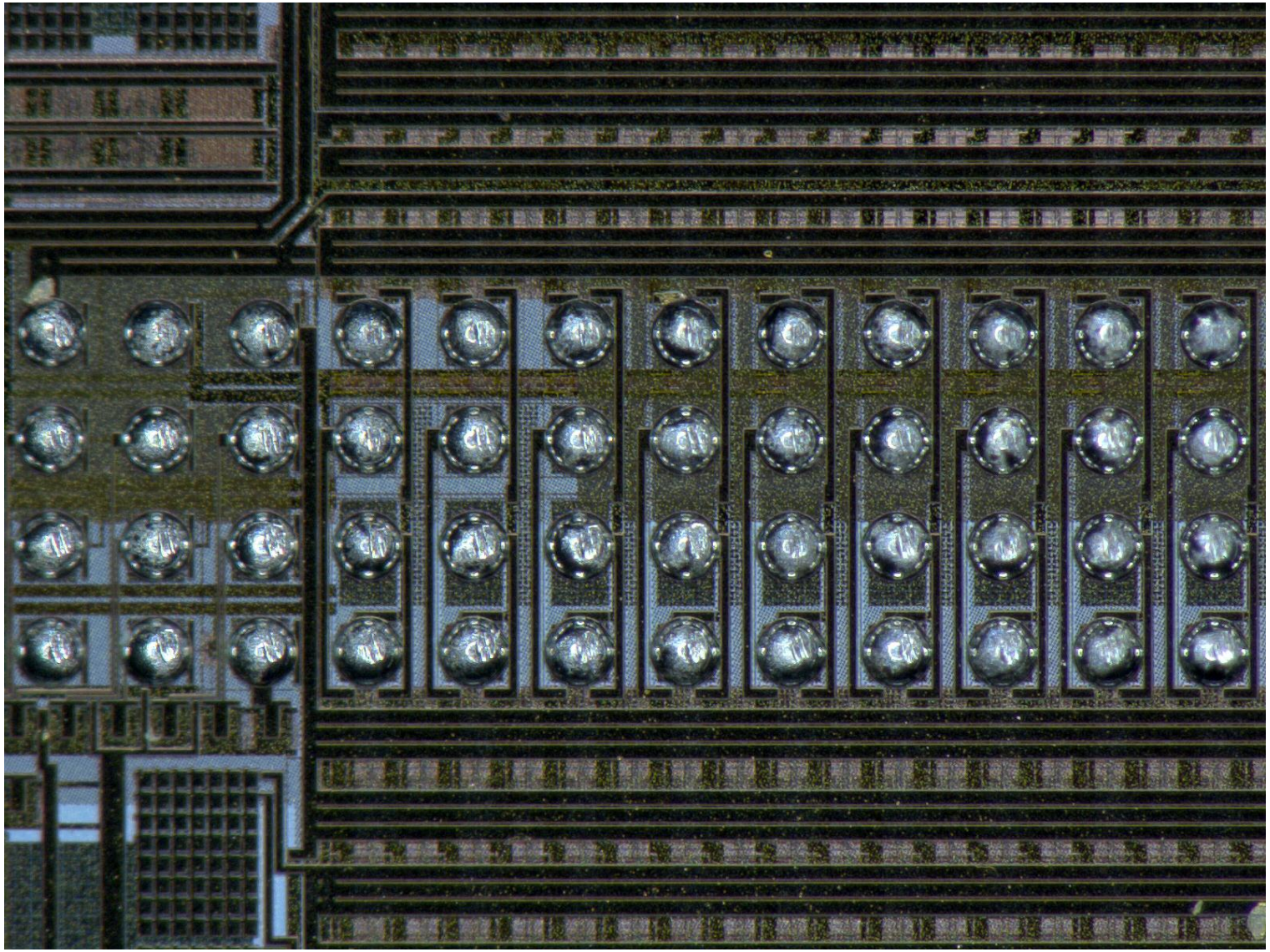


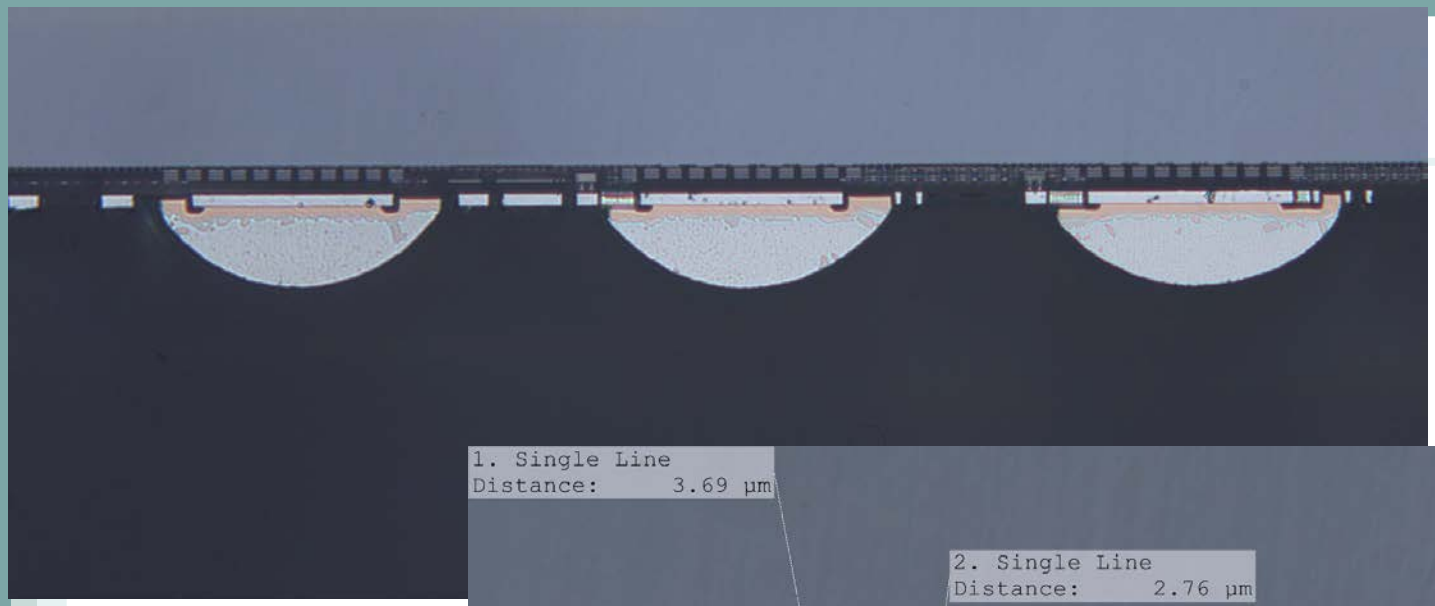
- The bumped chip after reflow

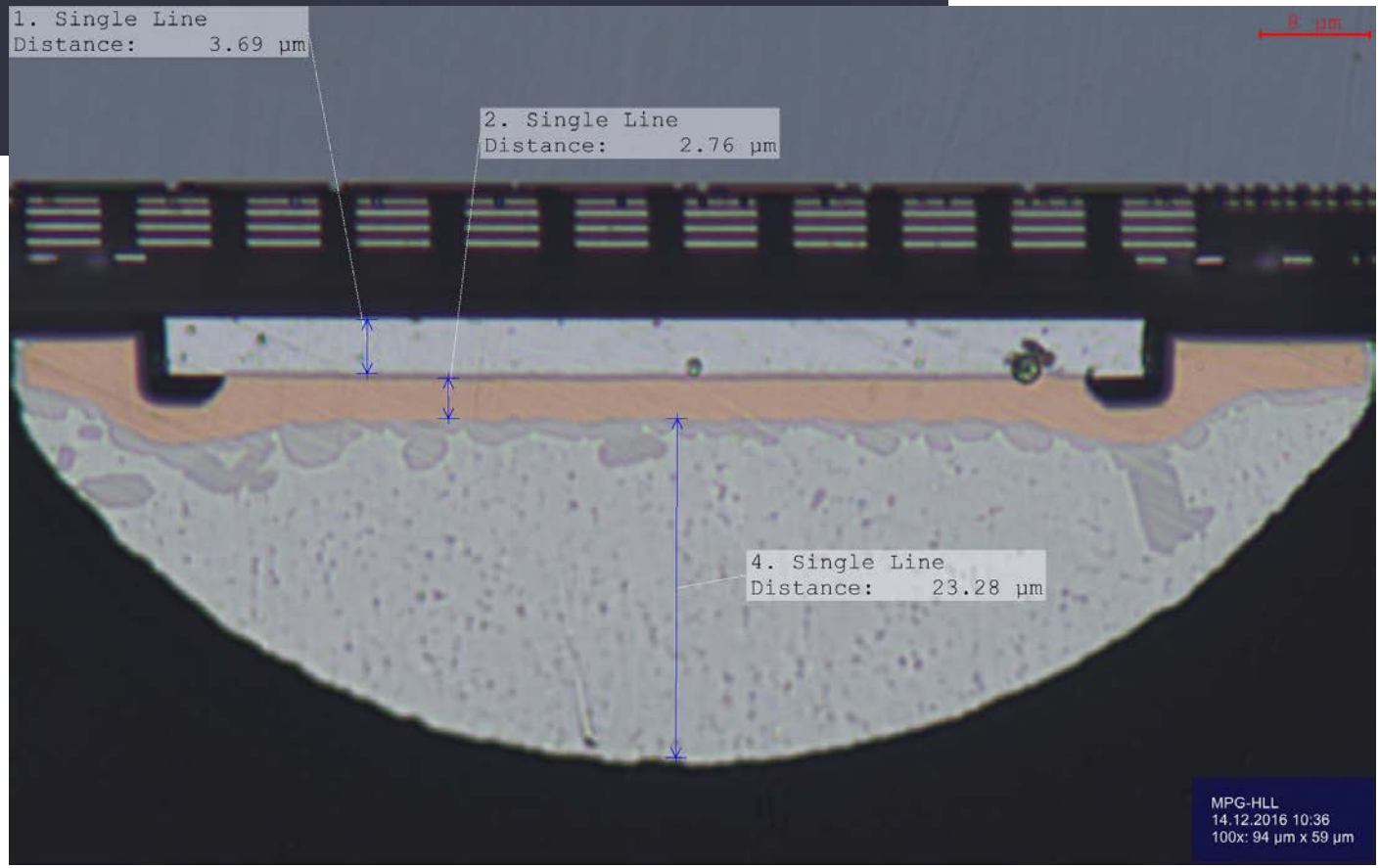


BELLE II- Switcher tests

Switcher Chips	Read JTAG ID	Bias Current	Boost Current	64 HV-channels
18	✓	✓	✓	✓
1	✓	✓	✓	✗
5	✗	✗	✗	✗






1. Single Line
Distance: 3.69 µm
2. Single Line
Distance: 2.76 µm
4. Single Line
Distance: 23.28 µm
MPG-HLL
14.12.2016 10:36
100x: 94 µm x 59 µm

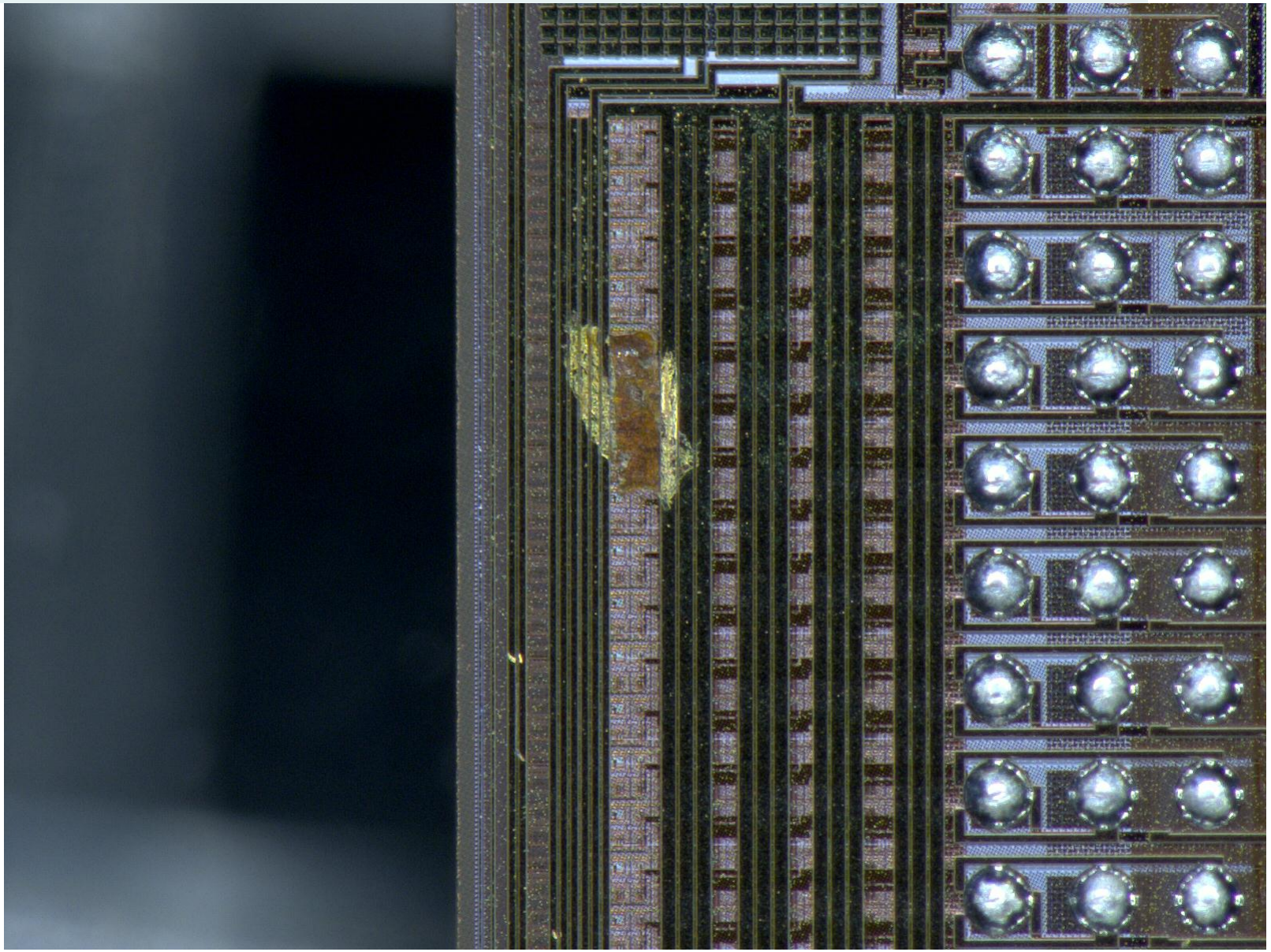
- New modules (batch “persy2”)
  - DCDB4.2, DHPT1.1, SWB2.1 (IZM bumps)
  - W37-IB, W31-OB2
  - Expected to be back from Flip Chip next week
  - Exchange the IB/OB with DCDB4 for the beam test

- W31-IF, W31-OF now under test, other possible candidates for beam test,

- ~450 SWB2.1 at IZM for bumping
  - Complicated, expensive and lengthy process
  - Expexted back for probe station testing mid/end February

Backup

Residues? Photo resist?



Not clear … (from adhesive tape??)