Preparations for PXD9 Module Testing

Philipp Leitl
phleitl@mpp.mpg.de

Max Planck Institute for Physics
Munich

Bi-weekly PXD Meeting
10th of January 2017

Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)

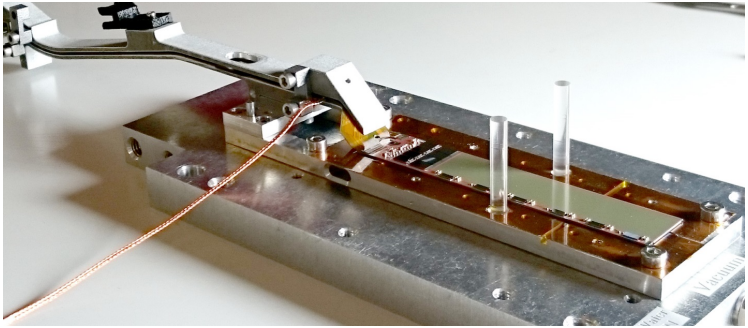
Probe Card

First module tests will be done before kapton attachment with needle cards.

Design A: IF, OB modules $\rightarrow$ ready and tested at HLL
Design B: IB, OF modules $\rightarrow$ design ready, fabrication and assembly ongoing

After Kapton Attachment

The production of the module is now finished, no rework foreseen any longer.



The modules will be tested again to ensure that the kapton attachment was successful (no shorts, no cracks introduced).
But the main task is the **characterization** of the modules: find the optimal settings, make a performance grading, choose the best modules for the PXD.

Configuration Database

Optimal settings (all PVs) are stored in the **configuration database**:

- new “file” for the PXD9 production modules
- own “branch” for each module (e.g. W31_OB1)
- module specific values can easily be reloaded later by just one number: commitid

Production Database

Test results as well as grading to be stored in the **production database**:
grading criteria not yet defined! more experience / statistics needed!

Meeting with Marca, Manfred and Pablo about checklist and grading in the DB.

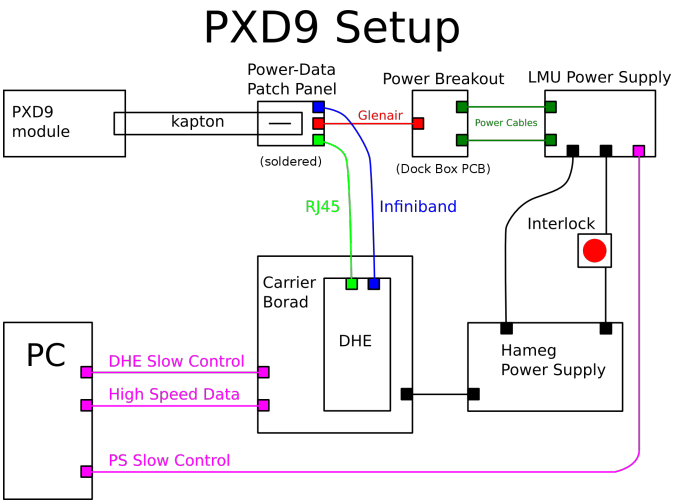
Suggestion:

- percentage grading
  100 % for ideal resulsts
  deductions for failures

- DHPT link stability
- ratio of working pixels
- pedestal spread
- ADC transfer curves (INL, DNL, gain, noise)
- signal to noise
- clear efficiency
- gated mode (turn on/off time, relaxation time)

Test Setup

- setup close to final configuration
- (no DHC, still DHE Carrier Cards)
- final PS, PS cables, Patch Panel, dockbox PCB



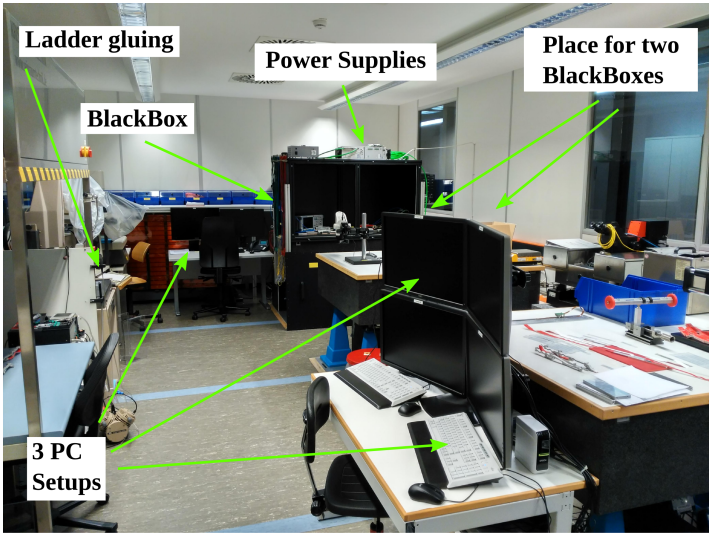
Required Hardware for 4 Setups

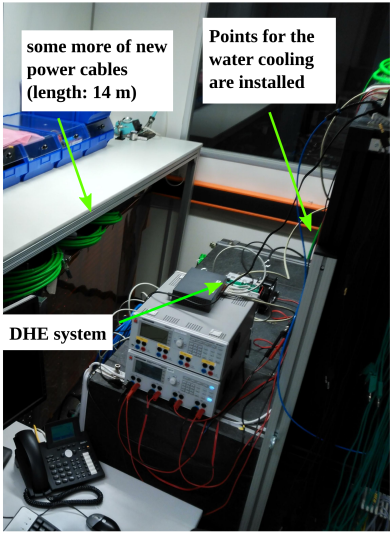
We are currently building 4 setups for parallel working (2 modules, 1 ladder).
Only few missing parts:

- new blackboxes (parts were delivered, will be painted black)
- new Patch Panels (first prototyps were debugged and used with new W31 modules)
- Cd source and Laser (already delivered, not yet installed)
- motorstage

spreadsheet: PXD9 Pilot Run/EMCM Setup

Setups so far





Actual Tests and Characterization

planned tests	time estimate	
powerup and JTAG configuration, voltage sanity check (digital, analog, matrix)	10 min	
JTAG Boundary Scan	10 min	
DHPT link parameters “Aurora Scan”	30 min	
DHPT - DCD communication “Delay Scan”	20 min	
pedestals (bit map working pixels)	30 min	$\sim$ 14 h per module
ADC transfer curves	270 min	
2bit offset DACs	60 min	
sample point	60 min	
DEPFET optimization without source	30 min	
DEPFET optimization with source (Cd-109)	120 min	
clear efficiency	60 min	
gated mode	60 min	