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PSI

Paul Scherrer Institut


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# GotthardII development status

XDAC Meeting, 16.05.2017

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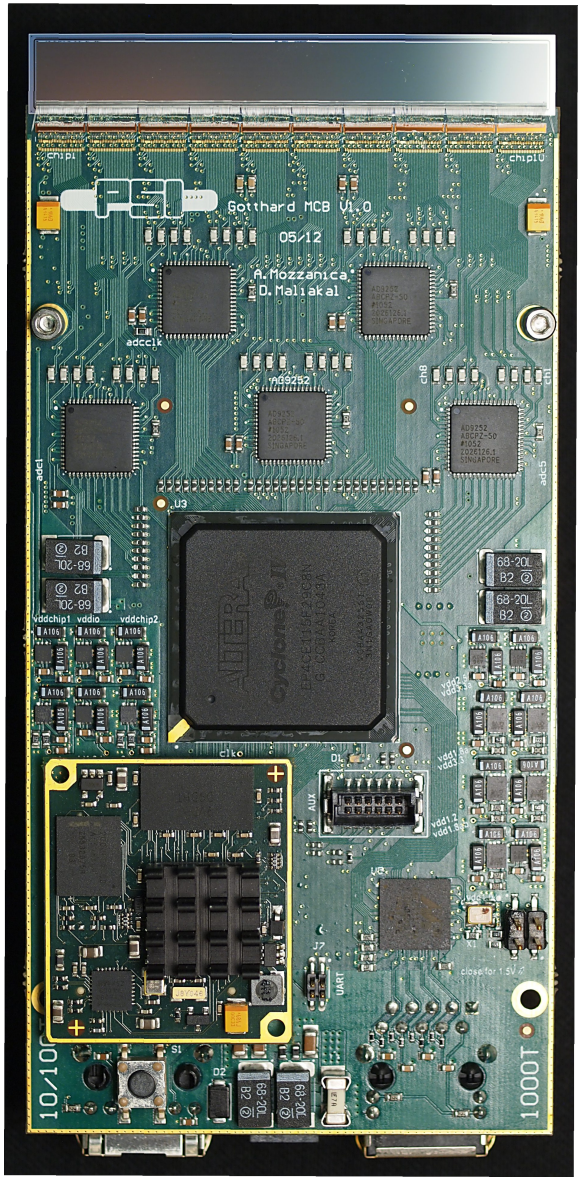
# GotthardI




- 67mm x 130mm
- 50 μm pitch, 1280ch/module (same as MYTHEN)
- 10 chips, 4 analog outputs per chip
- 40 ADC channels @32Mhz,14bits
- Gbit Ethernet data transfer for readout
- 100M Ethernet for slow control/setup
- Fast readout (1MHz) with ~600 bunches per EU-XFEL train measurable (memory for ~350)
- 60kHz continuous frame rate
- Integration in detector class for software control (same as Jungfrau)

- Developed in collaboration with Desy

- Start with GotthardI and replace it with GotthardII

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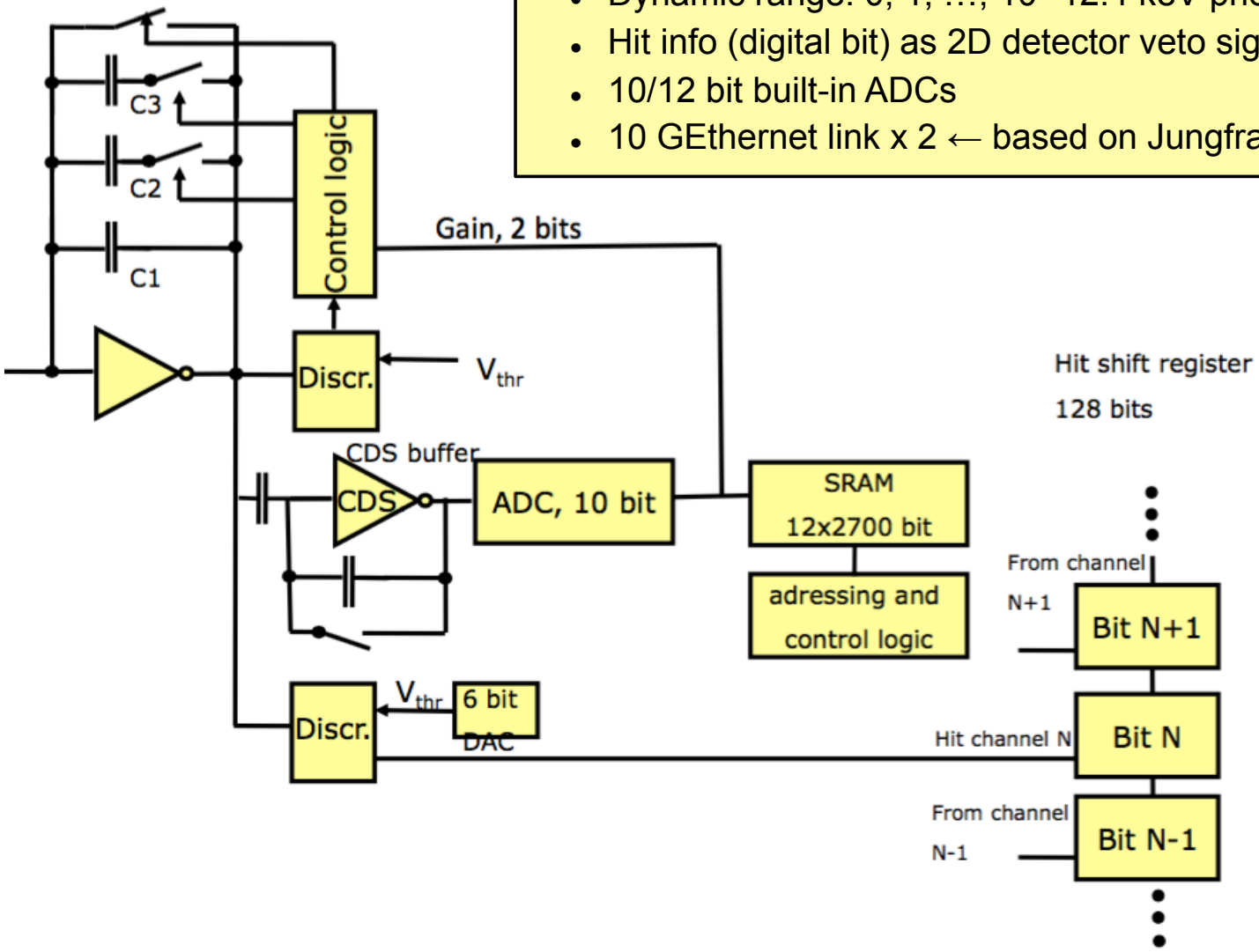
# Outline

- Gotthard-II
- Gotthard-1.7 front-end characterization
- ADC 0.2 characterisation
- New submission (March 17)
- Summary

# Reminder of Gotthard-II: Schematic

- 4.5 MHz frame rate ← bunch structure of the Eu-XFEL
- Dynamic range: 0, 1, …, $10^4$ 12.4 keV photons
- Hit info (digital bit) as 2D detector veto signal
- 10/12 bit built-in ADCs
- 10 GEthernet link x 2 ← based on Jungfrau read-out



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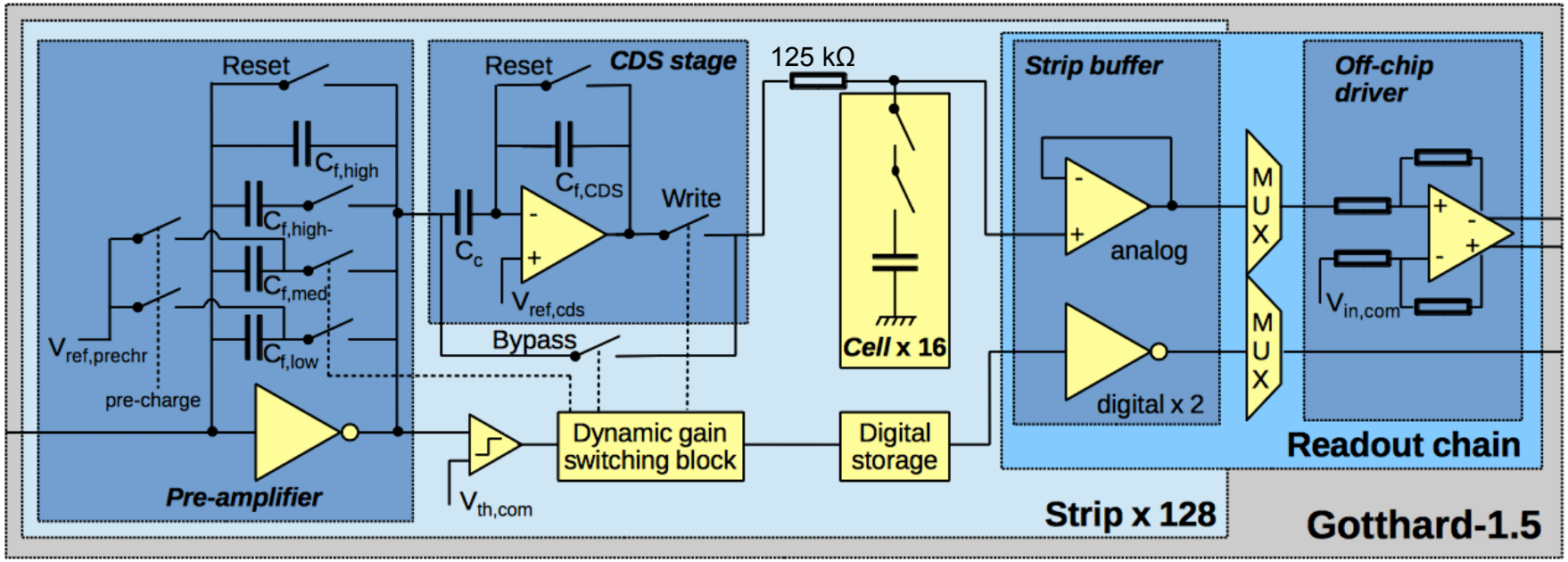
# Gotthard-1.4&1.5 analogue FE

Key features:

- Copied from Jungfrau, preamp scaled for strips

Main problems:

- To slow
- To small DC gain → high capactitive crosstalk



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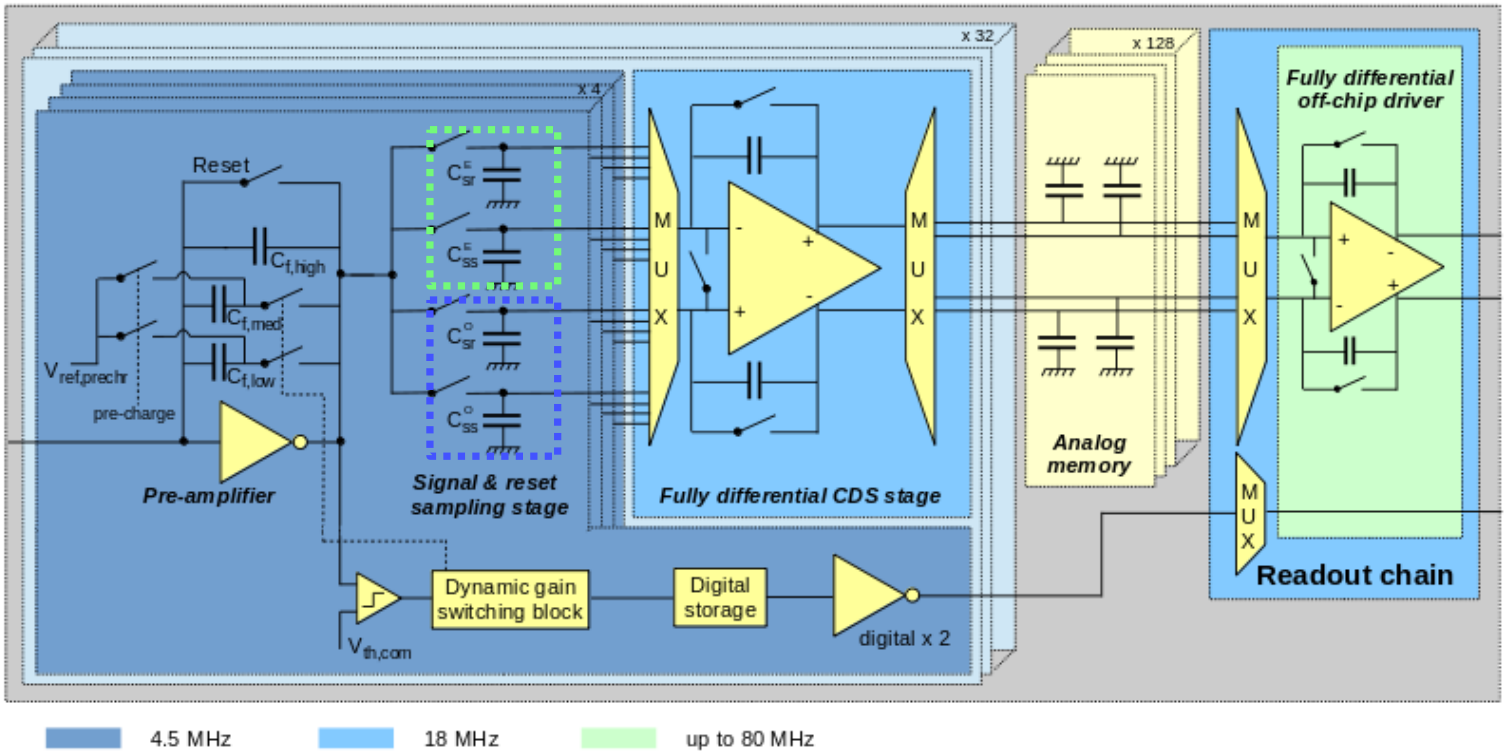
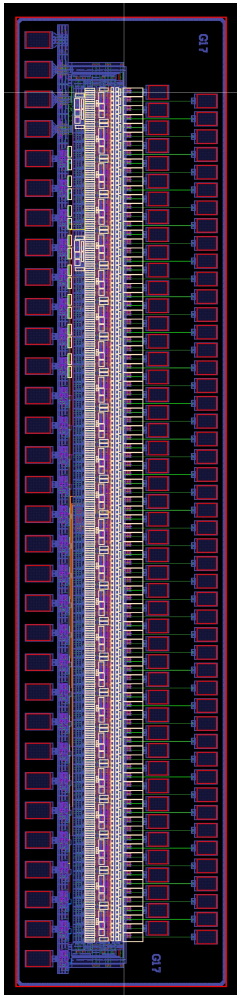
# Gotthard 1.7 analogue FE

- Development of high DC gain, fully differential front-end G-1.7
  - High DC gain pre-amplifier (700-950)
  - Continuous CDS sampling at > 18 MHz
  - Fully differential output to match ADC

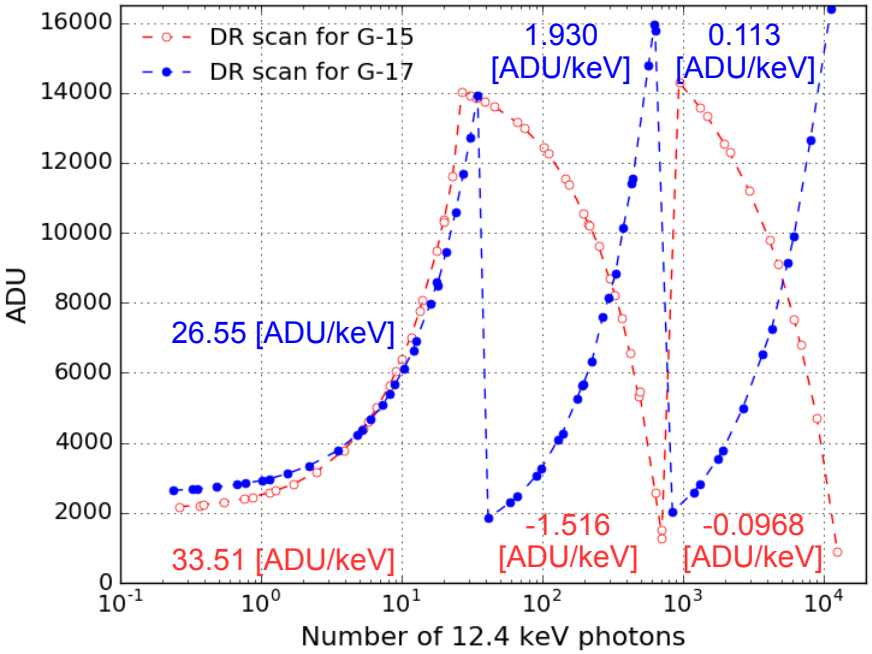


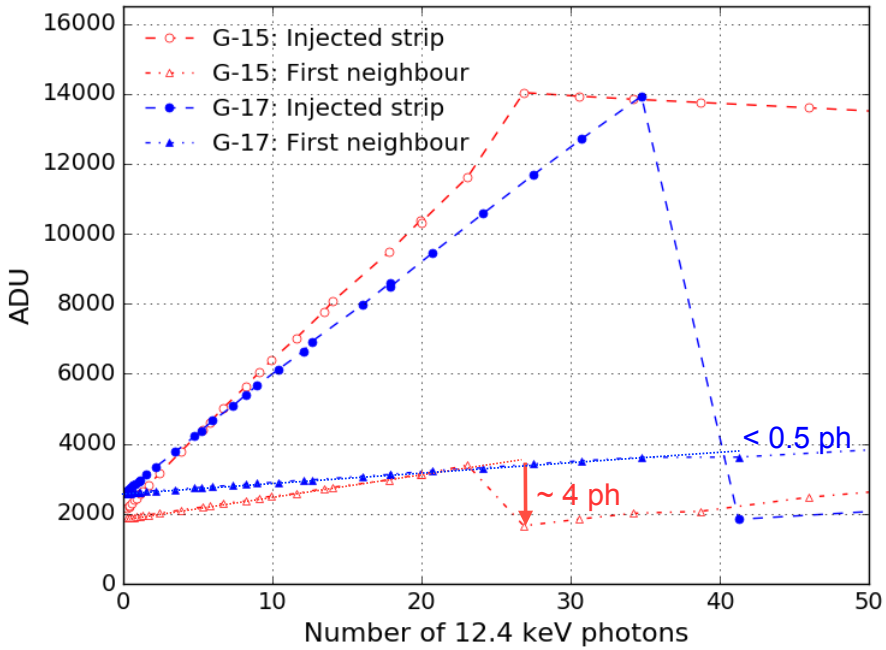
# Dynamic range and crosstalk after g.s.

- Dynamic range: Infrared laser injection into center of a strip
  - G-1.5: 12570 x 12.4 keV photons, G-1.7: 11260 x 12.4 keV photons

Dynamic range scan with laser



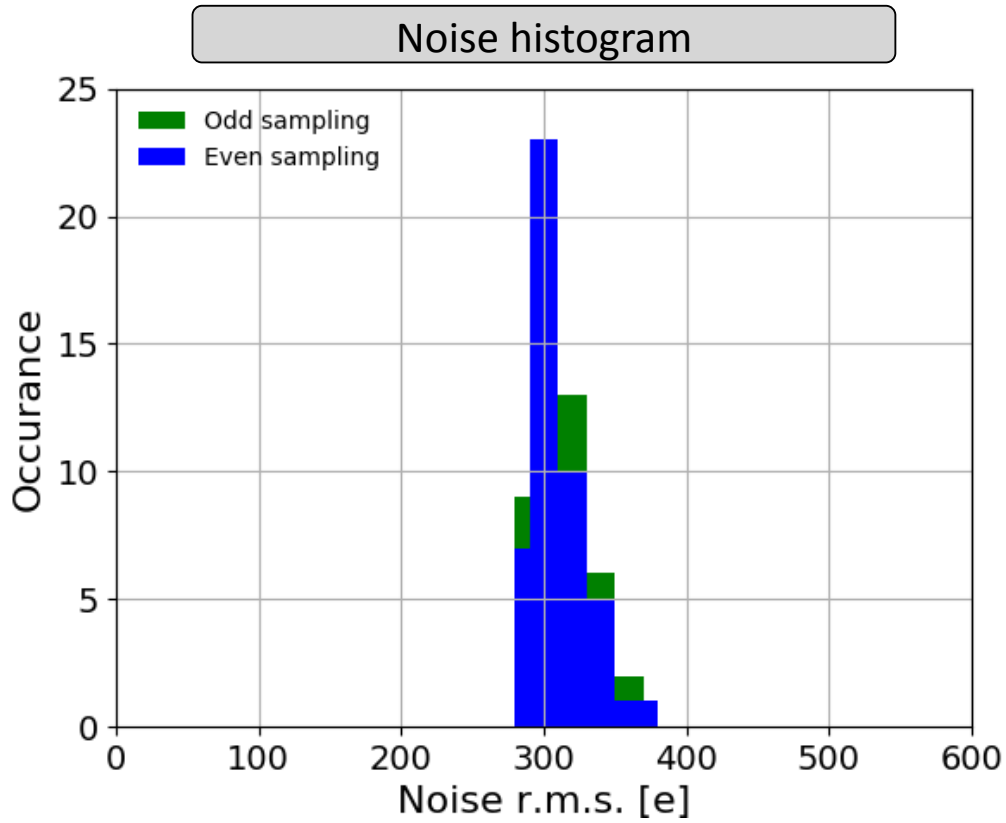

Coupling after gain switching




- "Charge loss" for neighbouring strip after gain switching
  - G-1.5: ~ 4 x 12.4 keV photons, G-1.7: ~ 0.5 x 12.4 keV photons

**Negligible "charge loss" after gain switching!**

# Gotthard-1.7 noise




Noise (HG0):

dark measurement

10 µs integration time

G-1.5: 158 ± 5 $e^-$

G-1.7: 312 ± 25 $e^-$

Causes: 1) Parasitic of pre-amplifier

2) Increased bandwidth

→ Optimize preamplifier design in G-1.8!

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# ADC status

- 3 ADC test structure were submitted in 3 MPWs
- first one had too low sampling speed (reported last XDAC)
- second one
  - Missing codes
- third one submitted in March, will report next xdac

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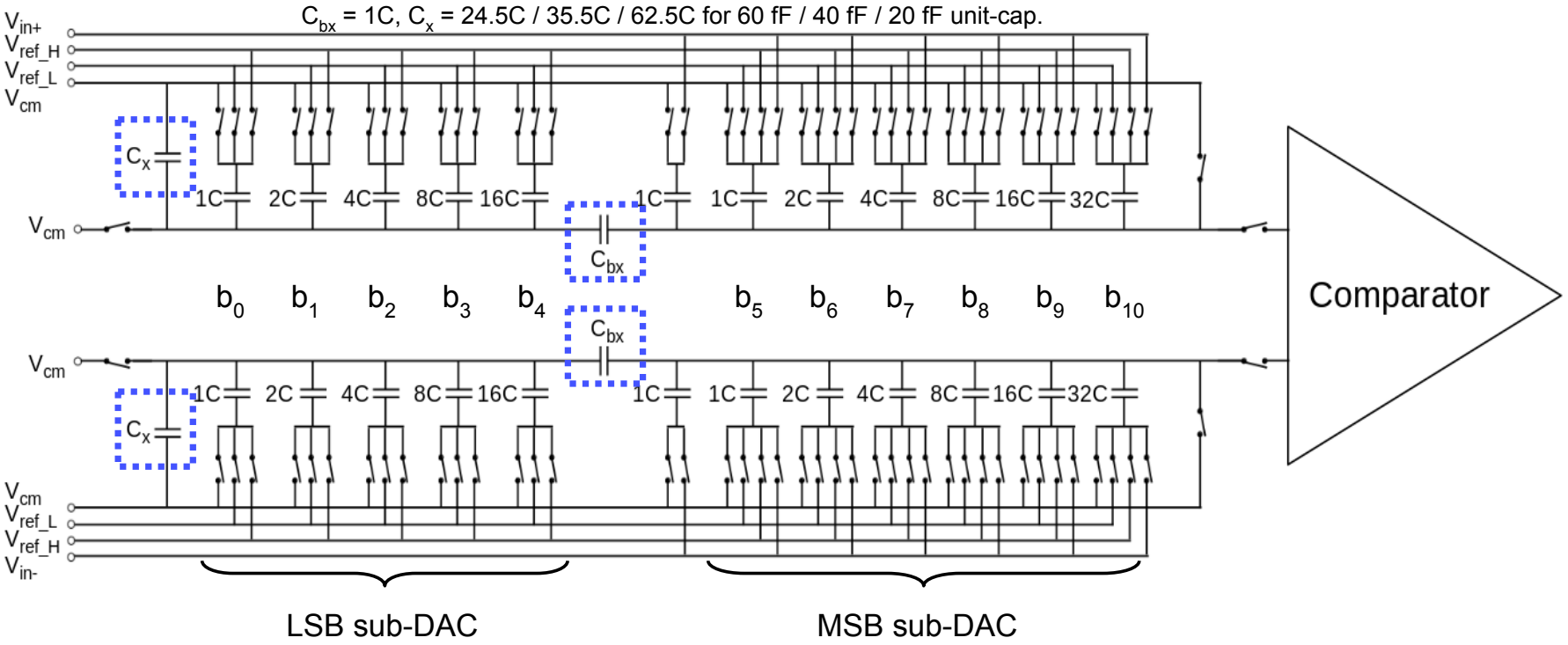
# ADC 0.2

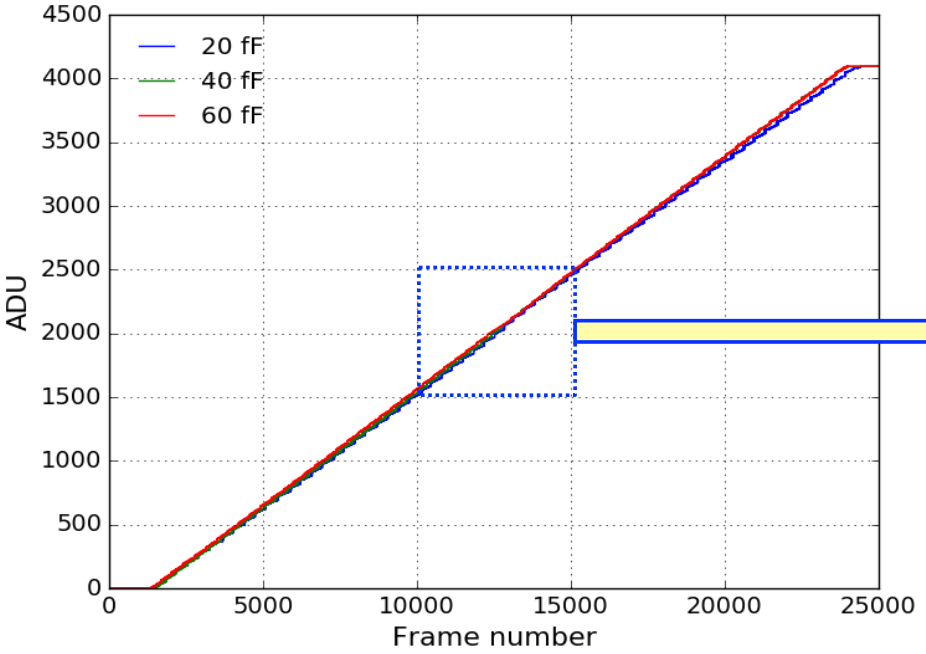
- 12-bit SAR (successive approximation) ADC
  - Split-capacitor DAC array → reduced total capacitance → charging time
  - Two sets of DAC arrays used
  - 3 variations of unit capacitance: C = 20, 40, 60 fF



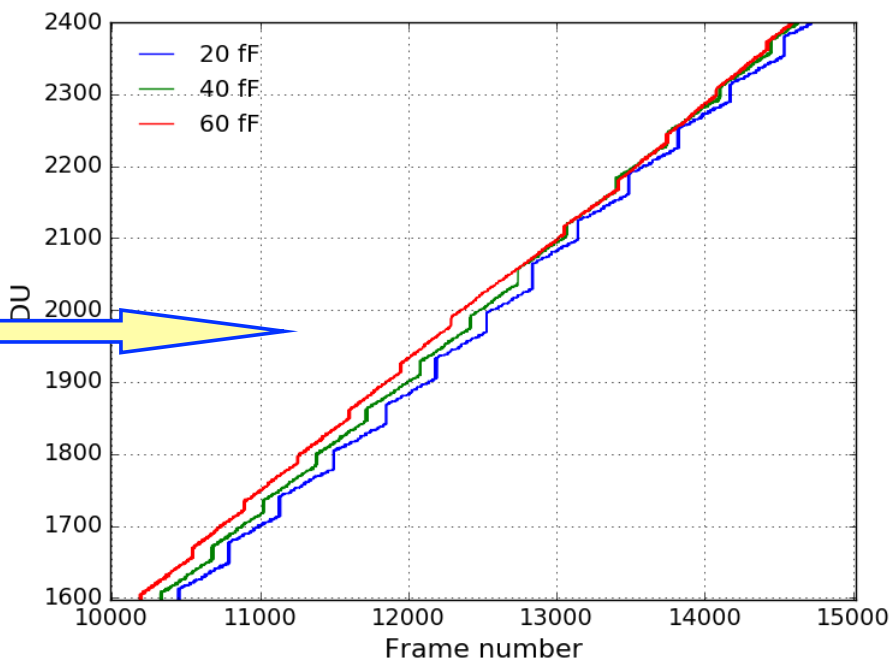
# ADC 0.2 results

- Ramping curve: Linear voltage input covering entire range
  - Segmentation size: 64 ADU → transition from MSB-DAC to LSB-DAC
    - 20 fF: 28 (28/64 = 43.75% missing codes)
    - 40 fF: 16 (16/64 = 25% missing codes)
    - 60 fF: 12 (12/64 = 18.75% missing codes)

Ramping curve

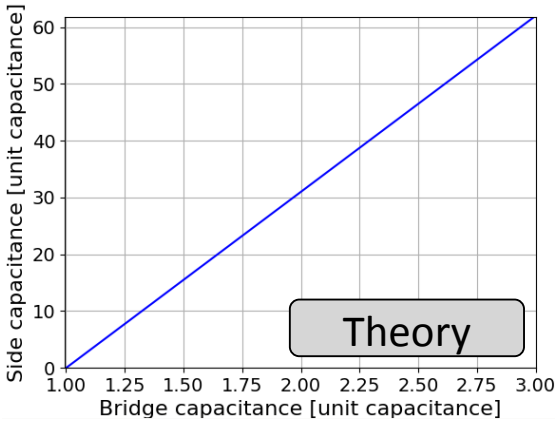



Zoom of ramping curve

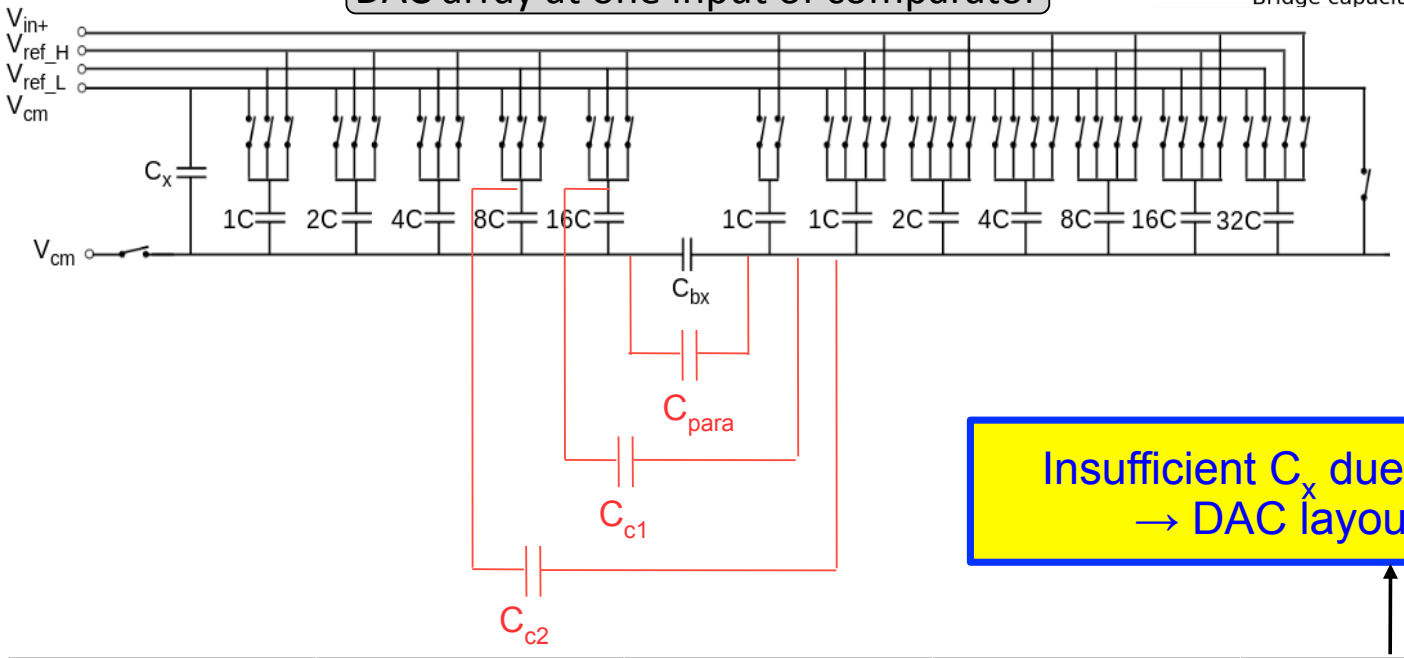


# ADC 0.2 results II

- Causes: 1) Parasitics of bridge capacitance ($C_{bx}$ > 1C)
  2) Coupling LSB-DAC to comparator input




DAC array at one input of comparator




Insufficient $C_x$ due to $C_{c1}$ & $C_{c2}$:
→ DAC layout routine

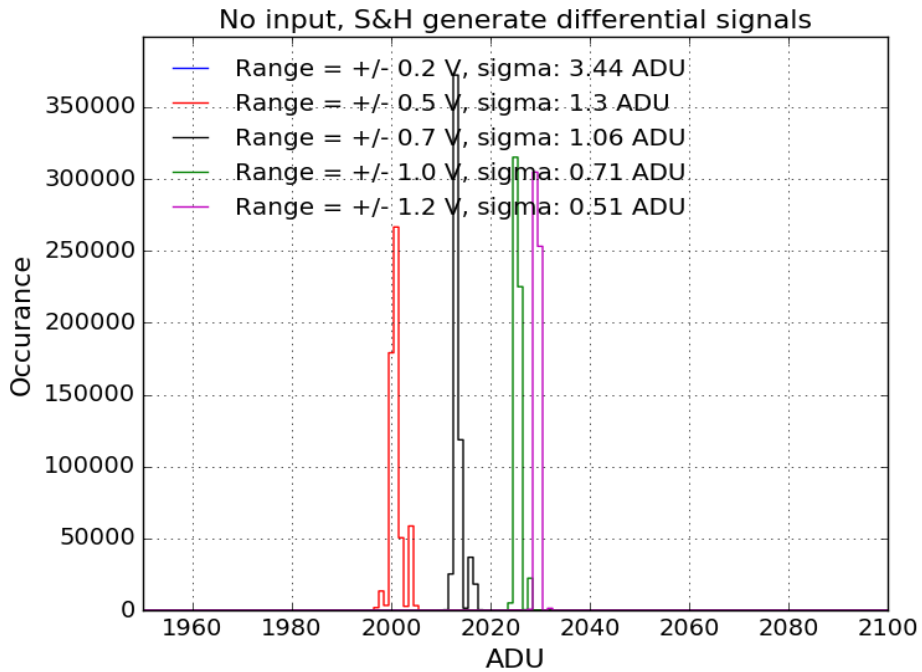
| Unit. Cap C | $C_{para}$ | $C_{c1}$ | $C_{c2}$ | $C_x$ |
|---|---|---|---|---|
| 20 fF | 38 fF | 4.2 fF | 2.0 fF | 62.5·C |
| 40 fF | 27 fF | 8.2 fF | 4.3 fF | 35.5·C |
| 60 fF | 32 fF | 7.5 fF | 3.8 fF | 24.5·C |

10 times smaller with optimized layout in ADC-0.3

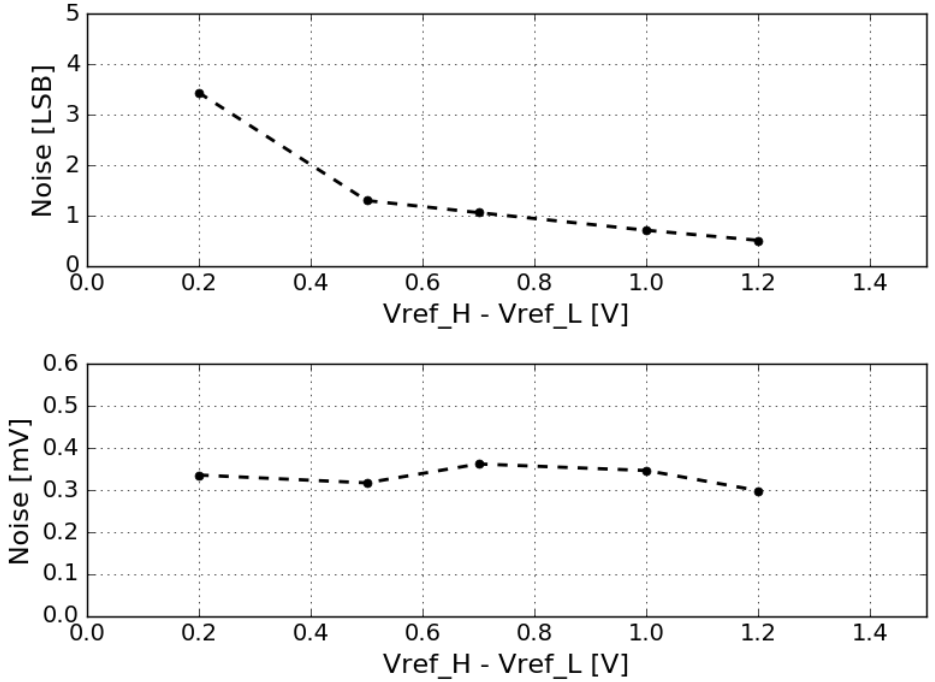
# ADC 0.2 noise

- Internal/intrinsic noise of ADC-0.2: Switch + comparator + ...
  - No external input, S&H used to generate differential signals, $V_{cm}$ = 0.7 V
  - Noise extracted in terms of LSB, 1 LSB = $2*(V_{ref\_H}-V_{ref\_L})/(2^{12}-1)$

Histogram for different $V_{ref\_L}$, $V_{ref\_H}$




Noise for different $V_{ref\_L}$, $V_{ref\_H}$




- Intrinsic noise: ~ 0.3 – 0.4 mV
- Good noise (< 0.5 LSB) for $V_{ref\_H}-V_{ref\_L} \geq 1.2$ V

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# Gotthard 1.7 and ADC 0.2 summary

| | Main issue | Reason | March MPW |
|---|---|---|---|
| G-1.7 | noise | transistor size of pre-amplifier | variations of pre-amplifiers for optimization |
| ADC-0.2 | noisy codes at two ends of input range | settling time to charge big capacitors | longer delay for charging big capacitors |
| | | $V_{cm}$ coupling | separated $V_{cm}$ in sampling and comparison cycles |
| | missing codes | parasitic of bridge capacitor | adjustable side capacitance (2 bit configuration) |
| | | coupling from LSB-DAC to comparator input | improved DAC layout |

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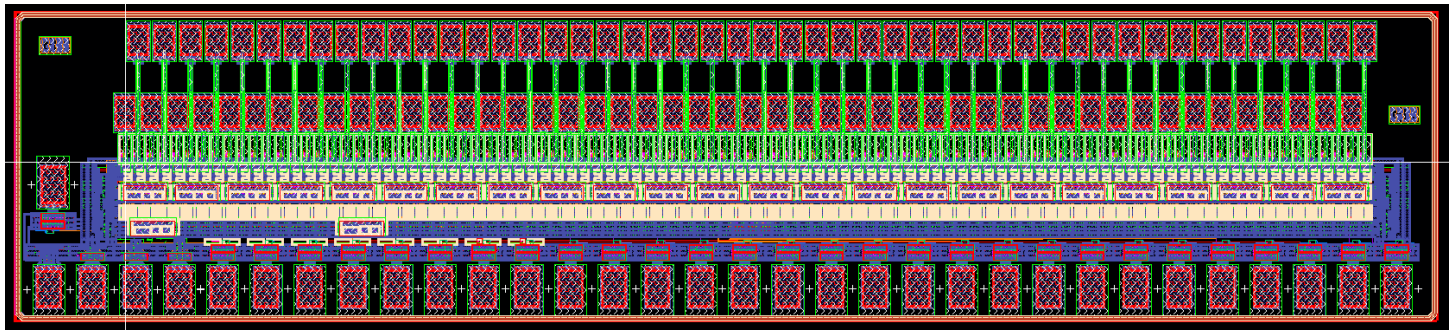
# Test structures submitted in MPW in March

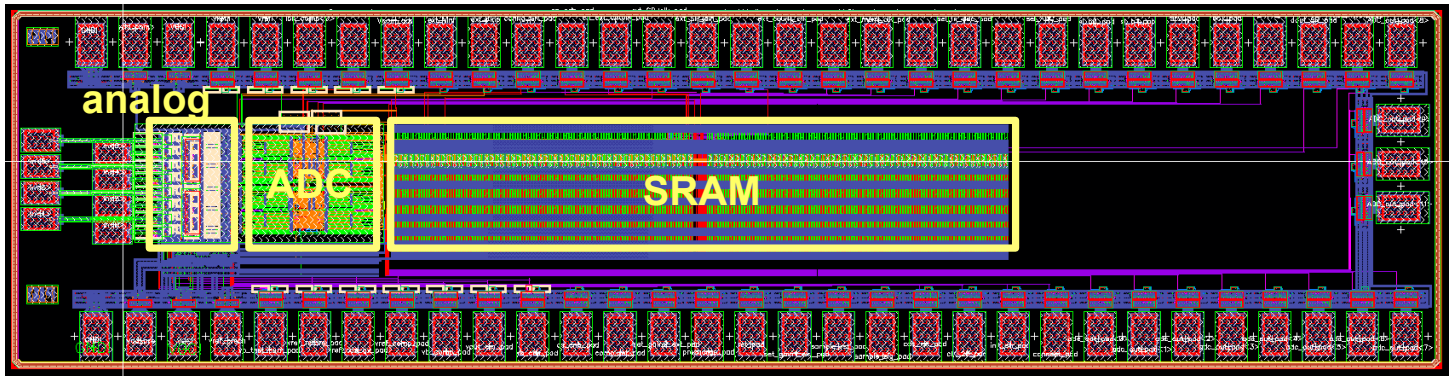
- submission 10.03.2017:

Analog front-end G-1.8:
8 variations,
analogue readout



ADC-0.3:
Unit cap. 20, 30, 40 fF,
Cx trimming

Complete chain G-1.9:
Analog + ADC + SRAM



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# Summary

- Gotthard-1.7 analogue FE characterized
  - Noise: 300 $e^-$ for G0 → ok, but try to optimize noise in 1.8 FE
  - Capacitive cross talk after gain switching 0.5 12.4 keV ph
- ADC0.2 characterized
  - Effective <10 bits, missing codes
  - Problems understood ADC0.3 submitted
- Full chain submitted
- Next steps
  - Test structures from MPW: Gotthard1.8 FE, ADC0.3, full chain
  - Work on design for full chip (engineering run)

    → engineering run end of 17 / beginning 18

    → first modules beginning 18