HOM BPM Signal Processing with FPGA Based Digitizers

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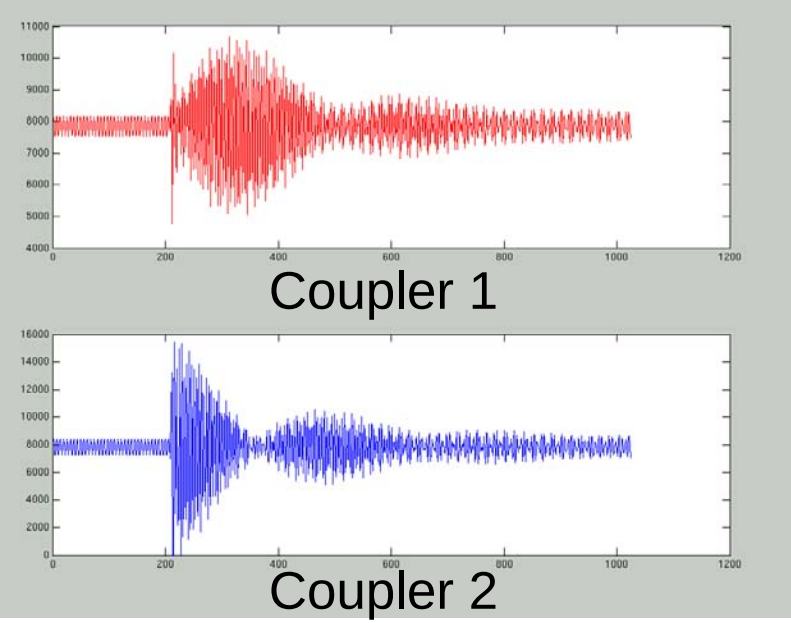
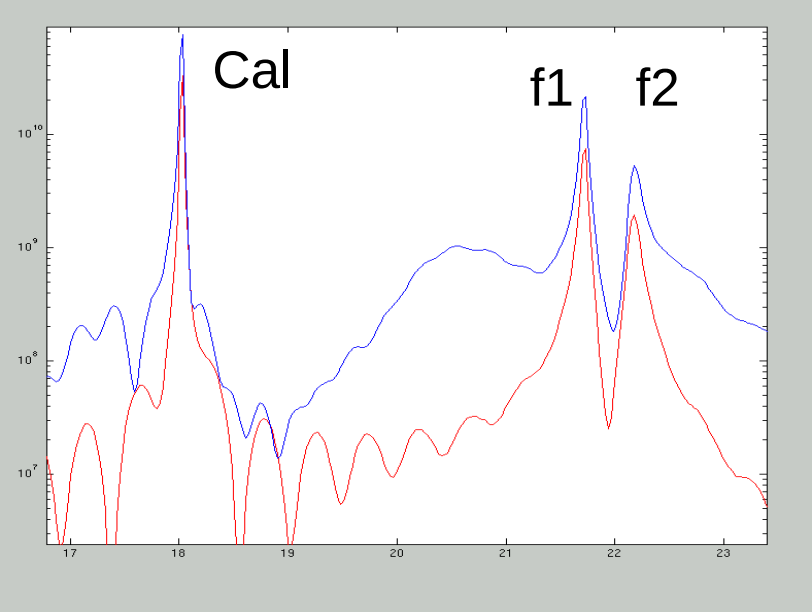
Fermilab

HOM Workshop 1/23/07

Determine HOM Mode Amplitudes





- Want to determine the amplitude & phase of of the degenerate dipole modes
- SVD provides orthogonal vectors…
- By hand can generate sin & cos vectors

HOM BPM Details

Mode Vectors

Raw Data

$$\begin{pmatrix} V_{11} & \cdots & \cdots & \cdots & \cdots & \cdots & V_{1j} \\ \vdots & & & & & & \vdots \\ \vdots & & & & & & \vdots \\ V_{k1} & \cdots & \cdots & \cdots & \cdots & \cdots & V_{kj} \end{pmatrix} \bullet \begin{pmatrix} X_{11} & \cdots & X_{1n} \\ \vdots & & \vdots \\ \vdots & & \vdots \\ \vdots & & \vdots \\ \vdots & & \vdots \\ \vdots & & \vdots \\ X_{j1} & \cdots & X_{jn} \end{pmatrix} = \begin{pmatrix} A_{11} & \cdots & A_{1n} \\ \vdots & & \vdots \\ \vdots & & \vdots \\ A_{k1} & \cdots & A_{kn} \end{pmatrix}$$

Amplitudes

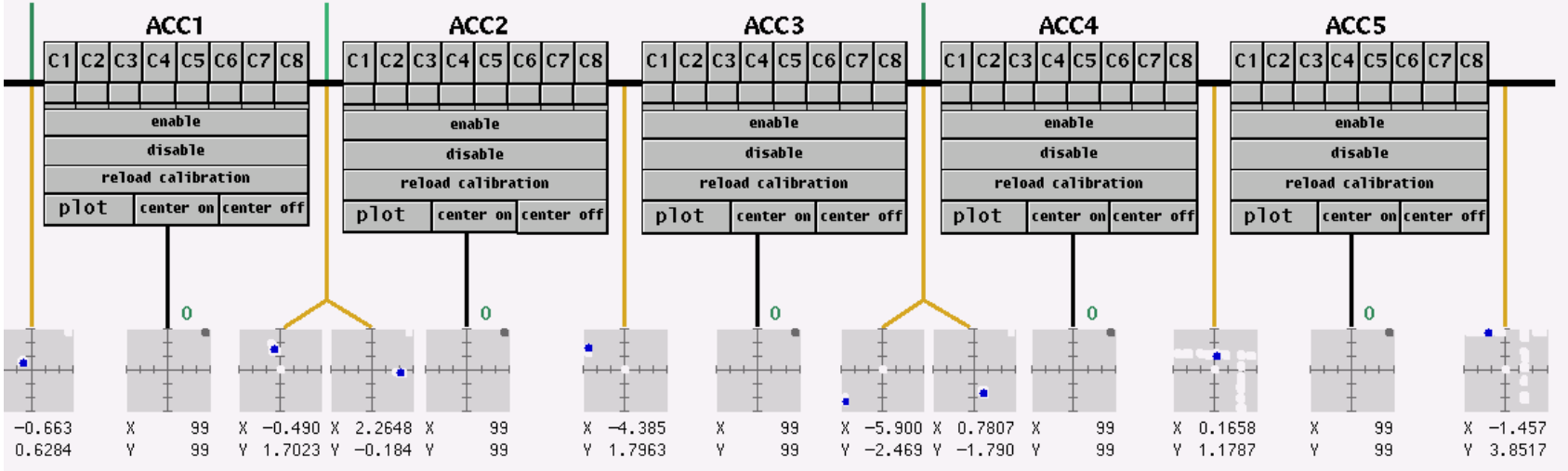
k ~ 6, j ~ 100 to 4k

Calibration Matrix

$$\begin{pmatrix} M_{11} & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & M_{1,k+1} \\ \vdots & & & & & & & & \vdots \\ \vdots & & & & & & & & \vdots \\ M_{41} & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & M_{4,k+1} \end{pmatrix} \bullet \begin{pmatrix} A_{11} & \cdots & \cdots & \cdots & A_{1n} \\ \vdots & & & & \vdots \\ \vdots & & & & \vdots \\ \vdots & & & & \vdots \\ \vdots & & & & \vdots \\ \vdots & & & & \vdots \\ A_{k1} & \cdots & \cdots & \cdots & A_{kn} \\ 1 & 1 & 1 & 1 & 1 \end{pmatrix} = \begin{pmatrix} x_1 & \cdots & \cdots & \cdots & x_n \\ x_1' & \cdots & \cdots & \cdots & x_n' \\ y_1 & \cdots & \cdots & \cdots & y_n \\ y_1' & \cdots & \cdots & \cdots & y_n' \end{pmatrix}$$

4D Position

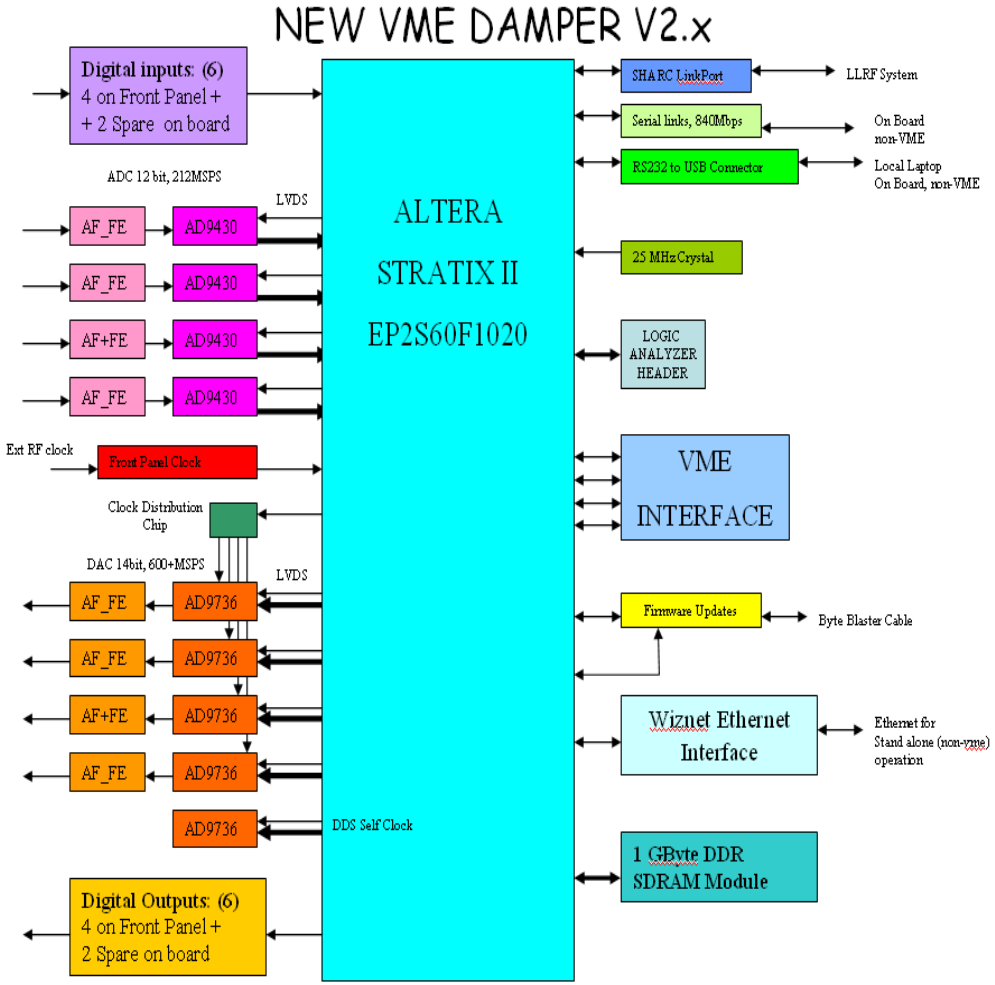
DESY System



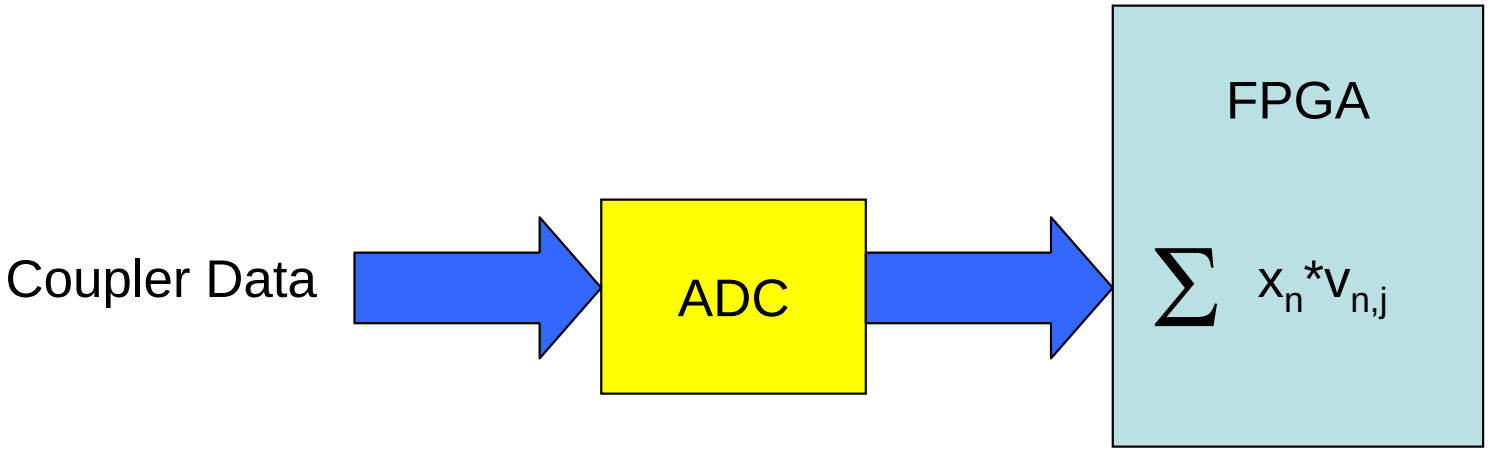
- Need to read out raw data for mod*cav*coupler channels at 4k to 10k data points per for multibunch then perform dot products to determine mode amplitudes
- This requires a lot of I/O in the front-end (slow) and then a bunch multiply accumulates which must be done sequentially on the front-end processor
- The current system is unable to report a position for every pulse at 5Hz for single bunch even with only a few cavities per module enabled

Custom FPGA Based Board

- Extreme flexibility inherent in FPGA
  - Algorithms and functionality can be changed and updated as needed
  - Code base which can be used for multiple projects
  - Intellectual Property (IP) cores provide off the shelf solutions for many interfaces and DSP applications
- The speed of parallel processing
  - Can perform up to 512 multiplies using dedicated blocks
- The Pipeline nature of FPGA logic is able to satisfy rigorous and well defined timing requirements



Dot Product FPGA Implementation



- Store mode vectors in FPGA RAM
- Perform dot product (multiply accumulate) in FPGA for digitized data as it arrives from ADC
- Simply read out mode amplitudes which are available as soon as data has arrived
- Can perform calculation on all channels in parallel
- Also able to store raw data in internal RAM

Dedicated HOM BPM Digitizer

- Dedicated HOM Digitizer
  - Provide amplitudes in real time
  - Reduce front-end processor I/O and load by orders 3-4 orders of magnitude
  - Provide bunch by bunch data for every pulse
- Design dedicated 8 channel digitizer
  - Modify existing design ~ 6 months
  - Commissioning time (have prototype already)
  - Conservative estimate of $200 per channel
- Commercial Solutions
  - Need access to FPGA configuration (can be tricky)
  - Have them developed needed firmware (expensive)