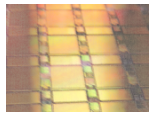
6th Beam Telescopes and Test Beam Workshop 2018

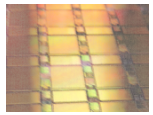
Monolithic Silicon Pixel Detectors in HEP

Petra Riedler, CERN EP-DT

Outlook

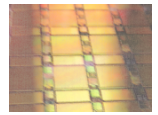


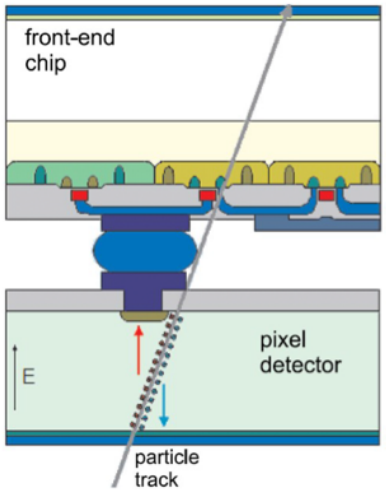
- Pixel detectors - hybrid and monolithic
- A variety of monolithic pixels
- Examples of monolithic pixel detectors in HEP
- Future developments
- Summary

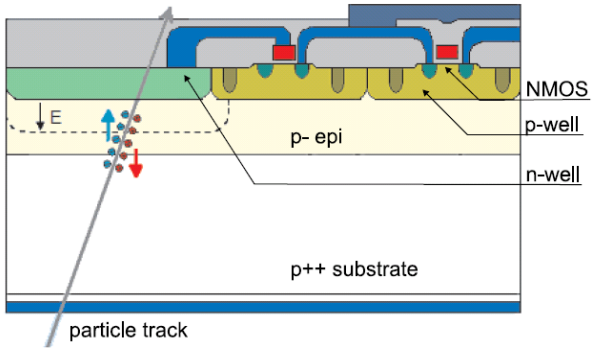


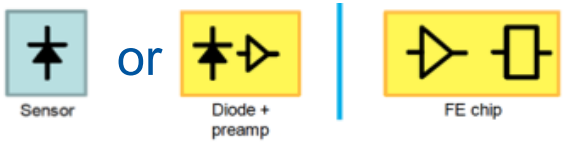
Pixel detectors – hybrid and monolithic

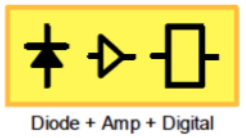
Hybrid Pixels – Monolithic Pixels







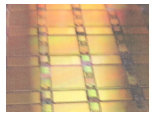




- Separately optimize sensor and FE-chip for very high radiation environment
- Fine pitch bump bonding to connect sensor and readout chip

- Charge generation volume integrated into the ASIC, but many different variants!
- Thin monolithic CMOS sensor, on-chip digital readout architecture

Hybrid Pixels



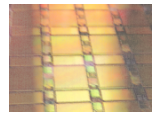
Offer a **number of pros due to the split functionality** of sensor and readout:

- complex signal processing in readout chip
- zero suppression and hit storage during L1 latency
- radiation hard chips and sensors to >10^{15} n_{eq}/cm^2
- high rate capability (~MHz/mm^2)
- spatial resolution ≈10 – 15 µm
- Potential from C2W and W2W assembly

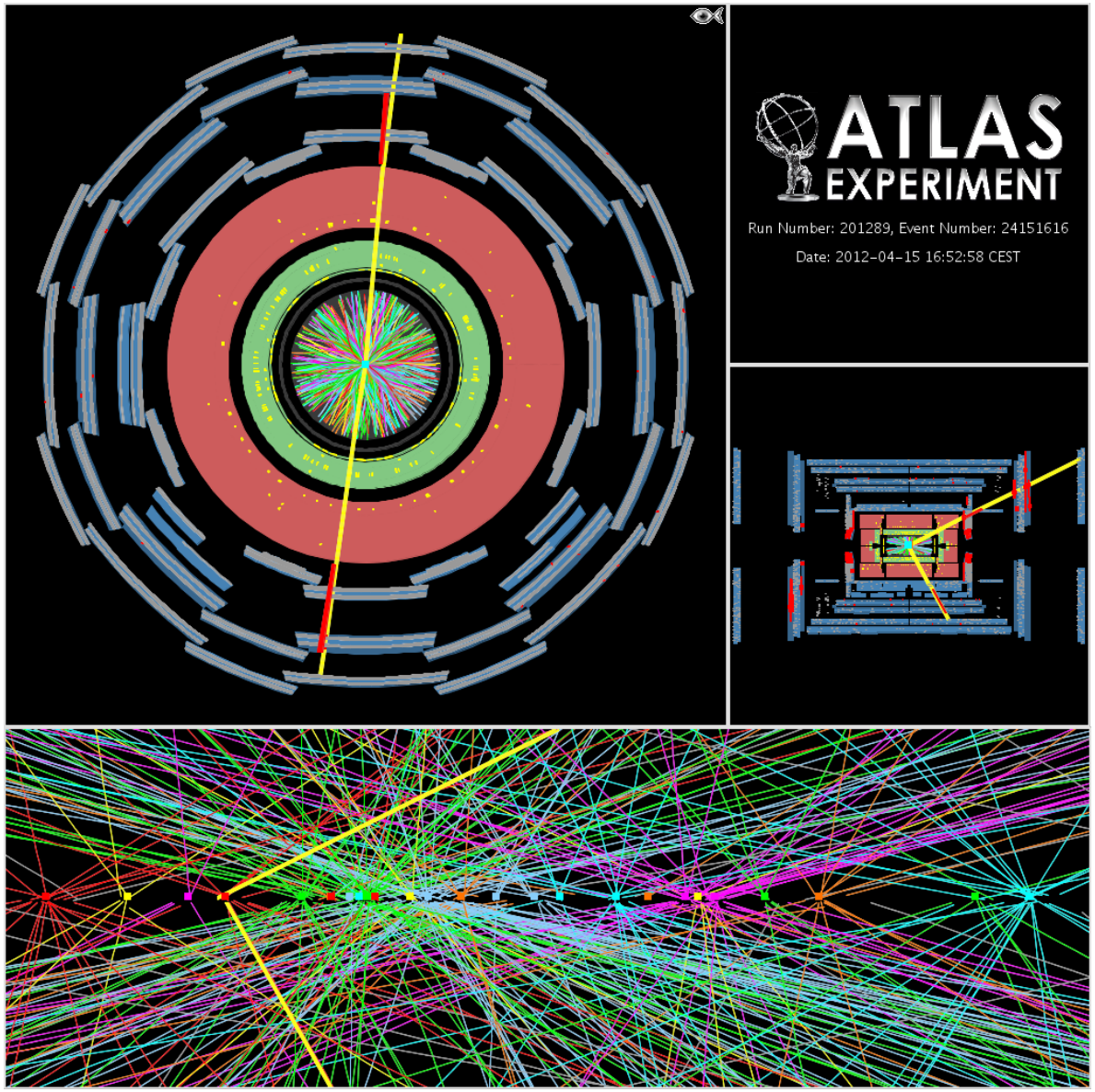
There are also **some aspects which are more cons:**

- relatively large material budget: >1.5% X_0 per layer
- resolution could be better
- complex and laborious module production
- bump-bonding / flip-chip
- many production steps
- expensive

But hybrid pixels are extremely successful and if you look at today's LHC experiments...

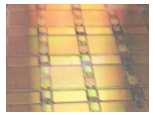


Z → μμ event with 25 reconstructed vertices.

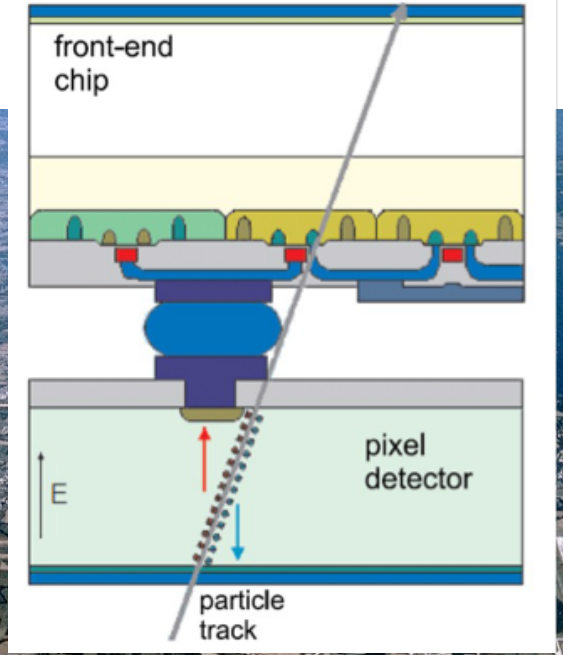


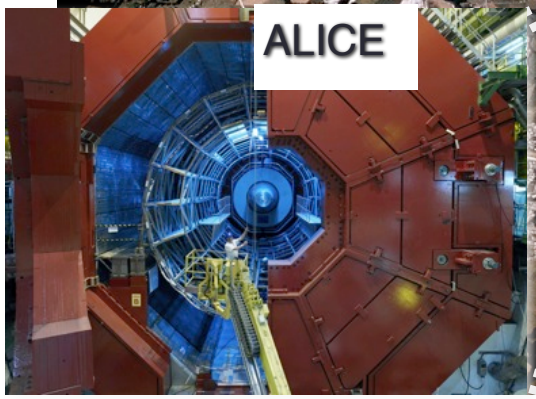
Pixels are installed in the regions closest to the IP

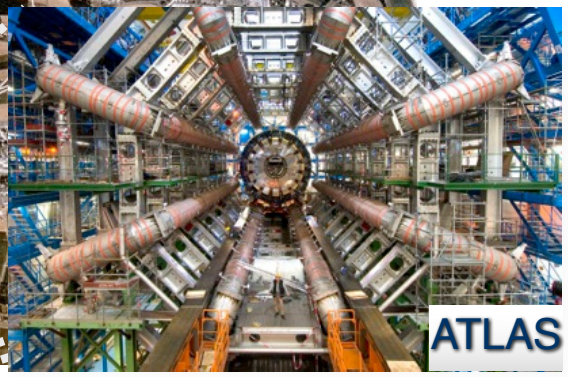
Pixel Detectors at LHC



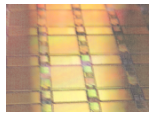
Using hybrid pixels







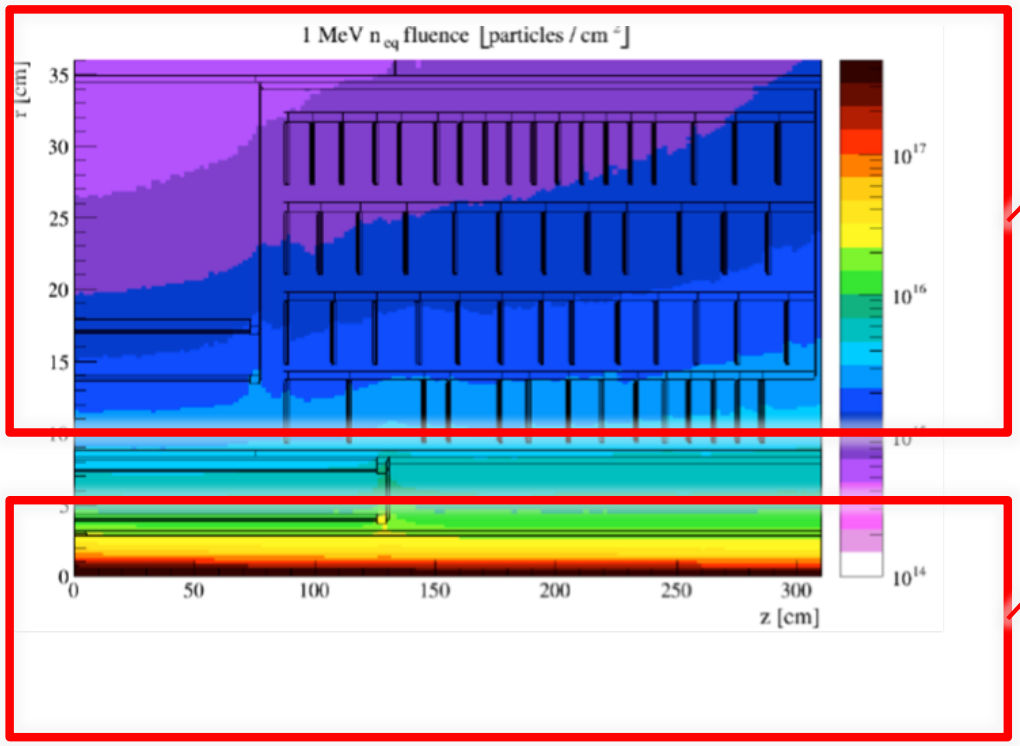
LHC Pixel Environment



Given by LHC radiation levels, hit rates and bunch structure

- 25ns
- L1 trigger rate

Example: ATLAS



Outer Pixel layers

- Occupancy 1MHz/mm^2
- NIEL ~ 10^{15} neq/cm^2
- TID ~ 50Mrad
- Larger area O(10m^2)

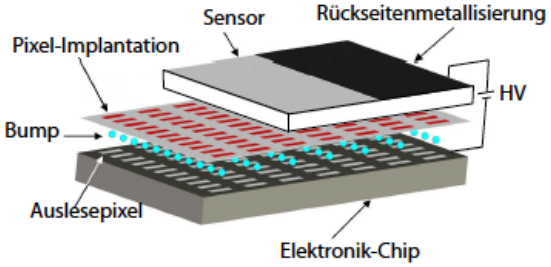
Inner Pixel layers

- Occupancy 10MHz/mm^2
- NIEL ~ 10^{16} neq/cm^2
- TID ~ 1Grad
- Smaller area O(1m^2)

~1997

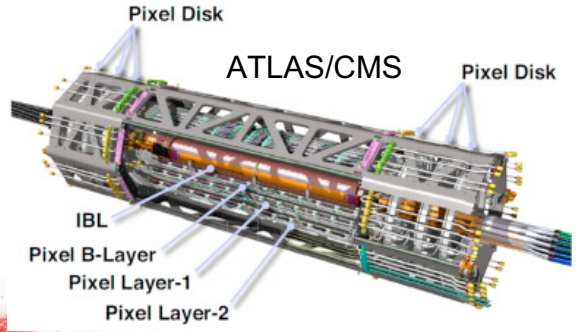
N. Wermes
HSTD11, Okinawa, 2017

Hybrid pixel detectors



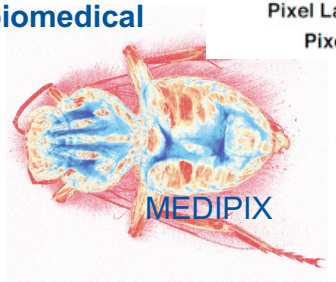
HEP tracking

- LHC
- HI

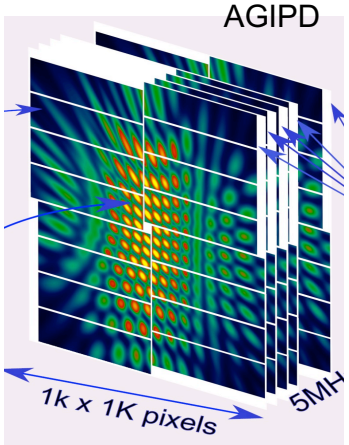


Imaging

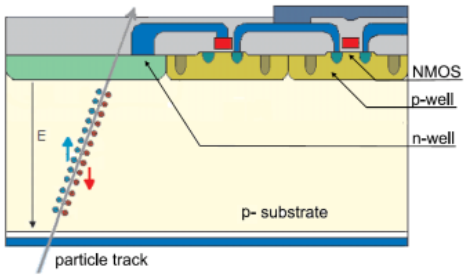
- biomedical



- photon science

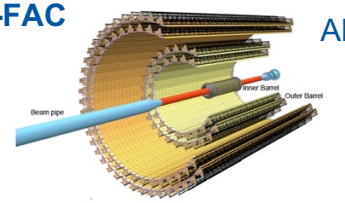


Monolithic pixel detectors



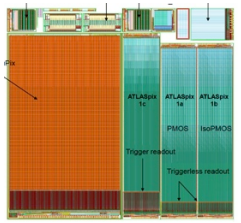
HEP tracking

- HI, B-FAC



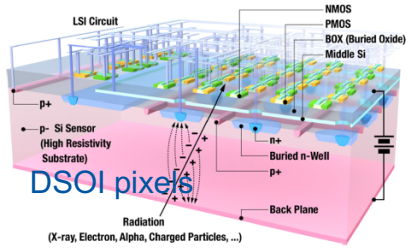
ALICE ITS

ATLAS CMOS



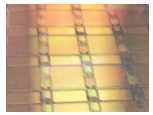
- LHC

Imaging

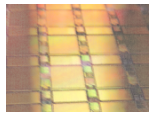


DSOI pixels

2017



A variety of monolithic pixels



CMOS Active Image Pixel Sensors

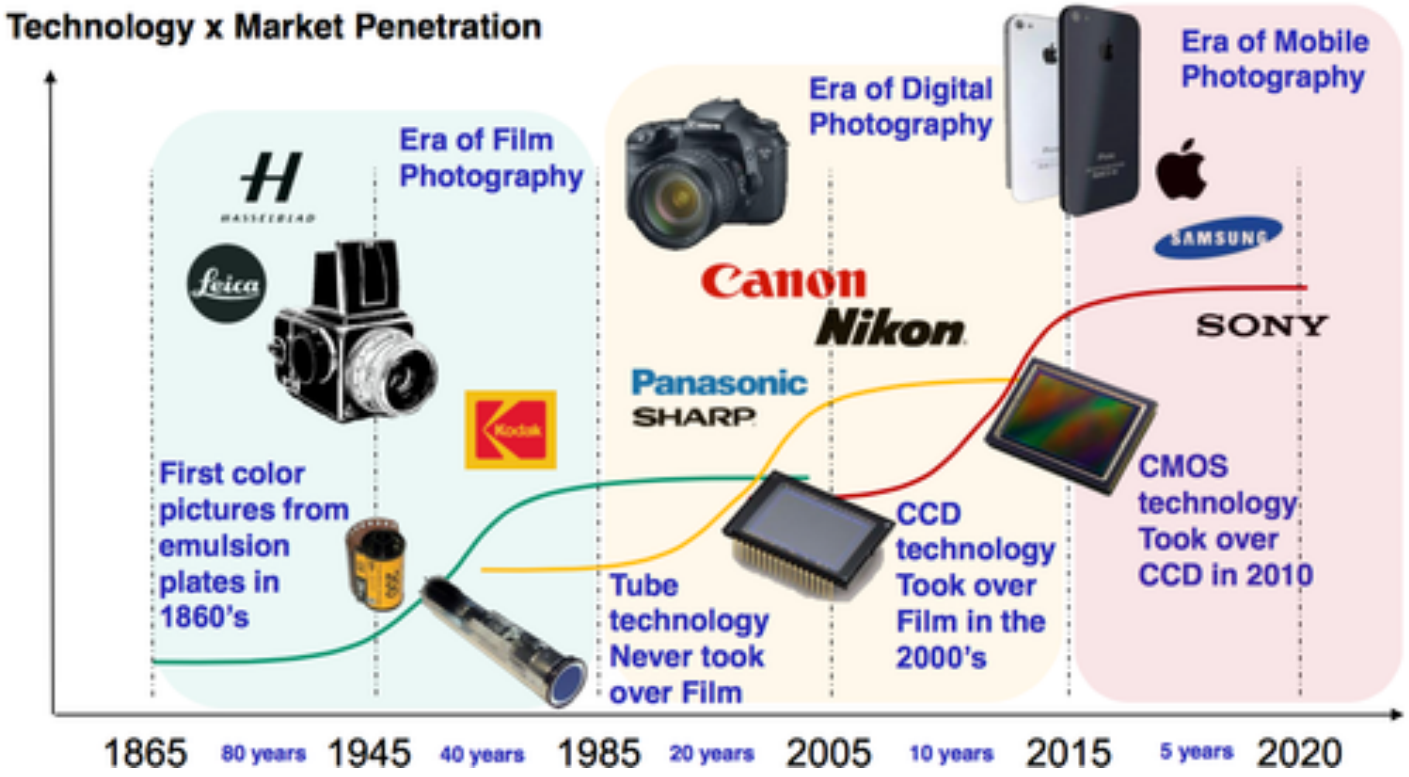
- CMOS active image pixel sensor developed by NASA/JPL (patents by Caltech) in 1992, plus proposals in HEP*
- Used (vanilla) CMOS process available at many foundries → easily accessible
- First versions contained in-pixel source follower amplifier for charge gain, low noise Correlated Double Sampling, basis for camera-on-chip
- Though specialized fab processes are required, the market has driven developments leading to CMOS sensors dominating the field.

ER Fossum, CMOS Active Pixel Sensors – Past, Present and Future, 2008
https://pdfs.semanticscholar.org/6d85/af67a846d13b7e7502f7fa96c0729c972590.pdf

*In HEP, e.g.
S. Parker, A proposed VLSI pixel device for particle detection
NIMA 275 (1989), 494-516

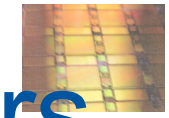
CMOS Active Image Pixel Sensors

- While 1980s were dominated by CCDs (camcorder market)
- The 1990s/2000s have shown an increasing demand for CMOS imaging sensors due to the camera phone market



http://www.eetimes.com/document.asp?doc_id=1325655&image_number=1

CMOS Active Image Pixel Sensors



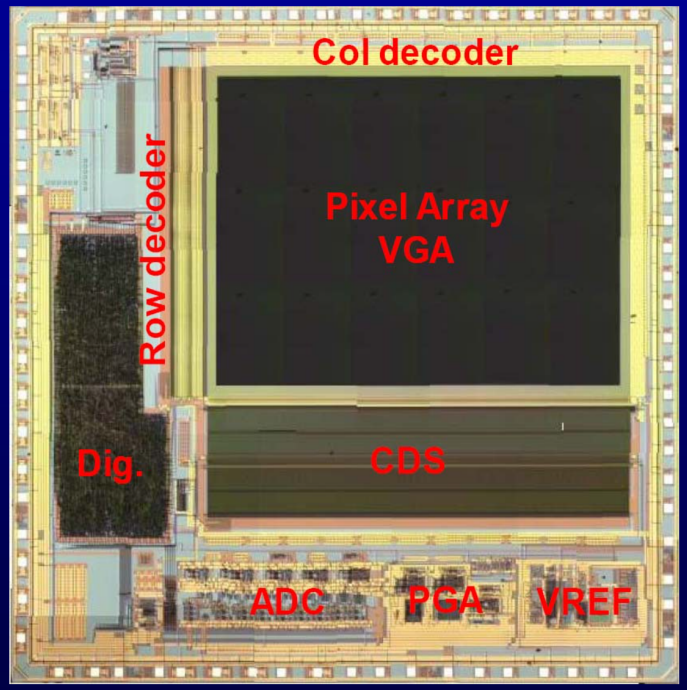
What are the advantages of CMOS imaging sensors (camera-on-chip) in industry? For example:

- Low power, important for portable devices
- Compact cameras due to system-on-a-chip
- Fewer components needed

ER Fossum, CMOS Active Pixel Sensors – Past, Present and Future, 2008
https://pdfs.semanticscholar.org/6d85/af67a846d13b7e7502f7fa96c0729c972590.pdf

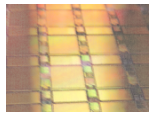
Camera-on-a-chip

- Pixel array
- Signal chain
- ADC
- Digital logic
  - I/O interface
  - Timing and control
  - Exposure control
  - Color processing
- Ancillary circuits



Pain et al.
2007 IISW

Monolithics in HEP?

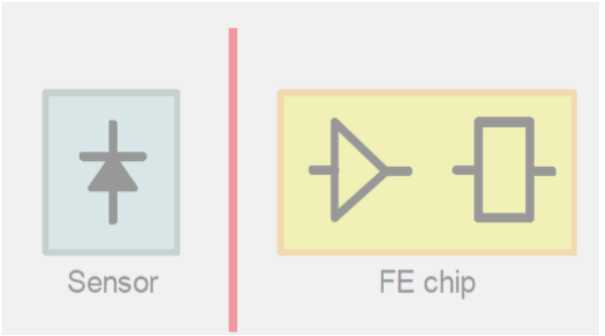


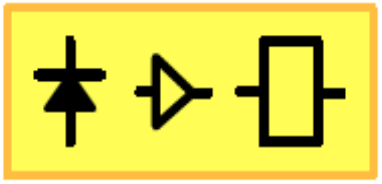
Silicon trackers are part of the core tracking systems of all present LHC experiments.

Monolithic pixel detectors can offer a number of interesting advantages for HEP experiments:

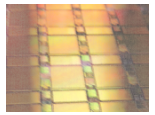
- Commercial process (8” or 12” wafers)
- Multiple vendors
- Potentially cheaper interconnection processes available
- Thin sensor (50-100 um) have less material and reduce cluster size at large eta
- ..

Strong interest in monolithic pixels, with many different variants!



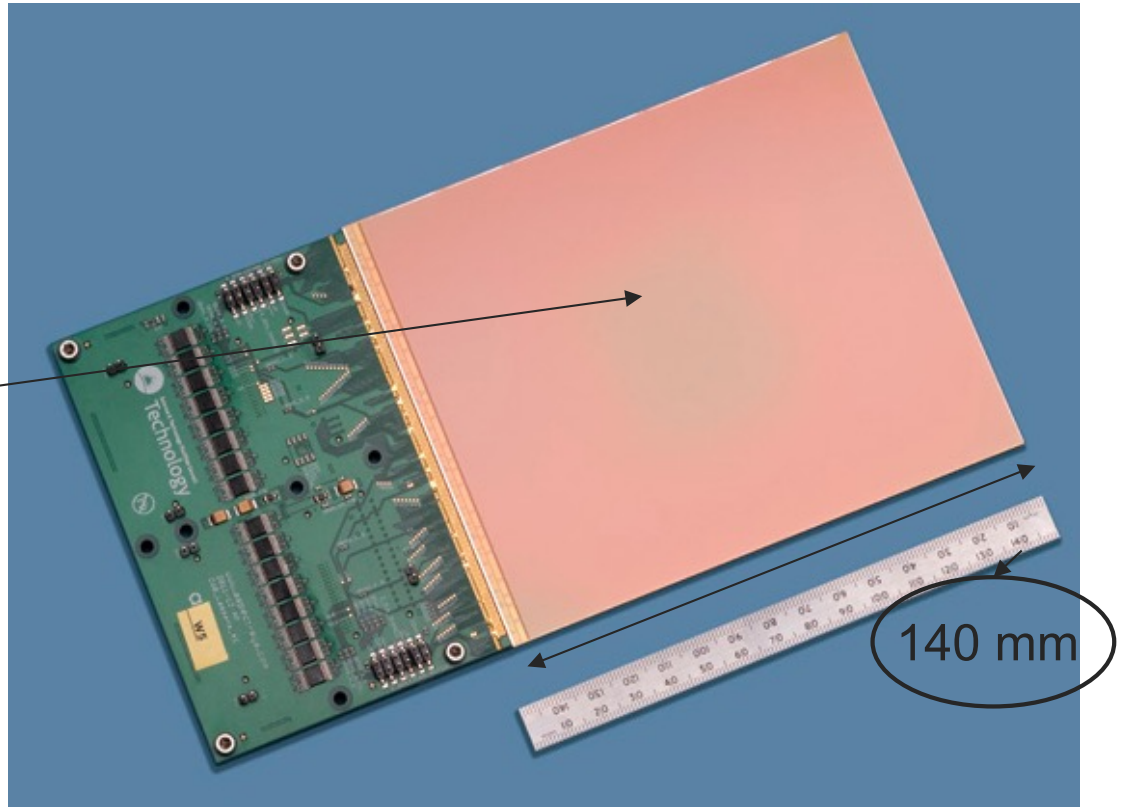


MAPS (Monolithic Active Pixel Sensors) for Imaging and More



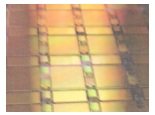
Many developments in the field of CMOS imaging sensors and MAPS in general within the community!

Example:
Wafers scale (8”) imaging sensor developed by the RAL team (stitched)



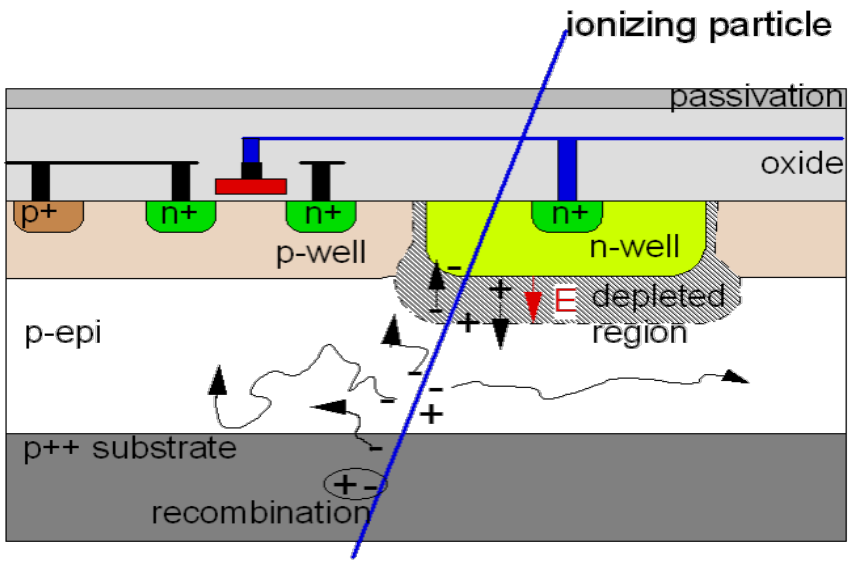
N. Guerrini, RAL, 5th school on detectors, Legnaro, April 2013

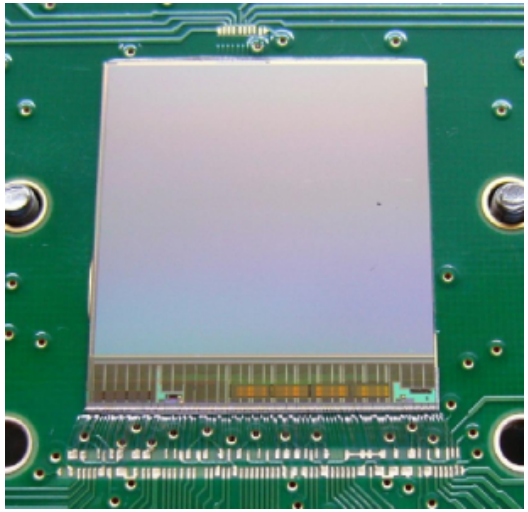
MAPS



Developments lead by IPHC created a number of monolithic pixel sensors of the MIMOSA family:

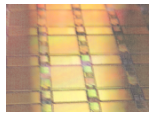
- Epitaxial wafers with collection diode and few transistors per cell (size ~ 20 x 20 μm^2), limited to NMOS transistors
- 0.35 µm CMOS technology with only one type of transistor
- Rolling shutter architecture (readout time O(100 µs))
- Charge collection mostly by diffusion
- Limited radiation tolerance (< 10^{13} n_{eq} cm^{-2})

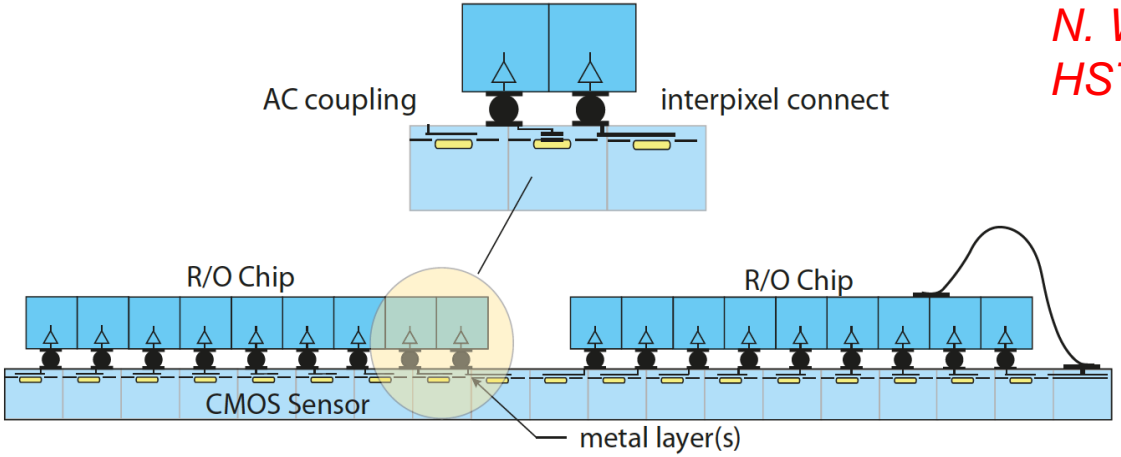




ULTIMATE chip for STAR HFT (IPHC Strasbourg)

„Passive“ CMOS Sensors



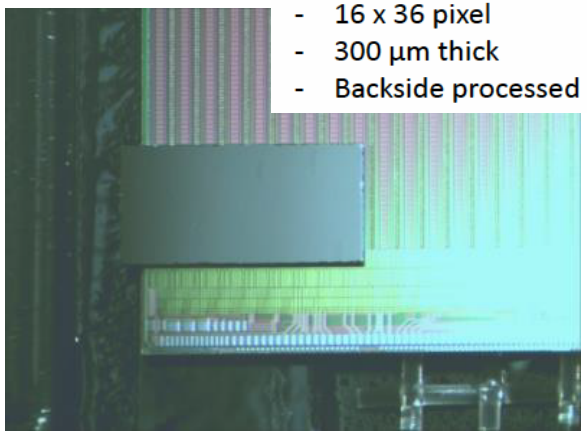


N. Wermes
HSTD11, Okinawa, 2017

- can have in-pixel **AC coupling**
- fancy **RDL** possibilities by metal layers

- **Cheap,** large feature size technology possible
- no extra bumping step, because bumps (**C4**) come with CMOS fabrication
- do flip-chipping in-house (large pitch)
- large sensors possible (→ reticule stitching)
- may be even wafer based flip-chipping (8“)

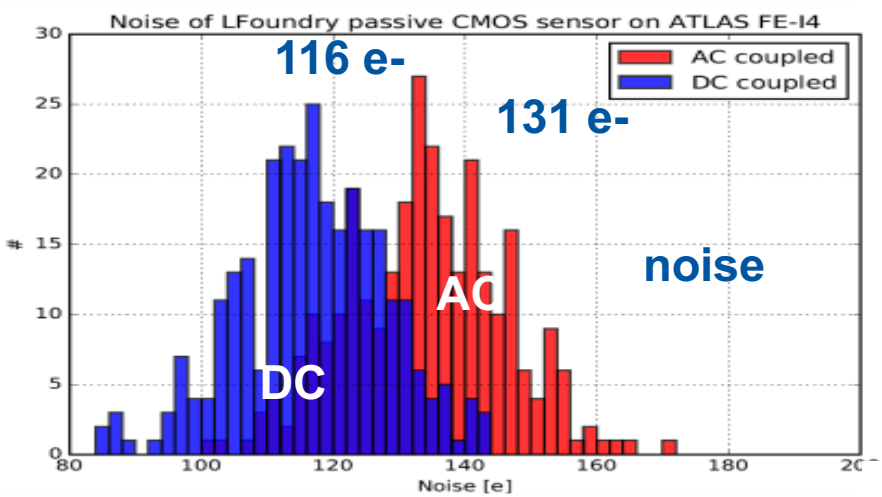
- LFounry 150 nm CMOS technology
- 2k Ωcm p-type bulk
- ATLAS FE-I4 pixel size (50 µm x 250 µm)
- 16 x 36 pixel
- 300 µm thick
- Backside processed



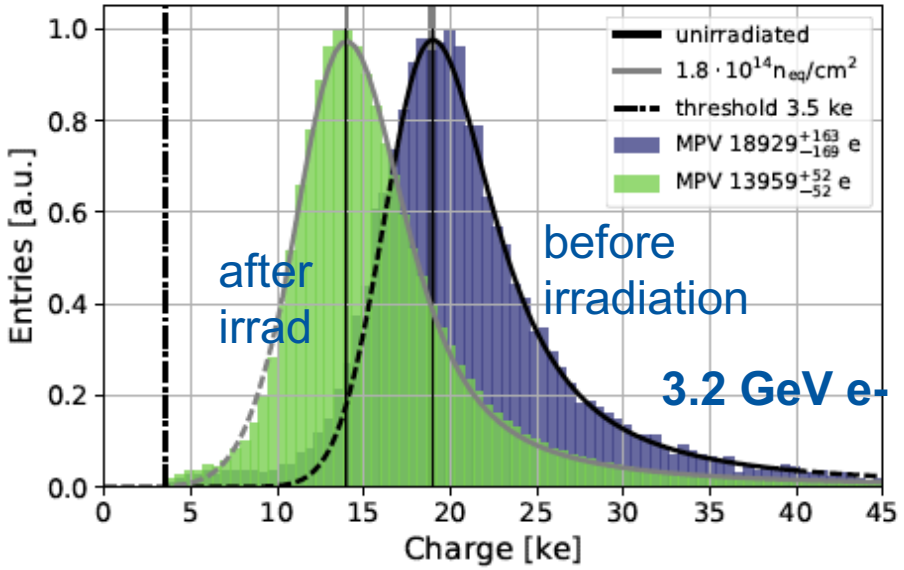
D.-L. Pohl et al., JINST 12 (2017) no.06, P06020

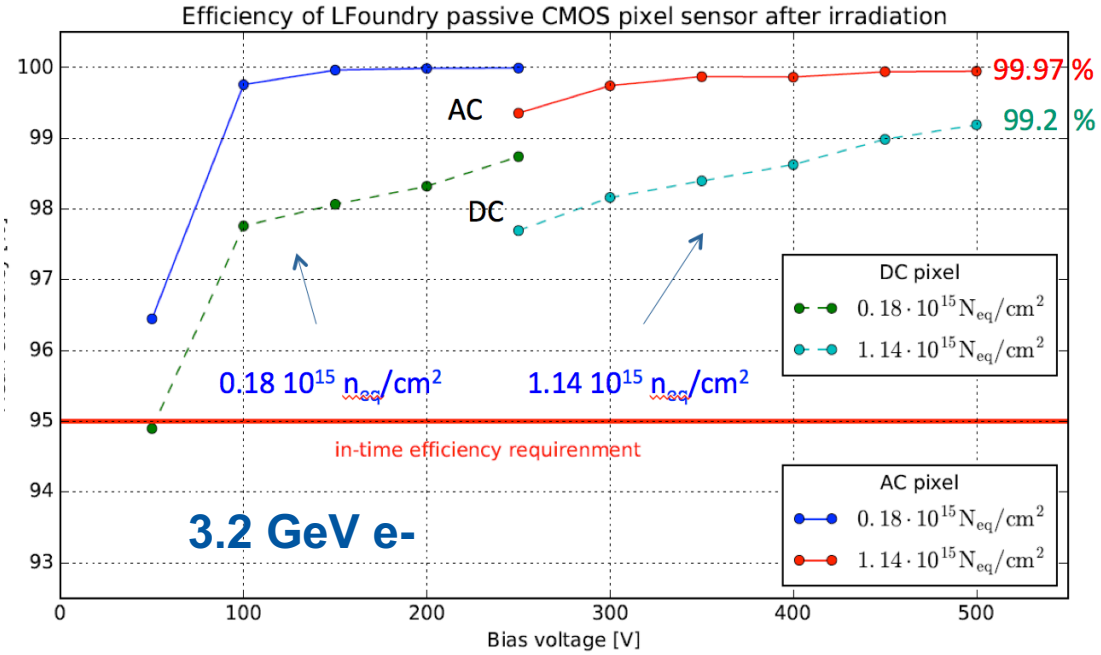
Performance of Passive CMOS Sensors

N. Wermes
HSTD11, Okinawa, 2017



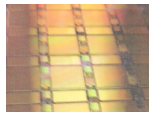
- **IV** curves of all samples ok (bias 120 V -> 500 V)
- about **220 µm** depletion depth
- leakage current **20 µA / cm³** (IBL: 15 µA/cm³)
- **noise** as in standard sensors
  - planar sensors (C_D = 117 fF): ENC = 120 e-
  - 3D-Si sensors (C_D = 180 fF): ENC = 140 e-
- **high efficiency after irradiation** (1 x 10^{15} n_{eq}/cm^2)





D.-L. Pohl et al., JINST 12 (2017) no.06, P06020

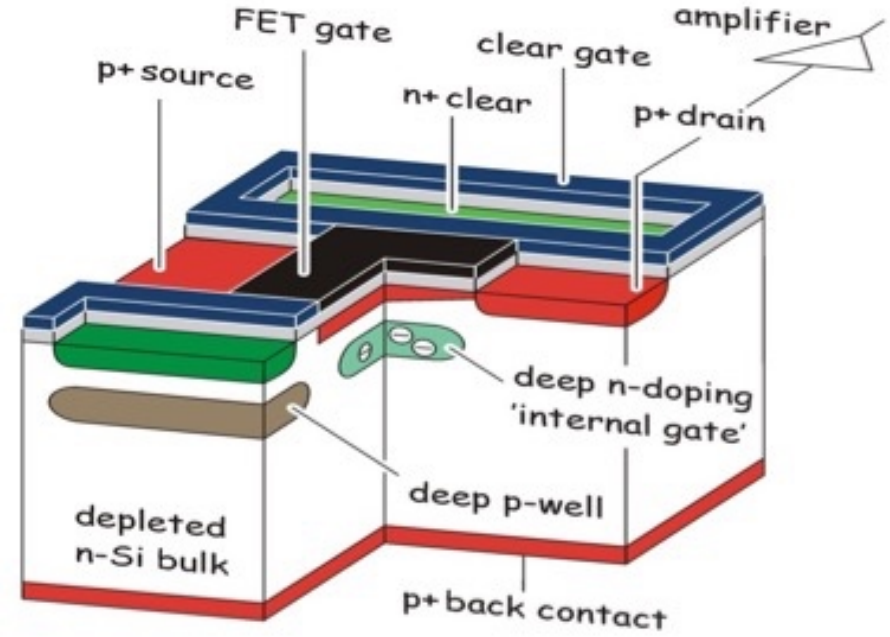
DEPFET

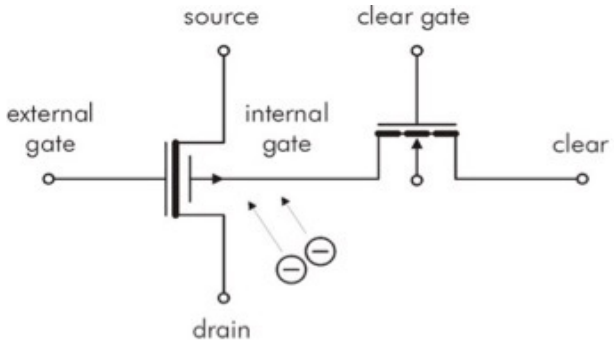


- **Depleted p-channel FET on high resistivity substrate (Kemmer & Lutz, 1987)**

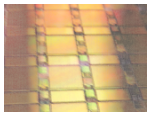
- First stage amplification in pixel
- Fully depleted bulk
- Charge is stored underneath an internal gate causing a modulation in the transistor current
- Charge needs to be cleared after readout
- Requires off-chip read-out circuitry

- **Used in the BELLE II pixel detector upgrade**



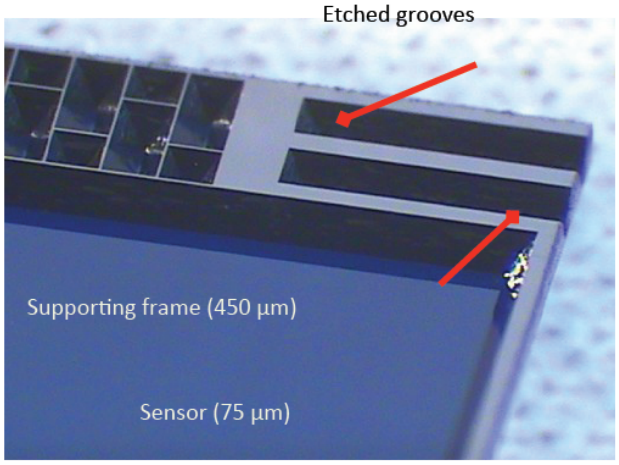


Belle II Pixel Detector at SuperKEKB: DEPFET

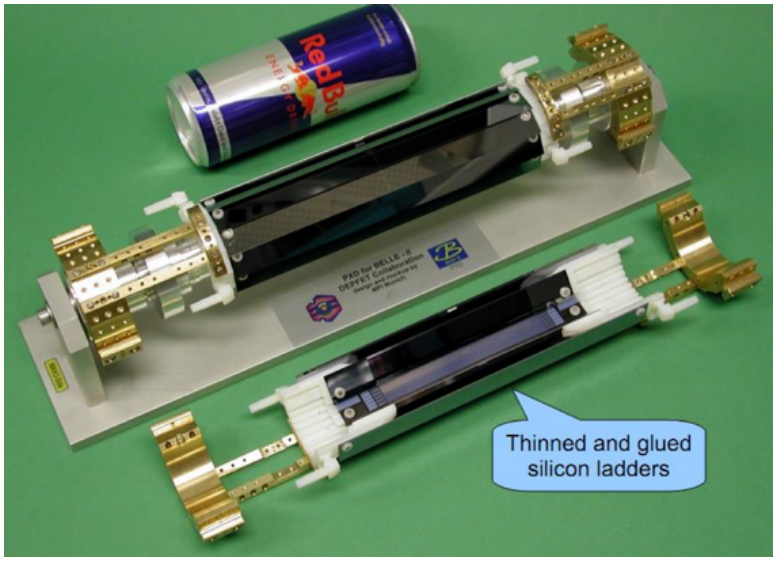


Pixel detector based on **DEPFET** sensors

- 2 barrel layers (r=1.4 cm and 2.2 cm)
- Pixel size 50 µm x 75 µm
- Row-wise read-out (rolling shutter), 20 µs/frame
- Special thinning of the matrix area to reduce material budget (75 µm thick)



C. Lacasta, VERTEX 2013

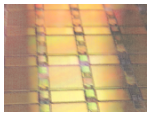


S. Tanaka, HSTD9, 2013

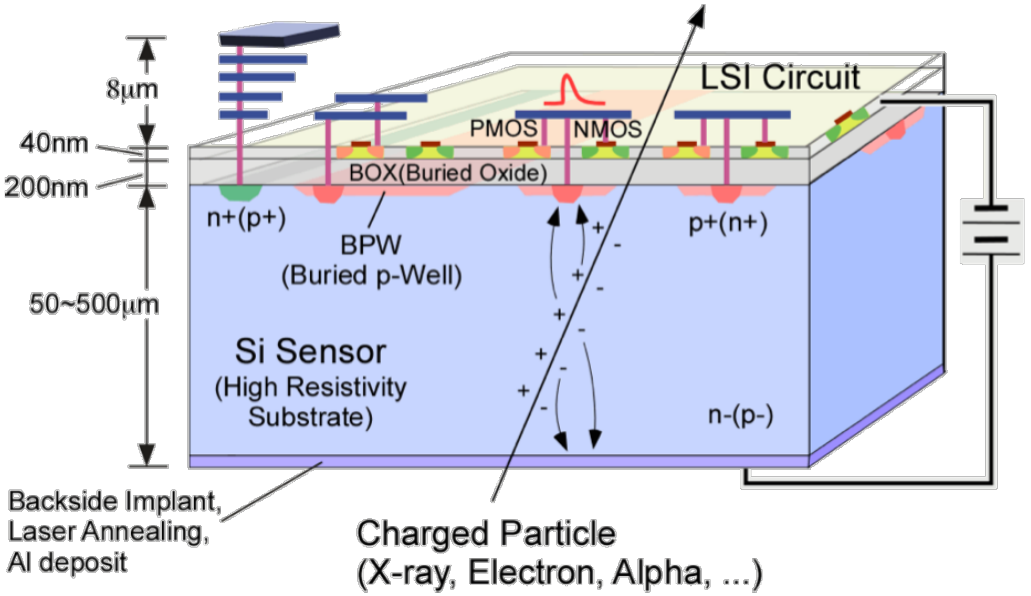
Radiation environment:
~ 1.9 Mrad / year
~ 1.2 10^{13} 1MeV n_{eq}/cm^2 per year

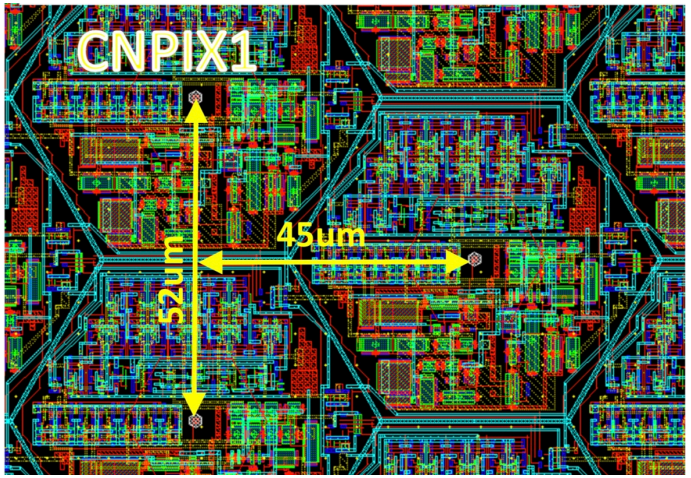
Material budget:
0.21 % X_0 per layer

SOI - Silicon On Insulator

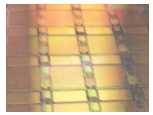


- SOI wafer with high resistivity sensor part and thin CMOS chip connected via oxide
- Fully depleted thick sensing region with low C, offers good Q/C
- Is one of the ways to integrate large amount of in-pixel circuitry
- Main issues (back-gate effect, signal cross talk and radiation tolerance) being addressed by using burried wells, double SOI and pinned depleted diodes.



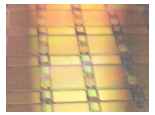


Y. Arai, HSTD11, Okinawa 2017

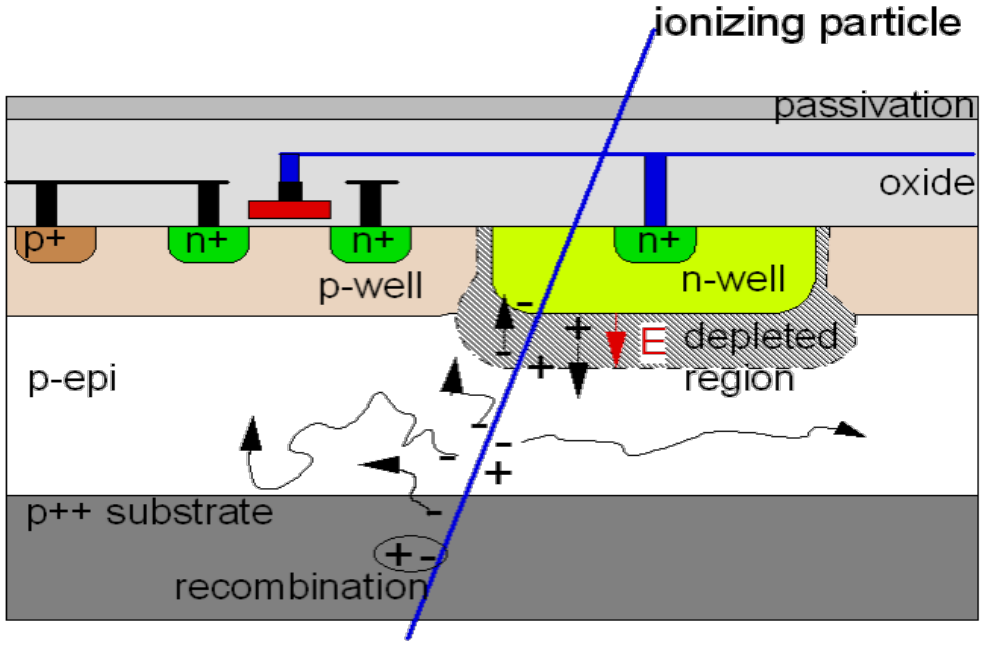


Examples of monolithic pixels in HEP

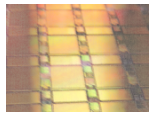
MAPS



In the remaining part of the presentation, focus on MAPS, their applications in HEP and future developments for high radiation environment.

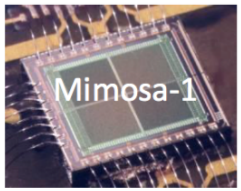


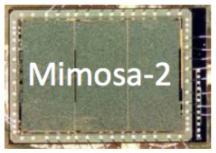
MAPS Evolution

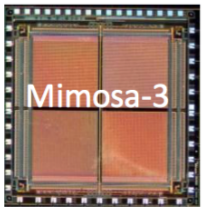


L. Musa, 30 years HI Forum
November 2016

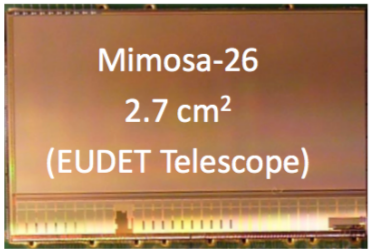
Owing to the industrial development of CMOS imaging sensors and the intensive R&D work (IPHC, RAL, CERN)

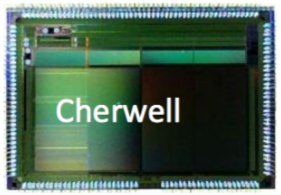


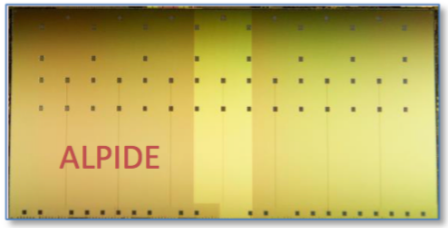




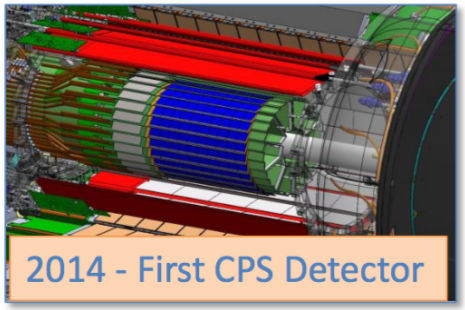
...



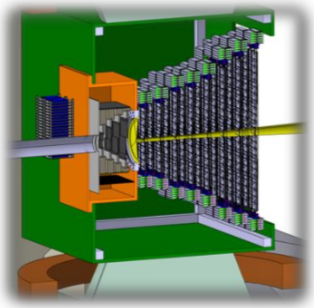




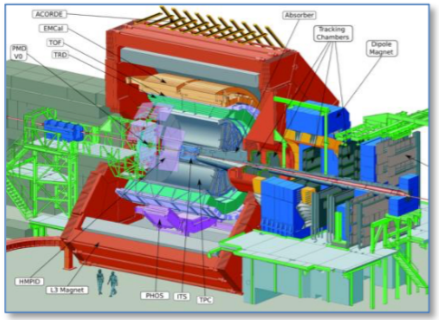
... several HI experiments have selected CMOS pixel sensors for their inner trackers



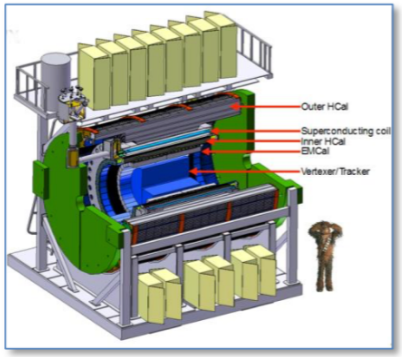
STAR HFT
0.16 m² – 356 M pixels



CBM MVD
0.08 m² – 146 M pixel



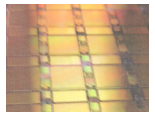
ALICE ITS Upgrade (and MFT)
10 m² – 12 G pixel



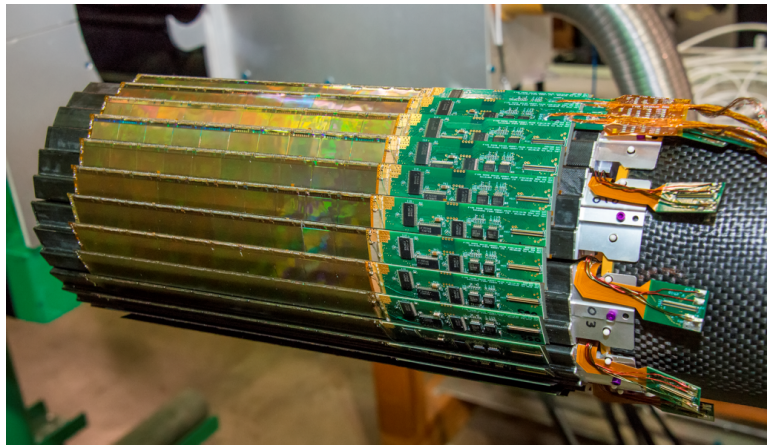
sPHENIX
0.2 m² – 251 M pixel

30

STAR Heavy Flavour Tracker



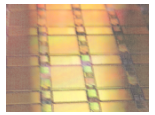
The upgrade of the STAR HFT included also the installation of the **first MAPS based vertex tracker at a collider experiment.**



DCA Pointing resolution	(10 ⊕ 24 GeV/p·c) μm
Layers	Layer 1 at 2.8 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 μm (6 μm geometric)
Position stability	5 μm rms (20 μm envelope)
Material budget first layer	X/X_0 = 0.39% (Al cond. cable)
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year $2*10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	< 1 day

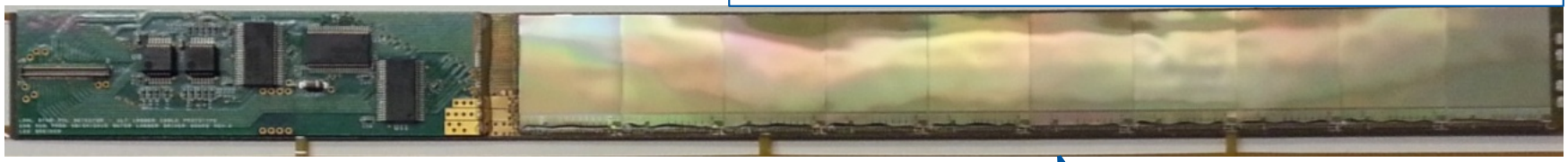
After R&D and prototyping the construction of 3 trackers started in 2013.

STAR HFT



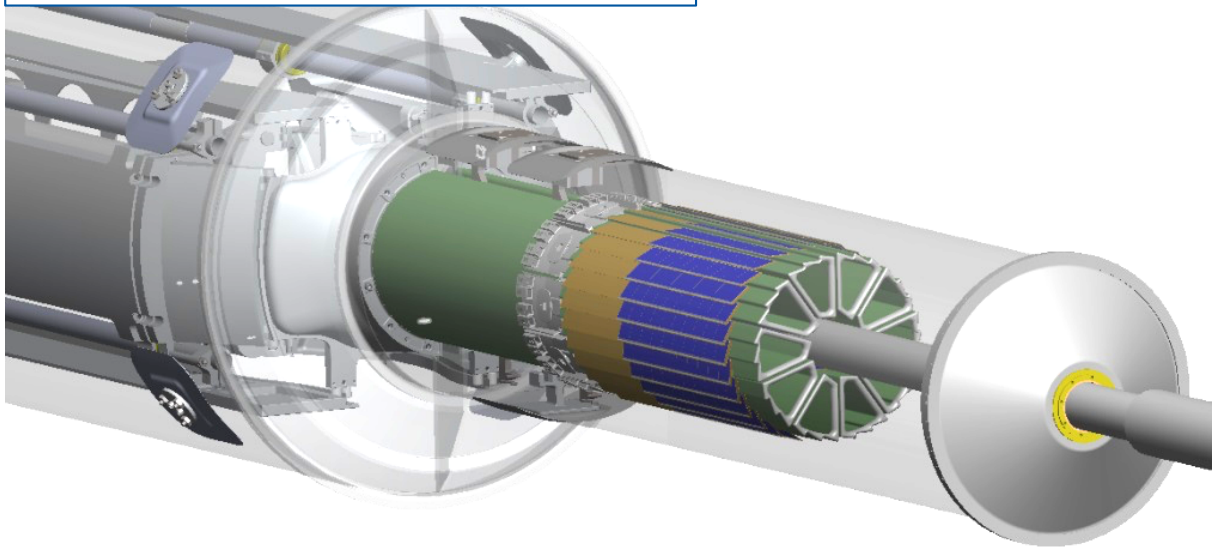
Basic Detector Element

Ladder with 10 MAPS sensors (~ 2×2 cm each)



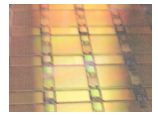
10 sensors / ladder
4 ladders / sector
5 sectors / half
10 sectors total

Mechanical support with kinematic mounts (insertion side)

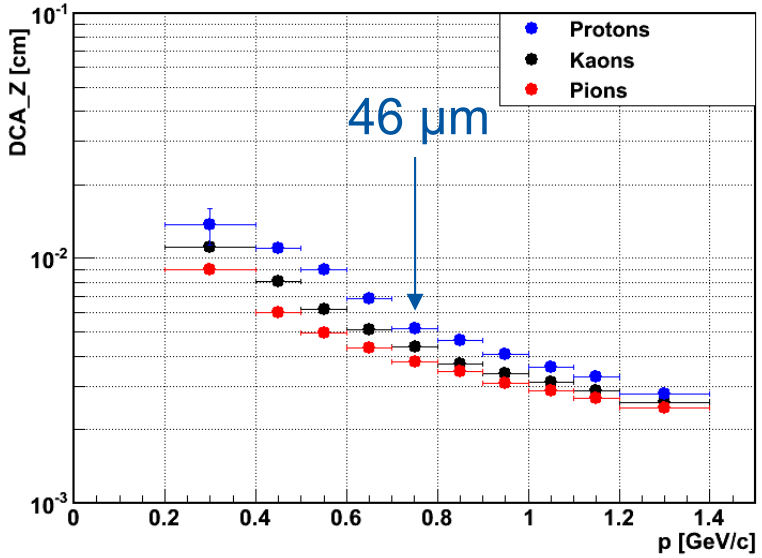


carbon fiber sector tubes (~ 200 µm thick)

STAR HFT

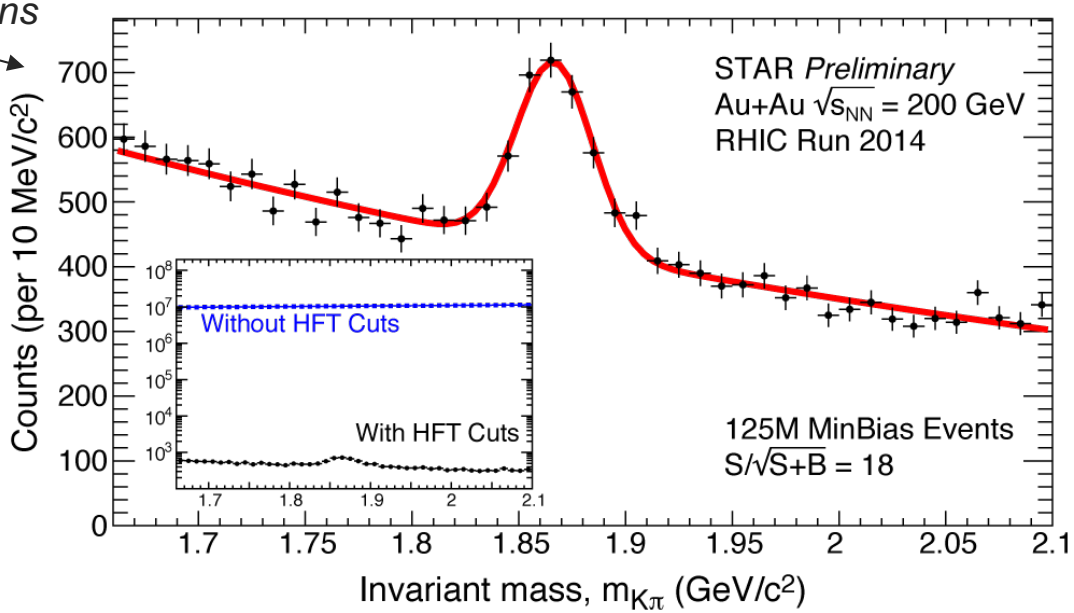


- DCA pointing resolution
  - Design requirement exceeded: 46 μm for 750 MeV/c Kaons for the **2 sectors** equipped **with aluminum cables on inner layer**
  - ~ 30 μm for p > 1 GeV/c
  - From 2015: all sectors equipped with aluminum cables on the inner layer



$D^0 \rightarrow K\,\pi$ production *in* $\sqrt{s_{NN}}$ **=** *200GeV Au+Au collisions (partial event sample)*

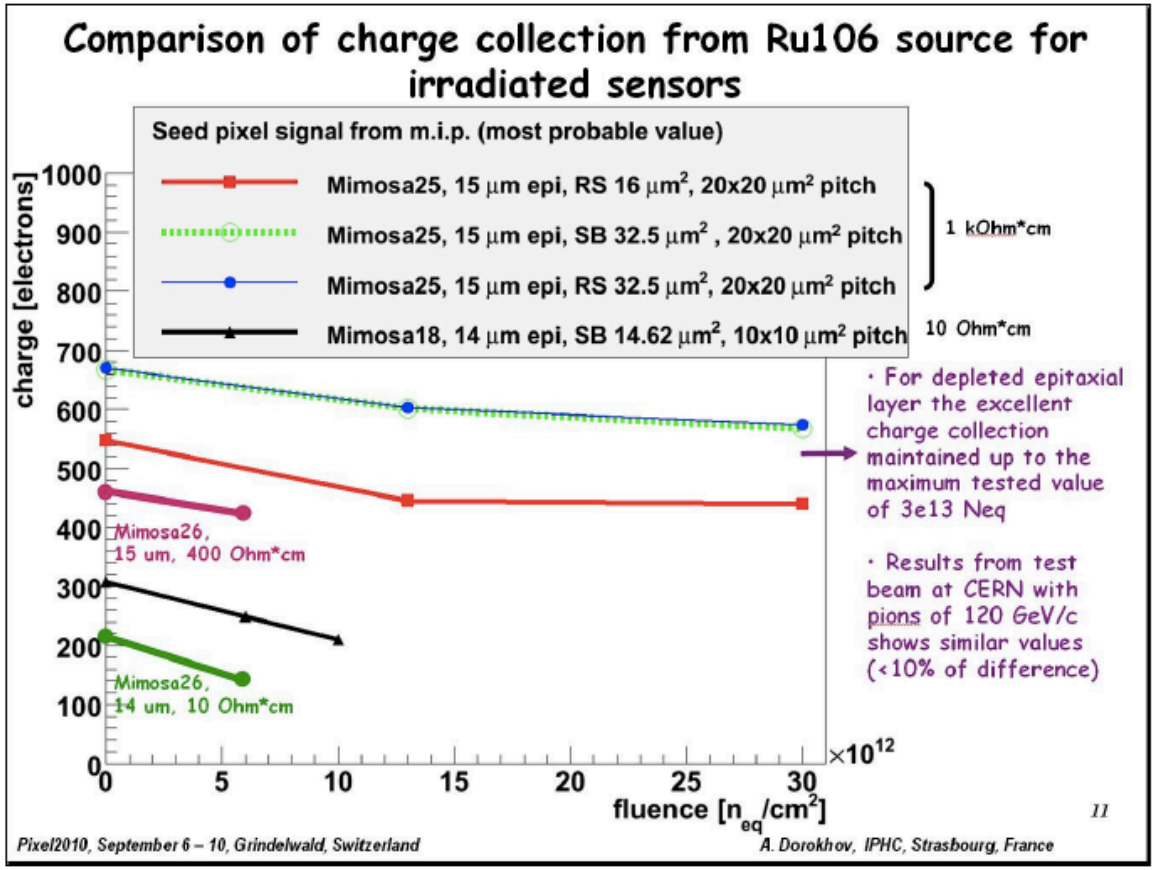
- Physics of D-meson productions
  - High significance signal
  - Nuclear modification factor R_{AA}
  - Collective flow v_2
- First Λ_c^+ signal observed in HI collisions (QM 2017)!

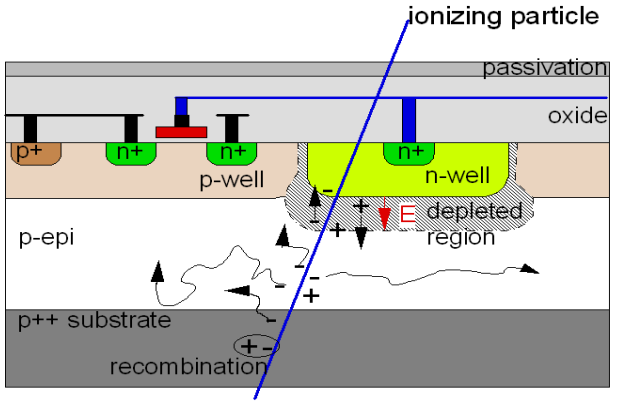


Radiation Tolerance

Transistor radiation tolerance comes “for free” for deep sub micron processes and improved design layout.

Charge collection by diffusion suffers from radiation damage beyond 10^{13} n_{eq} cm^{-2}!

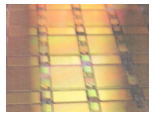




Deplete part or all of the charge generation volume to **collect charge by drift**

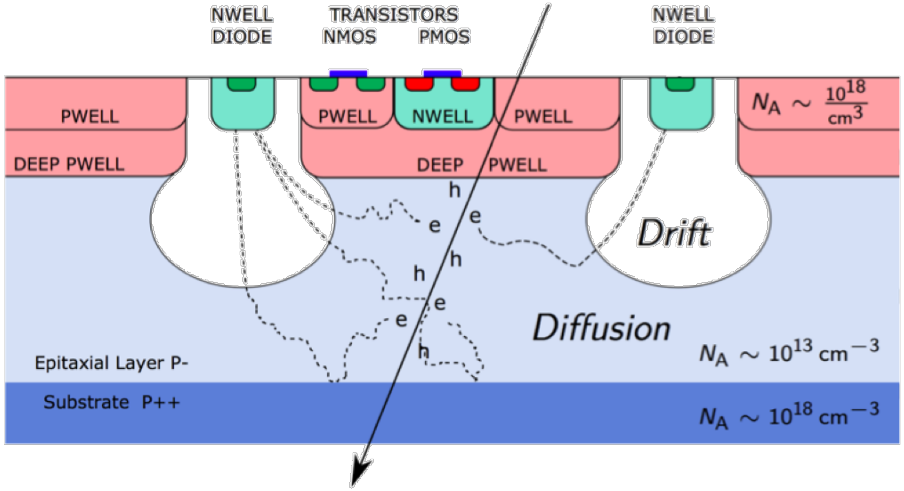
A. Dorokhov et al., Pixel 2010

MAPS – next step



TowerJazz 0.18µm CMOS imaging process

- N-well collection electrode in high resistivity epitaxial layer (>1kOhmcm)
- Present state-of-art based on **quadruple well allows full CMOS**
- **High resistivity (> 1kΩ cm) epi-layer** (p-type, 20-40 µm thick) on p-substrate
- **Moderate reverse bias => increase depletion region** around Nwell collection diode to collect more charges by drift



ALICE Inner Tracking System Upgrade

Based on high resistivity epi layer MAPS

3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

Radial coverage: 21-400 mm

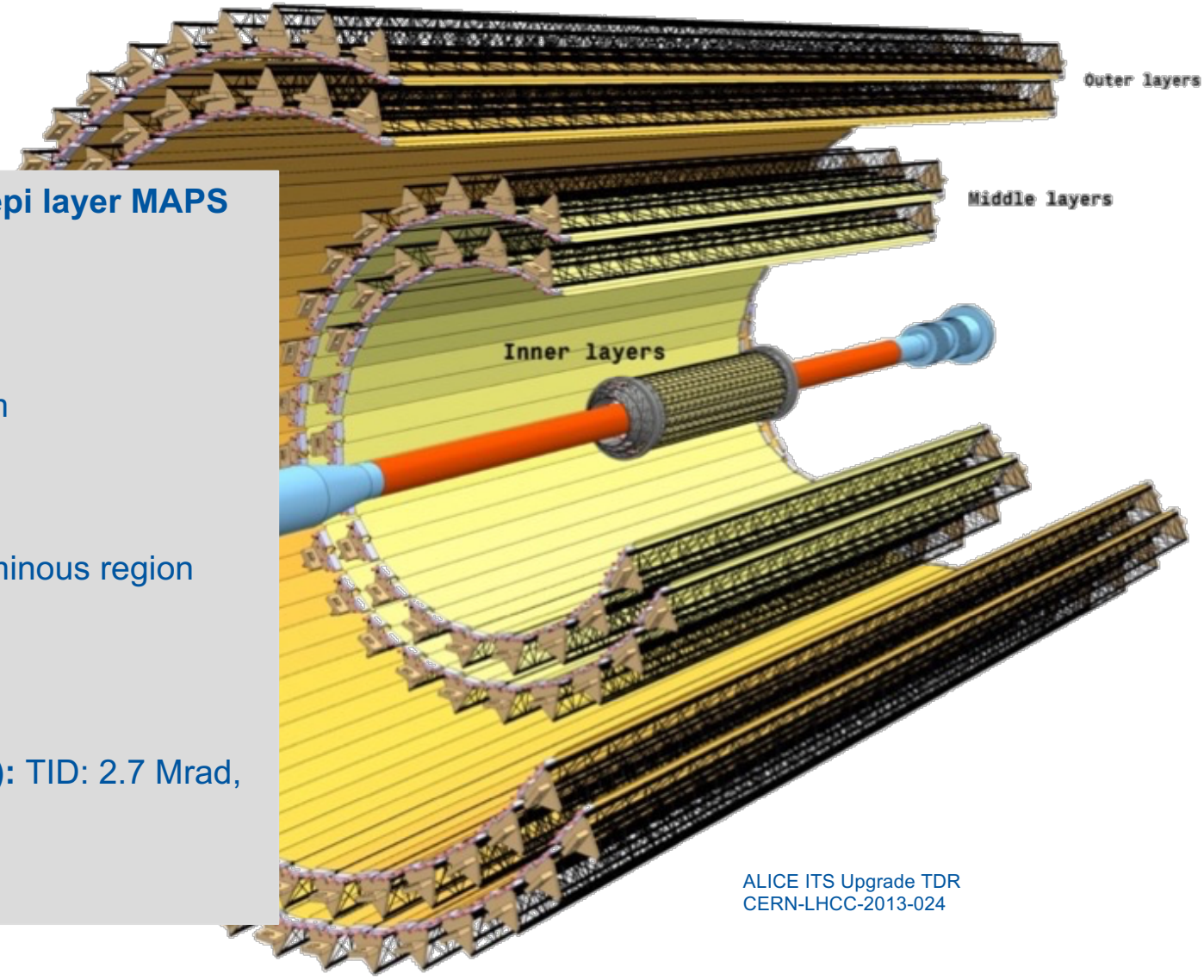
~ 10 m^2

$|\eta|<1.22$ over 90% of the luminous region

0.3% X_0/layer (IB)
0.8 % X_0/layer (OB)

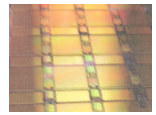
Radiation level (IB, layer 0): TID: 2.7 Mrad, 1.7 x 10^{13} 1 MeV n_{eq} cm^{-2}

Installation during LS2

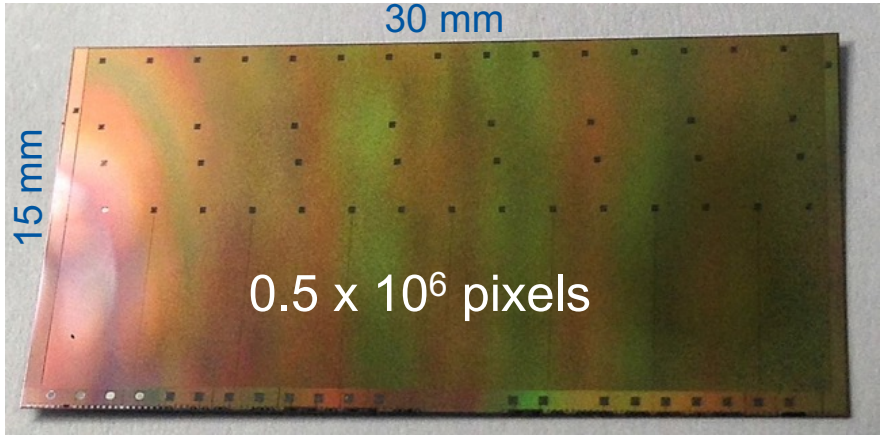


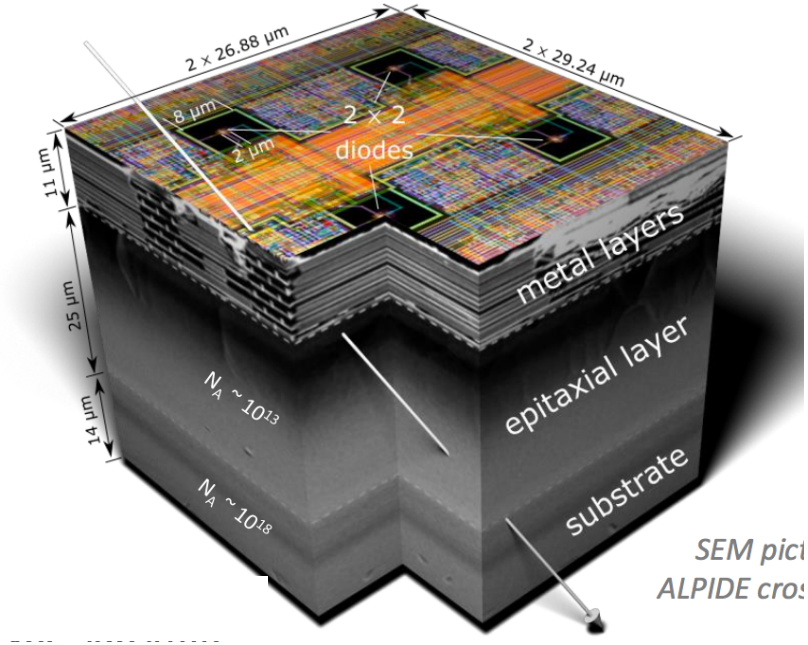
ALICE ITS Upgrade TDR
CERN-LHCC-2013-024

ALPIDE Chip



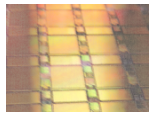
- Pixel size: 29 x 27 μm^2 with low power front-end (40 nW)
- Small n-well diode (2 μm diameter), ~ 100 times smaller than pixel size
- Asynchronous sparsified digital readout
- **Power density ~300 nW/pixel**
- Minimized inactive area on the edge due to pads-over-matrix design (~ 1.1 x 30 mm^2)
- Full size prototypes produced on different epitaxial wafers
- **Partial depletion of the sensitive region due to back bias**

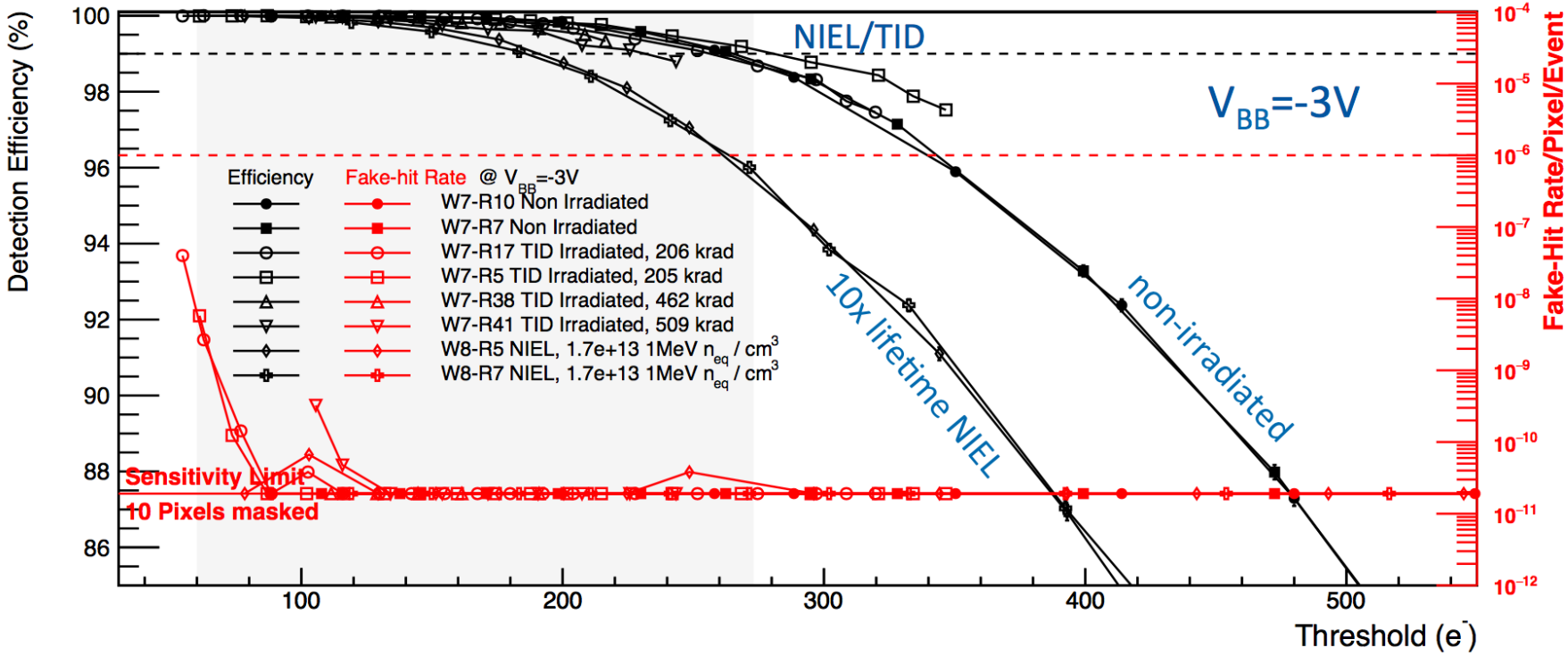




SEM pict
ALPIDE cros

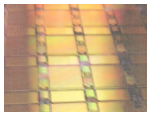
ALPIDE Chip Performance





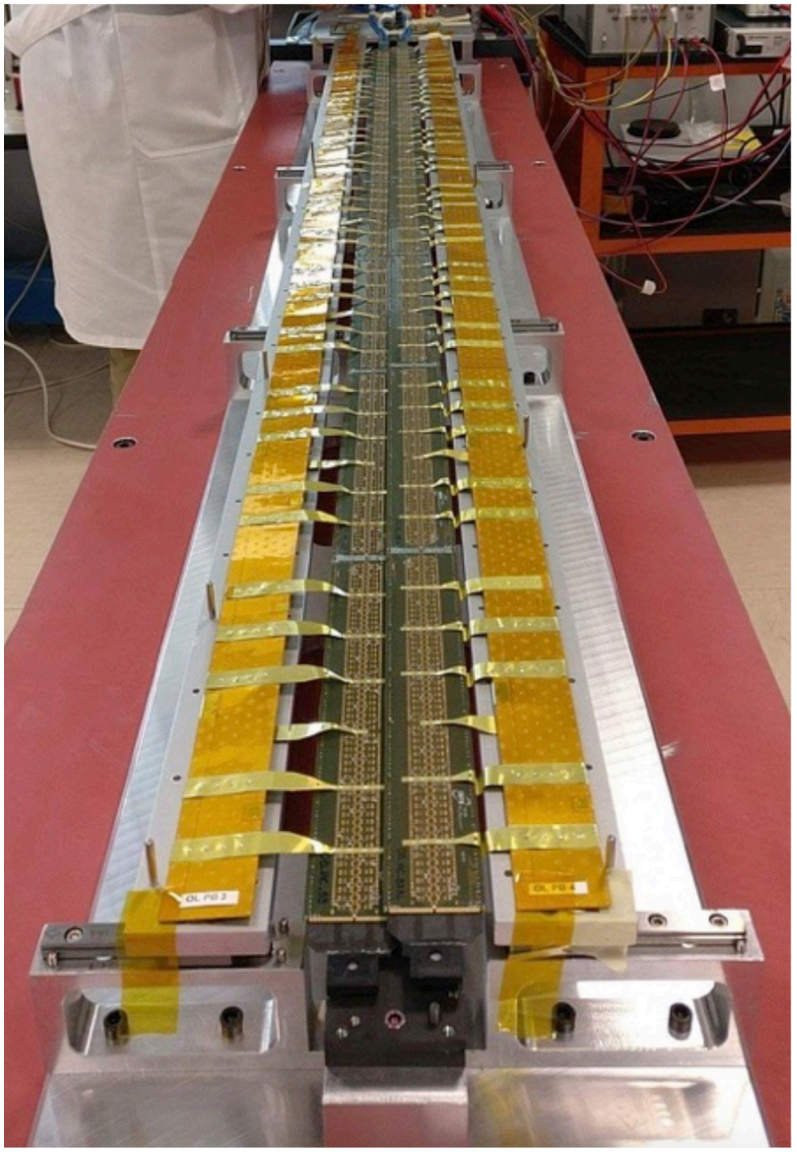
- Large operational margin before and after irradiation up to 10 x lifetime NIEL
- Chip-to-chip fluctuations negligible
- Fake hit rate << 10^{-5}

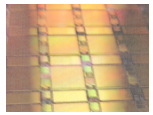
ALICE ITS upgrade



- Production ongoing with installation during LHC LS2.
- Very light weight design with 0.3% X_0 in the innermost layers and 0.8% X_0 in the outer layers.
- Largest area pixel detector based on monolithic pixels (MAPS) produced so far.

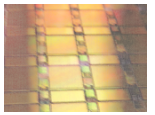
Picture: one outer barrel stave with ~ 100 M pixels





Future developments

Challenges for the Future



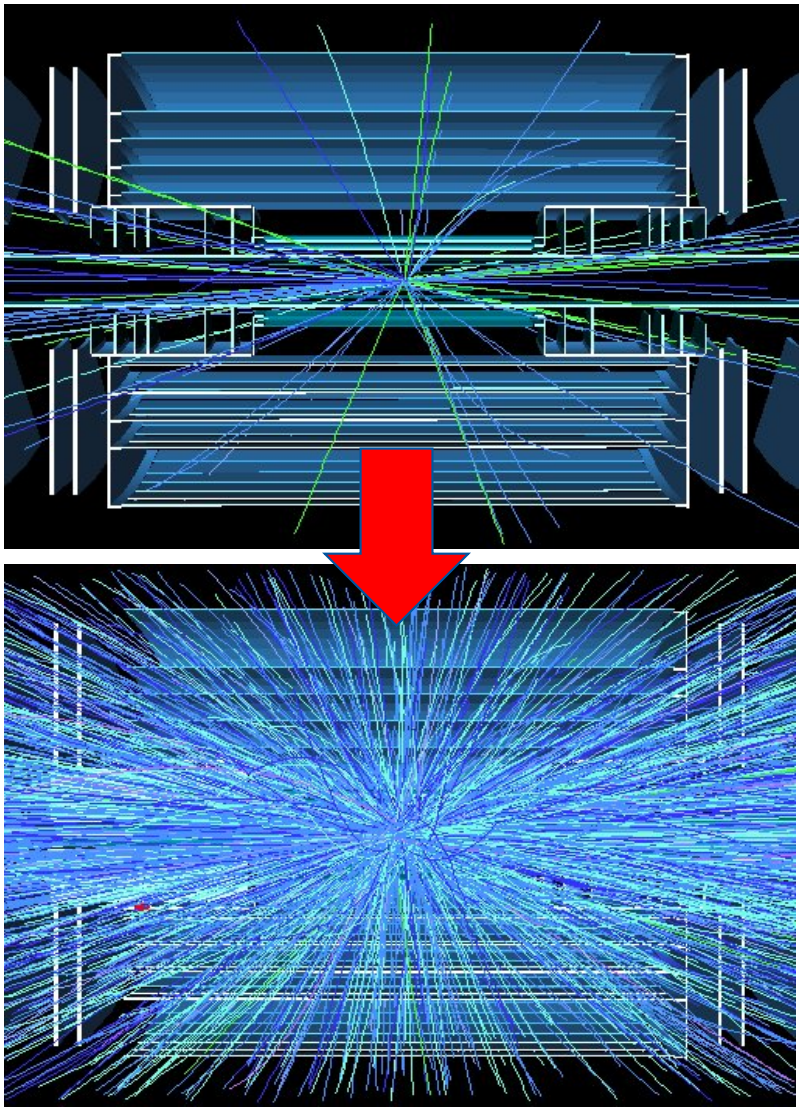
Increased luminosity requires

- Higher hit-rate capability
- Higher segmentation
- Higher radiation hardness
- Lighter detectors

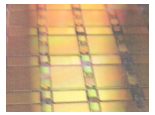
Radiation hardness improvement compared to now

- Phase-2 approx. factor 10-30

Can MAPS be ready for this environment?



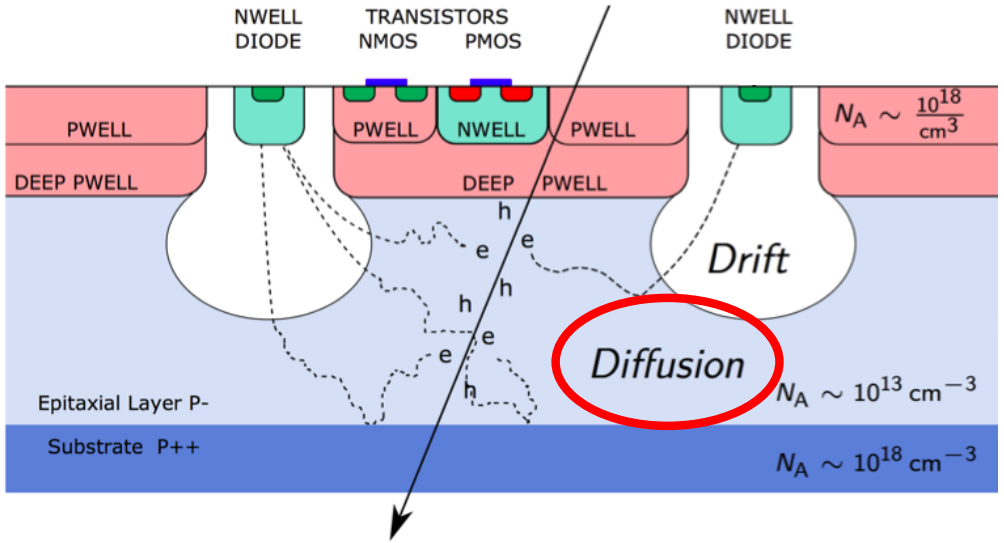
MAPS in Future Experiments



Present MAPS offer a number of very interesting advantages, but the diffusion is a limiting factor.

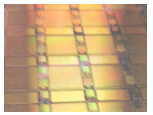
In a (very) high radiation environment (10^{15}-10^{16} n_{eq}/cm^2):

- The ionization charge is trapped/recombined in the non-depleted part → no more signal.
- Diffusion makes signal collection slower than typical requirements for pp-colliders.



Readout architectures are low power, but not designed for high rates like p-p at LHC.

CMOS for Future Trackers



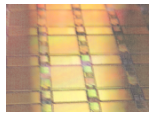
	ALICE ITS	ATLAS Outer Pixel	ATLAS Inner Pixel
NIEL [n_{eq}/cm^2]	10^{13}	10^{15}	10^{16}
TID	<1Mrad	80 Mrad	2x500Mrad
Response Time [ns]	2000	25	25
Hit rate [MHz/cm^2]	10 + SF	100-200	2000

Key parameters need factor up to ~100 Performance gain

H. Pernegger, HSTD11, Okinawa, 2017

- **Collect signal by drift through fully depleted sensor (DMAPS)**:
- **Dedicated designs** for high hit rates and fast response
  - New architecture developments to cope with high hit rates
- **CMOS** sensor post processing and **module integration**
  - Large area module concept and new interconnects technology for dedicated CMOS modules

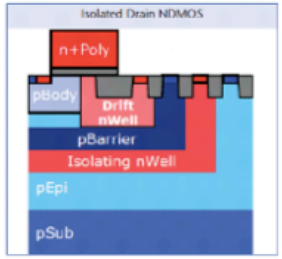
MAPS for the Future



Different types of MAPS are under study, with the aim to achieve radiation hardness through depletion, high rate capability, low power, …..

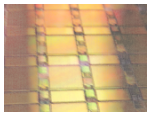
Enabling technologies are now available, which were not there some years ago ,e.g.:

"High" Voltage add-ons	Special processing add-ons (from automotive and power management applications) **increase the voltage handling capability** and create a depletion layer in a well's pn-junction of o(10-15 µm).
"High" Resistive Wafers	8" hi/mid **resistivity** silicon wafers accepted/qualified by the foundry. Create depletion layer due the high resistivity.
Technology features (130-180 nm)	Radiation hard processes with **multiple nested wells.** Foundry must accept some process/DRC changes in order to optimize the design for HEP.
Backside Processing	Wafer thinning from backside and backside implant to fabricate a **backside contact** after CMOS processing.



from: www.xfab.com

Depletion and Fill Factor



To better **deplete the active volume**:

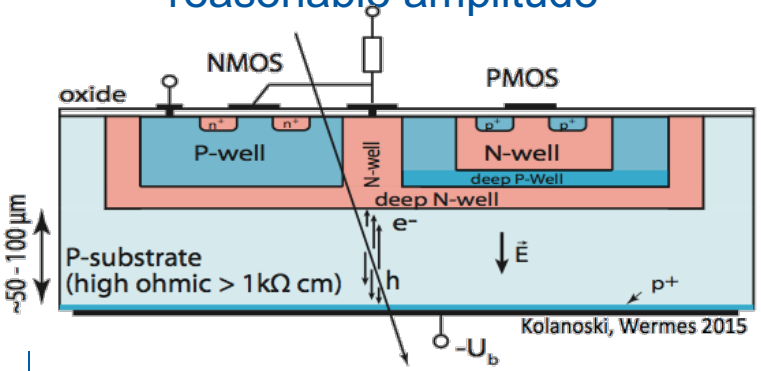
- Use high resistivity (epi) wafers (~kOhmcm)
- Apply bias voltage

$$d \propto \sqrt{\rho V}$$

The **fill factor** will affect how the depletion region grows:

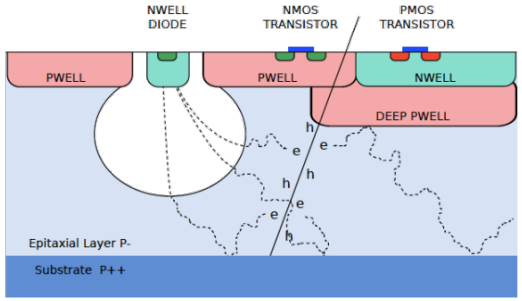
Large fill factor

- Uniform charge collection
- Large capacitance (~50-200 fF) on CSA
- More power necessary to achieve fast signals with reasonable amplitude



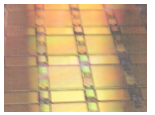
Small fill factor

- Higher gain and faster response due to smaller capacitance (2-5fF) and higher Q/C
- Potentially lower power consumption
- Signal collection under DPW after irradiation more difficult on edges



Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

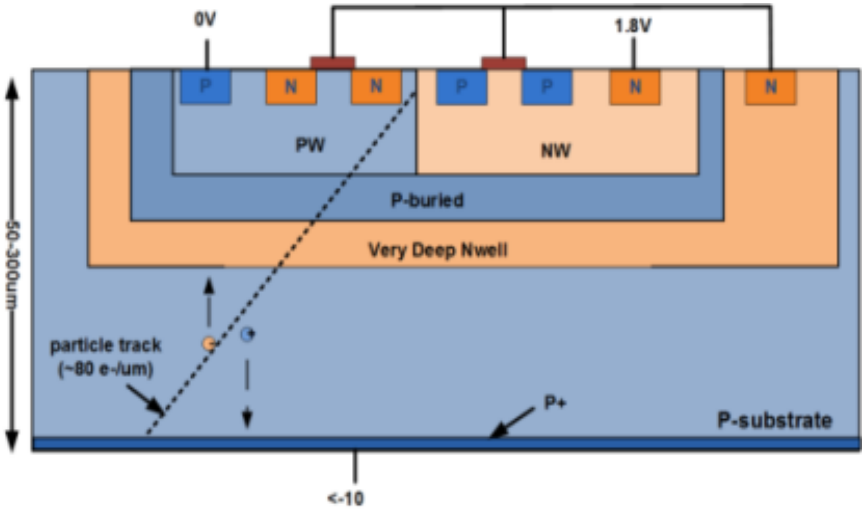
Examples: Large Fill Factor

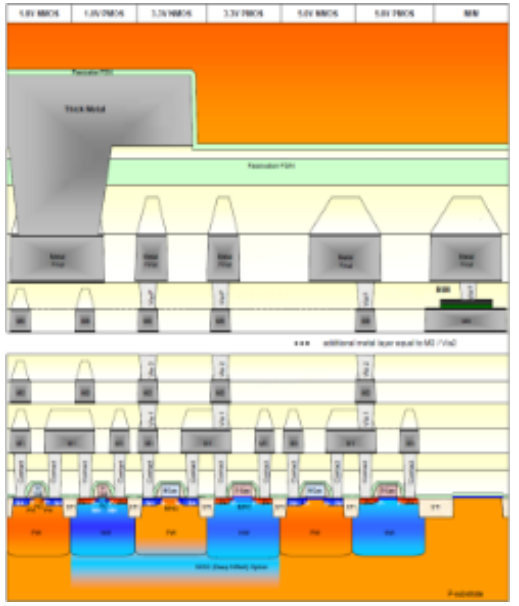


An example of large electrode pixel sensors are the development lines in the LFoundry and in AMS processes.

LFoundry:

- L-Foundry 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- Resistivity of wafer: **>2000 Ω·cm**
- Small implant customization
- Backside processing

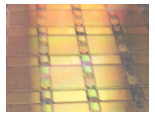




P. Rymaszewski et al., JINST 11 (2016) 02 C02045
T. Hirono et al., doi:10.1016/j.nima.2016.01.088

universitätbonn

LFoundry Development Line



CCPD_LF

- Subm. in Sep. 2014
- 33 x 125 µm^2 pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test
- ***(Almost) Fully characterized***

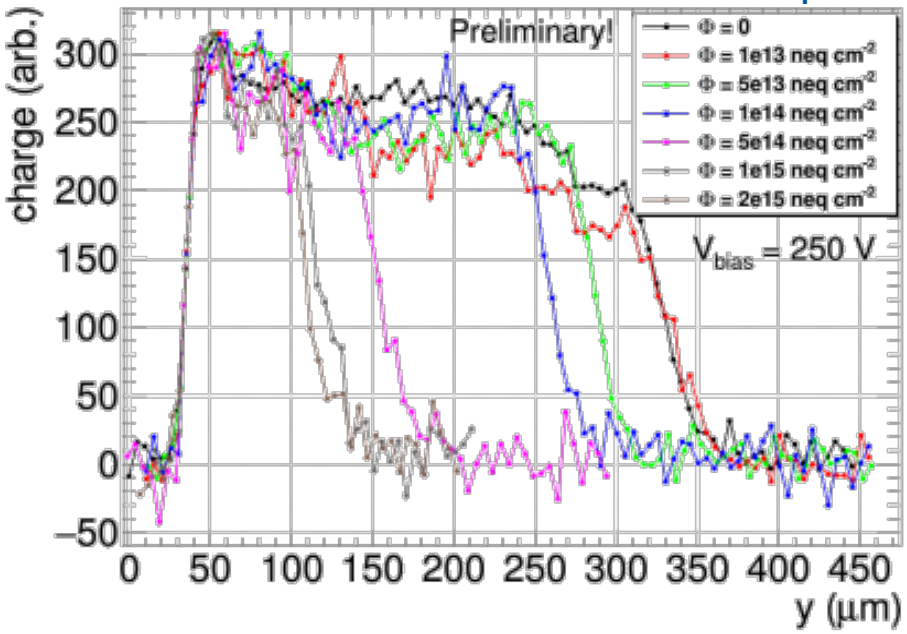
LF-CPIX (DEMO)

- Subm. in Mar. 2016
- ***CPIX demonstrator in LF***
- 50 x 250 µm^2 pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test
- ***First meas. available***

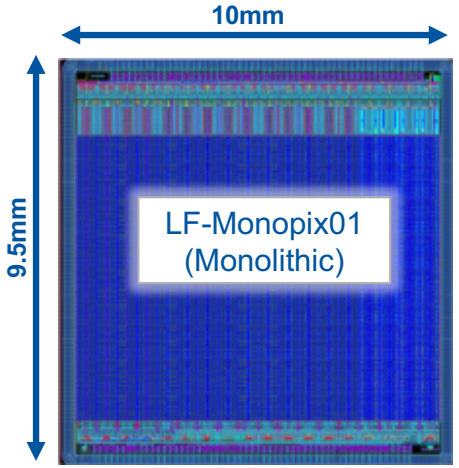
LF-Monopix01 (monolithic)

- Subm. in Aug. 2016
- "Demonstrator size"
- 50 x 250 µm^2 pixels
- ***Fast standalone R/O***
- Standalone R/O like LF-CPIX

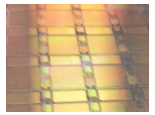
Edge TCT on neutron irradiated CPIX sensors up to 2x10^{15} neq/cm^2



I. Mandic, B. Hiti (Ljubljana)



AMS Development Line



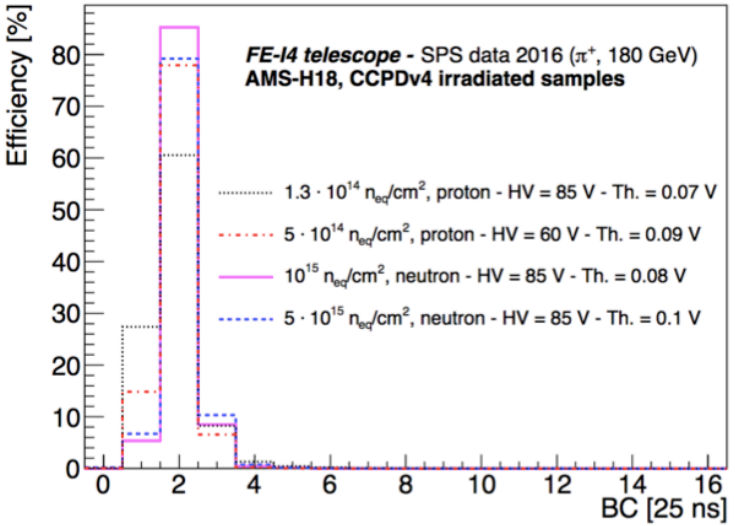
Capacitively Coupled Pixel Detectors (H18 AMS process)

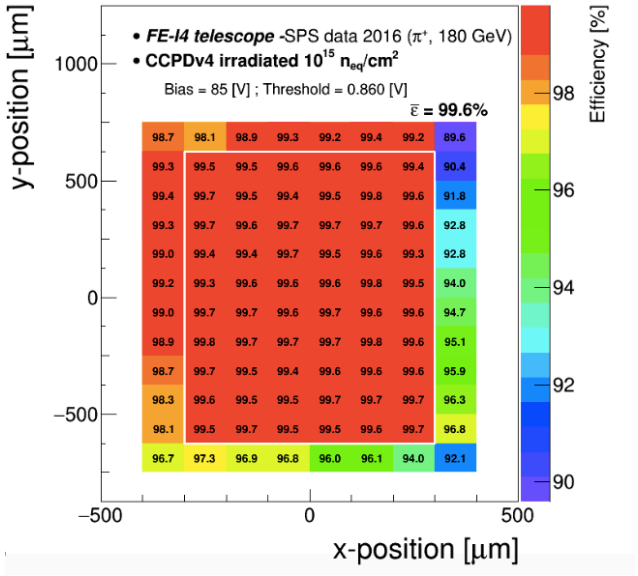
- Capacitive-Coupling of CMOS sensor to ATLAS FEI4 (sensor pixel size 33x 125um2)
- Blocks for monolithic design implemented an studied (DAC,Amplifier, Discriminators, Configuration)
- Efficiency of > 99.5%
- Signal collected in 3BC

T. Weston/ Uni Bern @ TREDI 2017
Mathieu Benoit / Uni Geneve

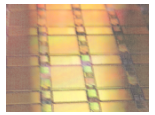
H18 CCPDv5

- First prototype in aH18 process (Hi-Resistivity wafer processing)
- Many beam tests carried out to test operation, tuning, achievable threshold and efficiency
  - 600-650e Threshold





Example: Small Fill Factor



Small input capacitance of few fF compared to hybrid pixels (O (100fF, IBL))* or large fill factor MAPS → beneficial for timing, noise and power!

1. Input capacitance drives peaking time and ENC → low input capacitance will reduce peaking time and ENC

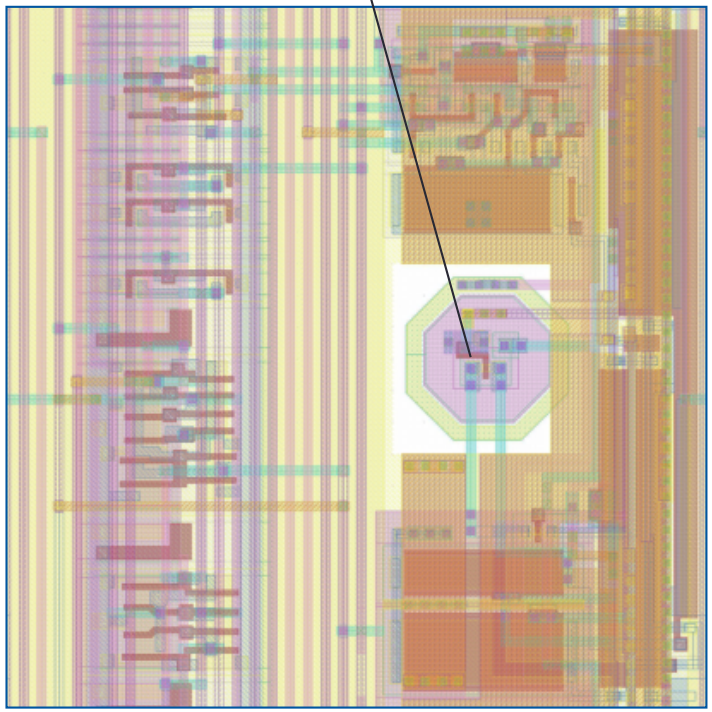
2. Analog power: depends on collected charge over capacitance Q/C in the pixel → optimize sensing node**

$$P \sim \left\{ \frac{S}{N} \frac{Q}{C} \right\}^{m} \quad with\ 2 \leq m \leq 4$$

But collection underneath deep p-Well is limited due to depletion limit…

Collection diode ~ 2-3 µm ø, C~ O(few fF)
27 µm x 29 µm pixel

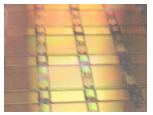
T. Kugathasan, W. Snoeys



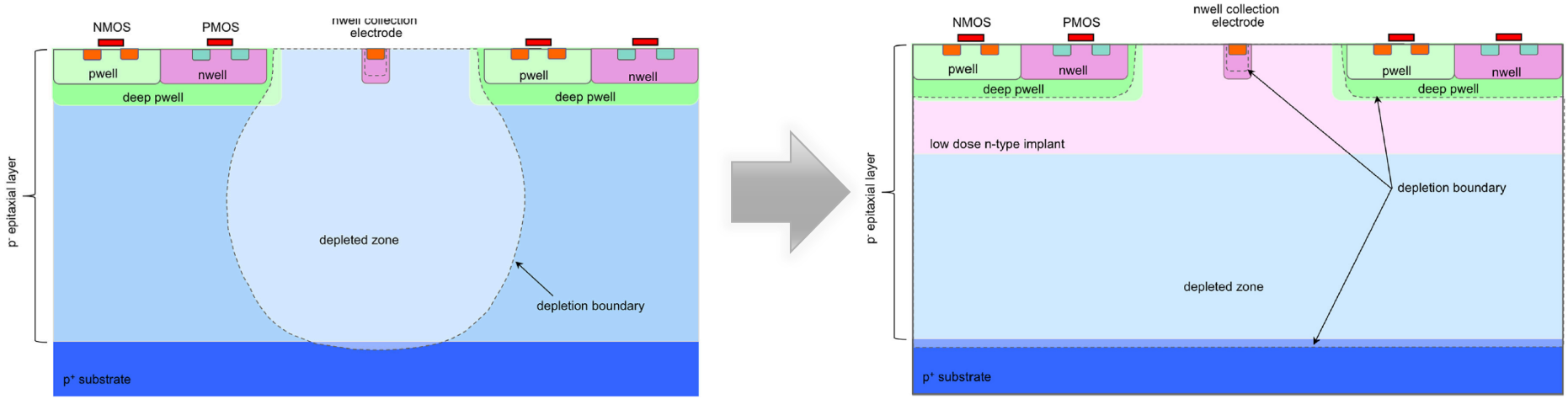
*Havranek et al, NIMA 714 (2013) 83-89

** W. Snoeys, NIM. A765 (2014) 167-171

TJ 180 nm modified process



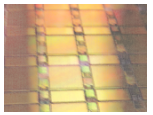
- Novel modified process developed in collaboration of CERN with TJ foundry, originally developed in context of ALICE ITS.
- Combined with a small collection diode.

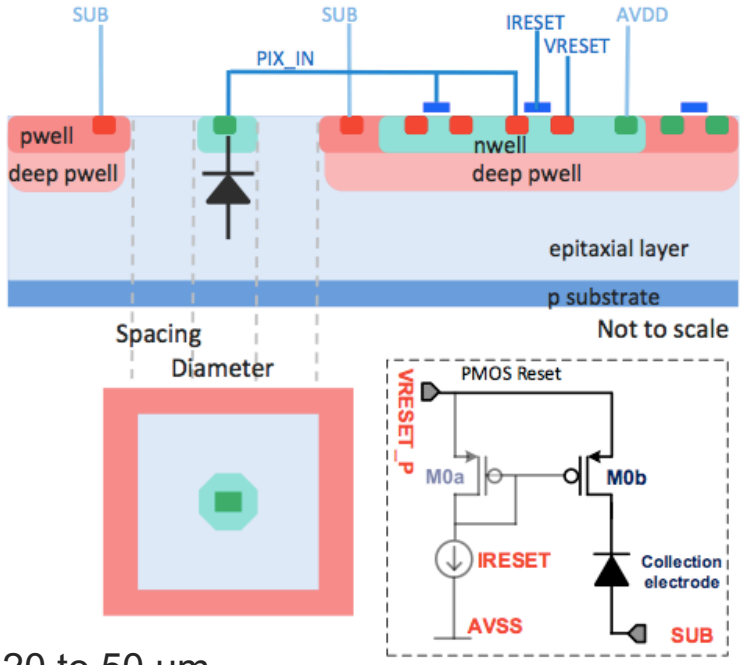


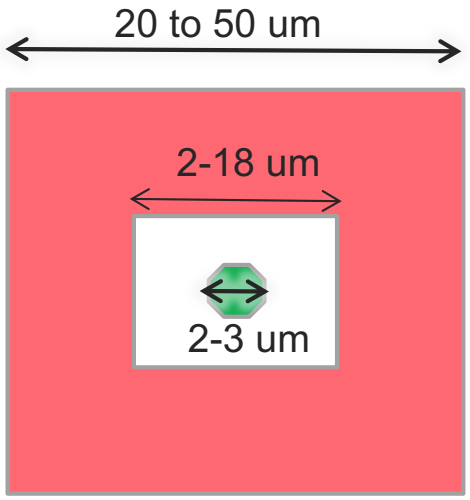
- Adding **a planar n-type layer** significantly improves depletion under deep PWELL
- Increased depletion volume → **fast charge collection by drift**
- better time resolution reduced probability of charge trapping (**radiation hardness**)
- Possibility to fully deplete sensing volume with no significant circuit or layout changes

W. Snoeys et al., NIM A871 (2017) 90 – 96.

TowerJazz 180nm Investigator







- **Pixel dimensions for the following measurements:**
- 20x20 to 50x50um^2 pixel size
- **3 um diameter electrodes** 25um EPI layer

Designed as part of the ALPIDE development for the ALICE ITS upgrade

Emphasis on small fill factor and small capacitance enables low analog power designs (and material reduction in consequence)

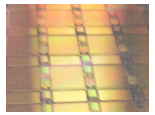
C. Gao et al., NIM A (2016) 831
http://www.sciencedirect.com/science/article/pii/S0168900216300985

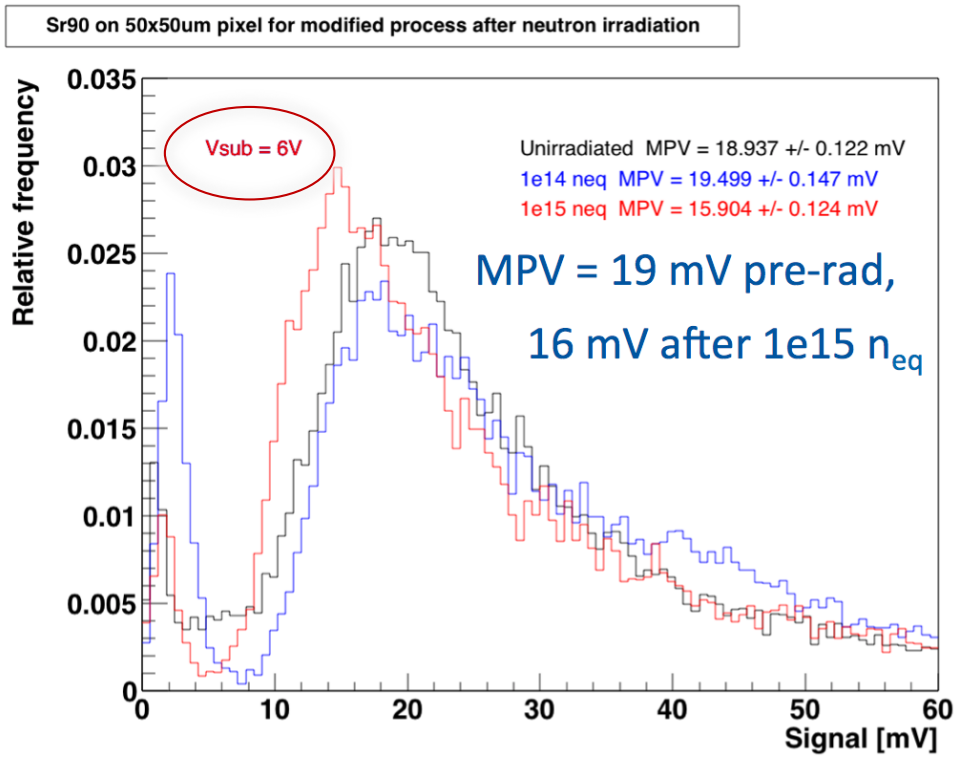
J. Van Hoorne, proceedings of NSS2016
http://2016.nss-mic.org/nss.php

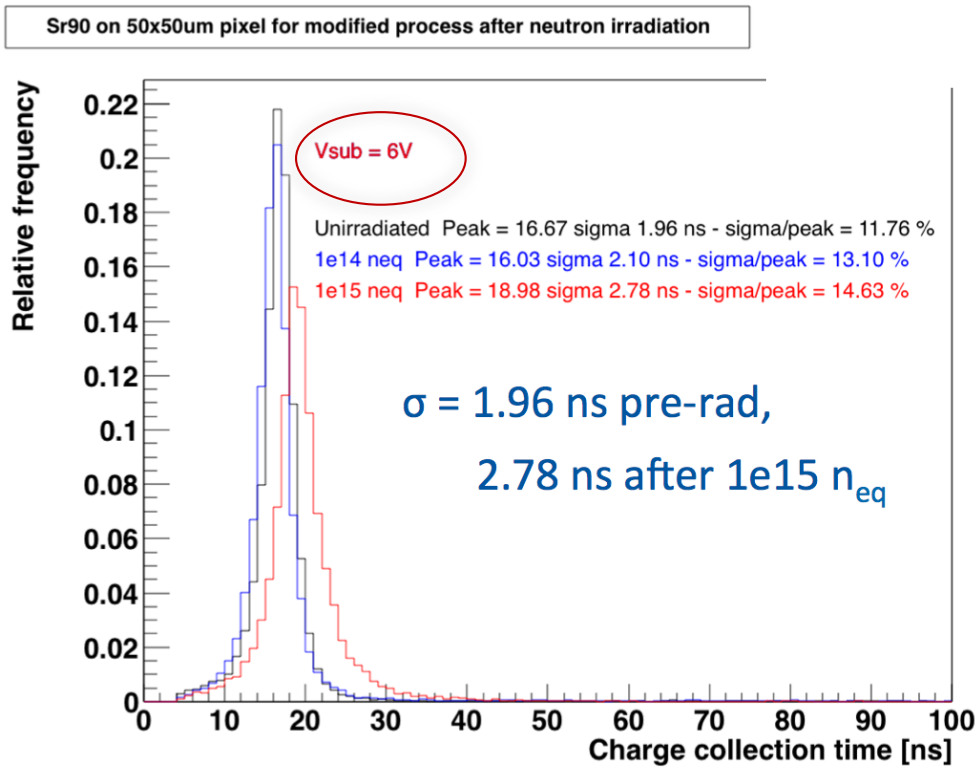
Produced in TowerJazz 180nm on 25-30um thick epi layer in the modified process

Design: C. Gao, P. Yang, C. Marin Tobon, J. Rousset, T. Kugathasan and W. Snoeys

After 10^{15} n_{eq}/cm^2 and 1Mrad TID

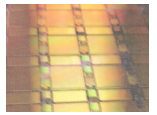






Very little signal loss after 10^{15}, also very encouraging results on detection efficiency.
Signal well separated from noise.
Measurements on samples irradiated to 10^{16} n_{eq}/cm^2 ongoing.

H. Pernegger, Terascale Detector Workshop, DESY, April 2017

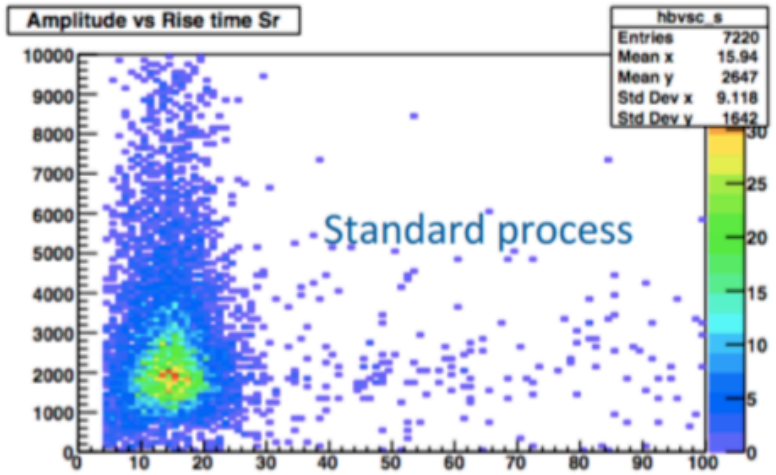


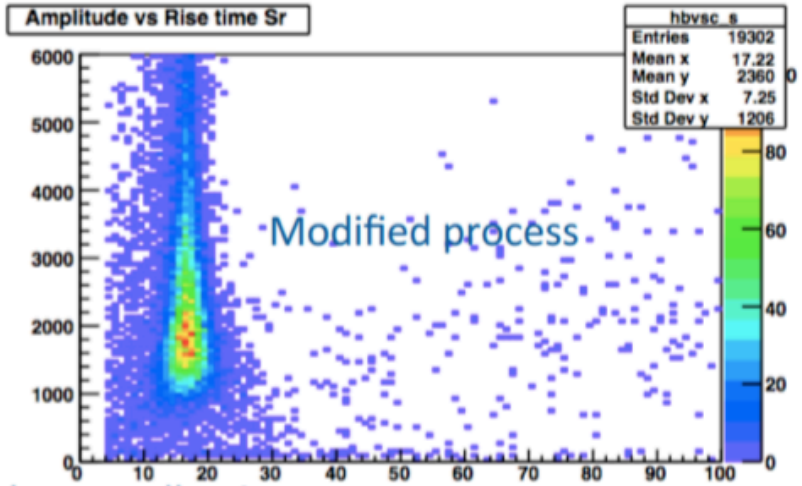
Charge versus collection time

- Calibrated charge signal in ^{90}Sr source tests
  - Calibration of mV to e- by ^{55}Fe source tests

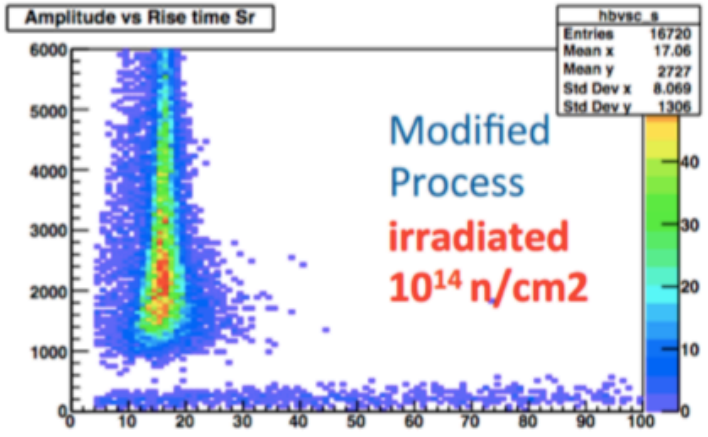
H. Pernegger, Terascale Detector Workshop, DESY, April 2017

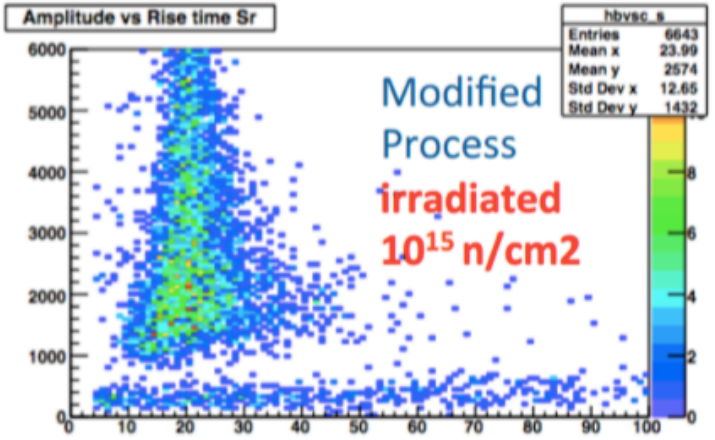
- Better timing with modified process (narrower collection time distribution)



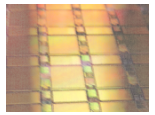


- Modified process after irradiation maintains charge collection

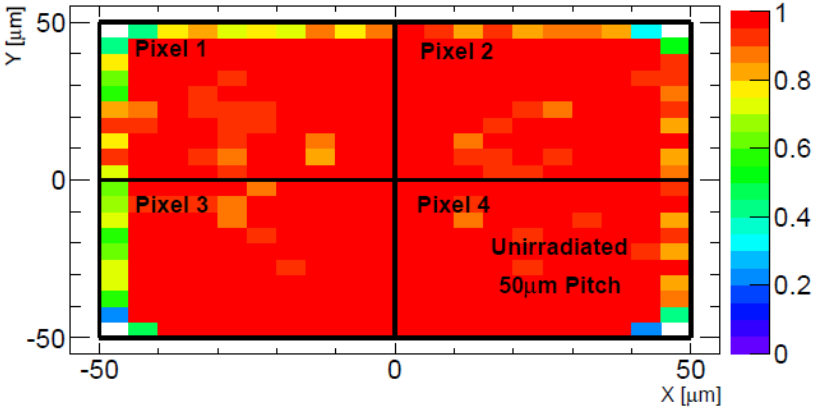


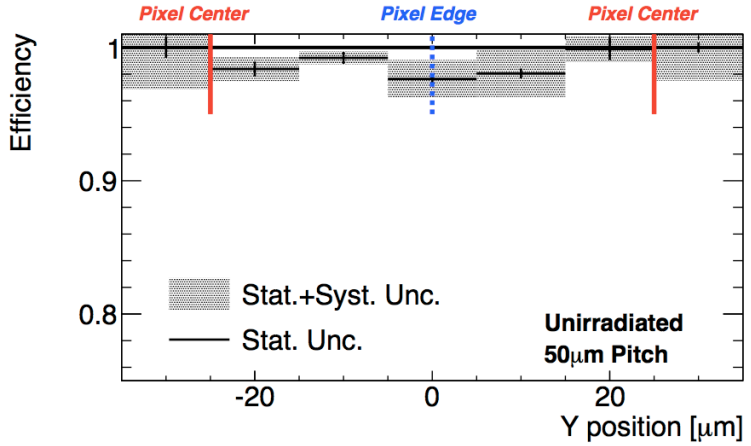


Beam test results

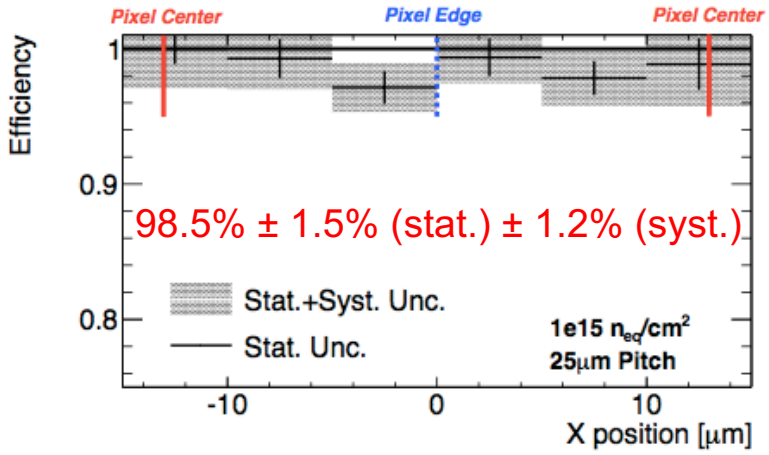


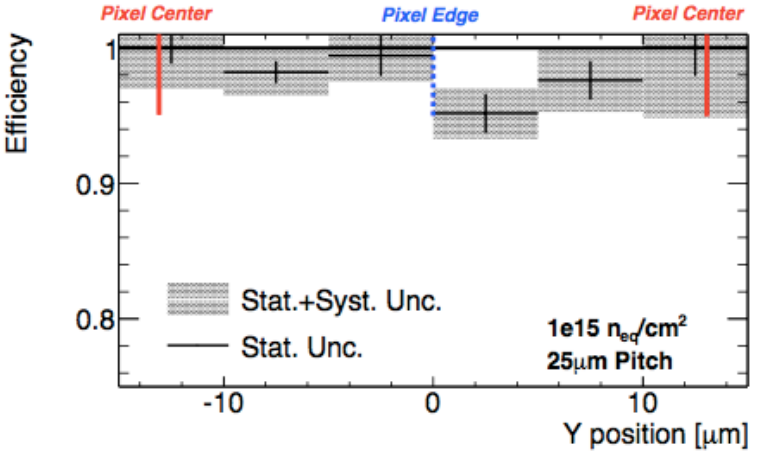
- Unirradiated sensor efficiency 98.5% ± 0.5% (stat.) ± 0.5% (sys.) (50x50 μm²)





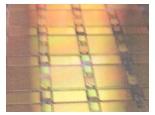
- Irradiated sensor also shows uniform efficiency across 25x25 μm² pixel





H. Pernegger, Terascale Detector Workshop, DESY, April 2017

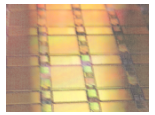
Monolithics for the future



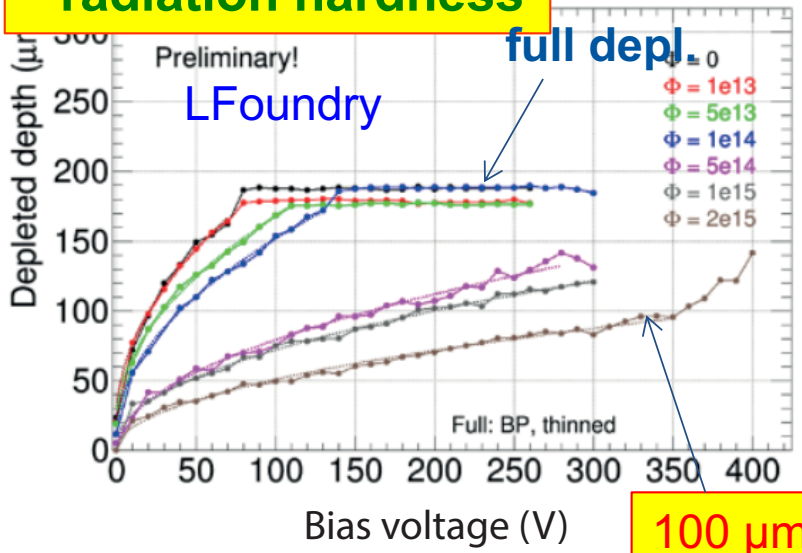
- Very encouraging results from the different development lines (large and small fill factor designs, different starting materials, etc…)

- Testing of key parameters:
  - Radiation hardness
  - Timing
  - Efficiency

Results extremely encouraging



• radiation hardness

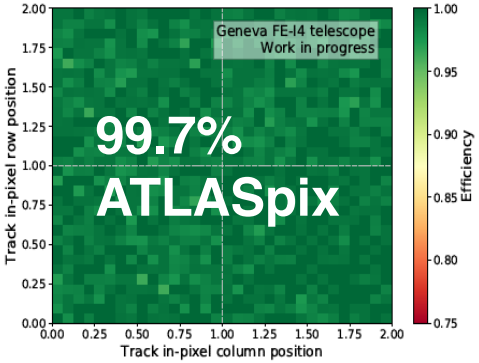


100 µm after 2×10^{15}

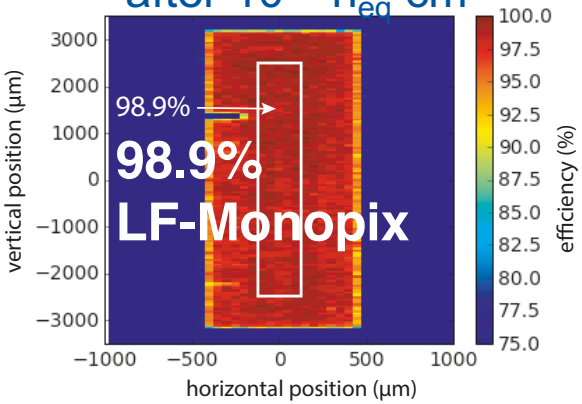
I. Mandić et al., JINST 12 (2017) no.02, P02021

• efficiency

before irrad



after 10^{15} n_{eq} cm^{-2}

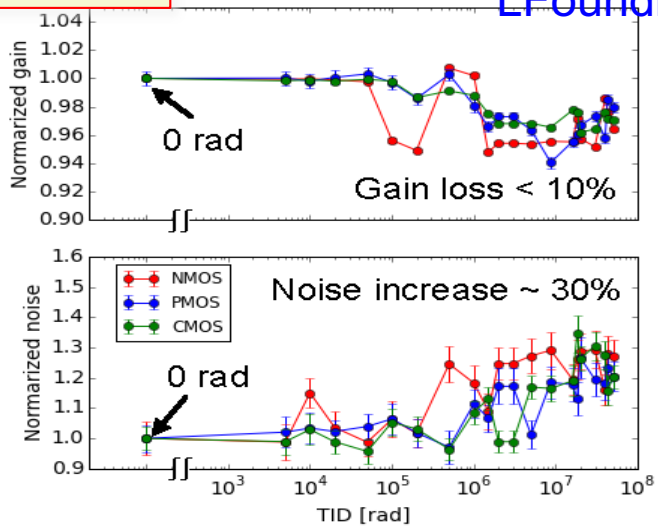


TID 1 MGy

LFoundry

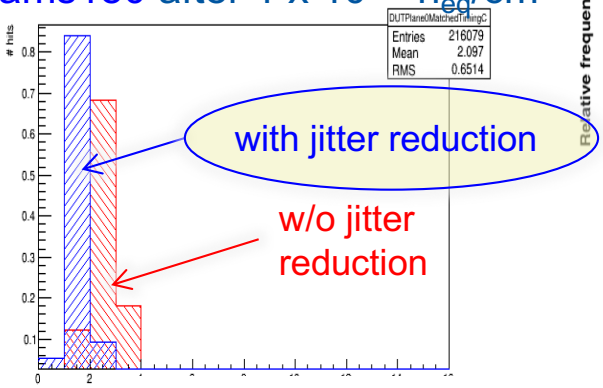
gain

noise

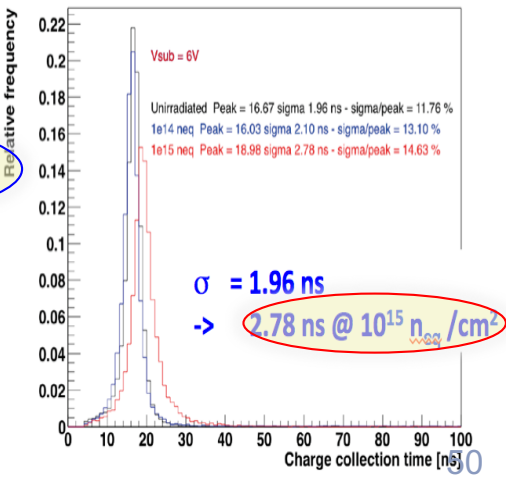


• timing

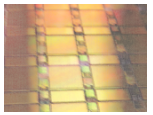
ams180 after 1 x 10^{15} n_{eq}/cm^2



TowerJazz (small fill factor)

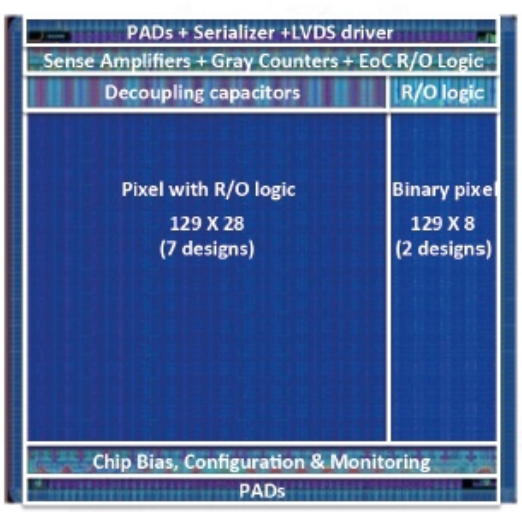


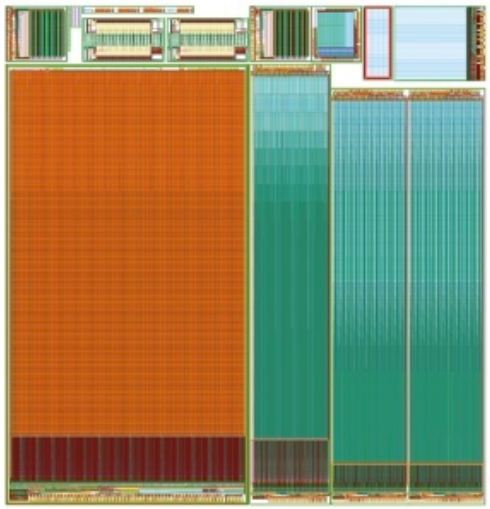
N. Wermes, HSTD11, Okinawa, 2017

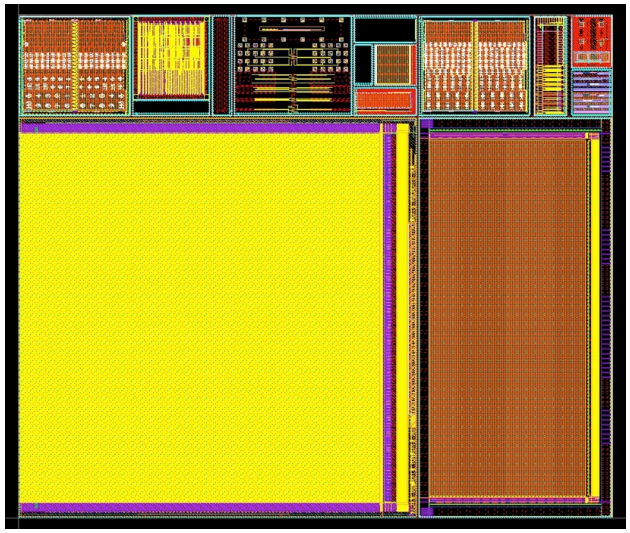


…to large size Chips

- Following the encouraging results obtained from test chips, larger size chips (O(cm^2) have been designed and processed.
- **These chips are available for module assembly!**



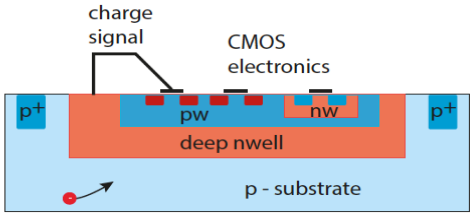




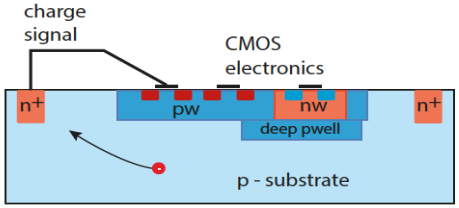
LFoundry 150 nm
substrate ρ > 2 kΩcm

ams 180 nm
substrate ρ ~ 0.08 - 1 kΩcm

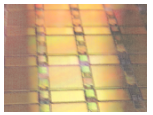
TowerJazz 180 nm epitaxial (25 µm)
substrate ρ > kΩ cm



(a) Large fill-factor

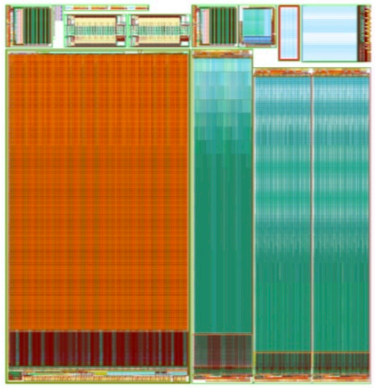


(b) Small fill-factor



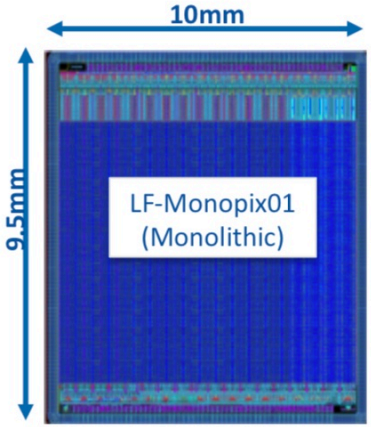
Chip name	Technology	CE Size*	Pixel size [µm²]	R/O architecture	Staust
aH18	AMS 180nm	Large	56 × 56	Asynchronous	Measurements
Malta	TowerJazz 180nm	Small	36 × 36	Asynchronous	Submitted Back after Xmas
TJ Monopix		Small	36 × 40	Synchronous	
LF Monopix	LFoundry 150 nm	Large	50 × 250	Synchronous	Measurements
Coolpix		Large	50 × 250	Synchronous	
LF2		Large	50 × 50	Synchronous	

* CE Size = Collection Electrode Size



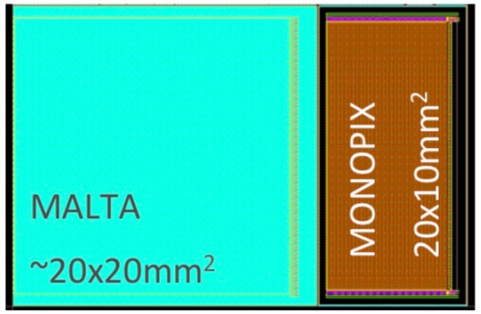
ATLAS Pix & MuPix

AMS 180 nm



MONOPIX, LF2 & COOLPIX

Lfoundry 150 nm

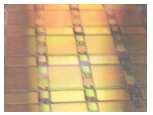


MONOPIX & MALTA

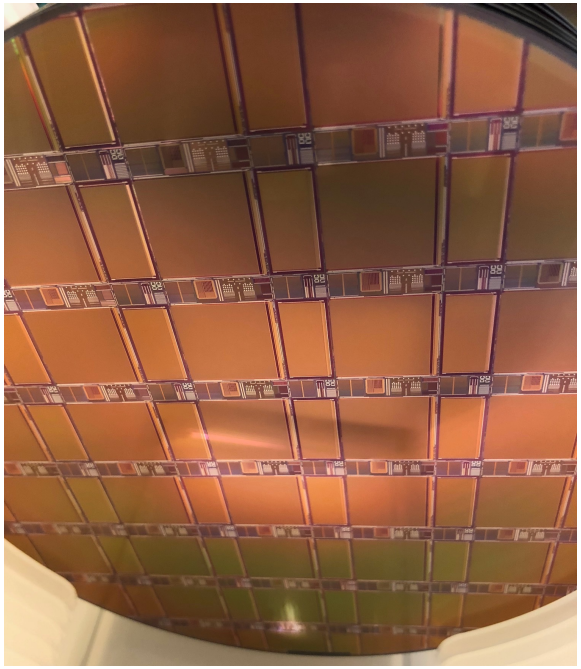
TowerJazz 180 nm

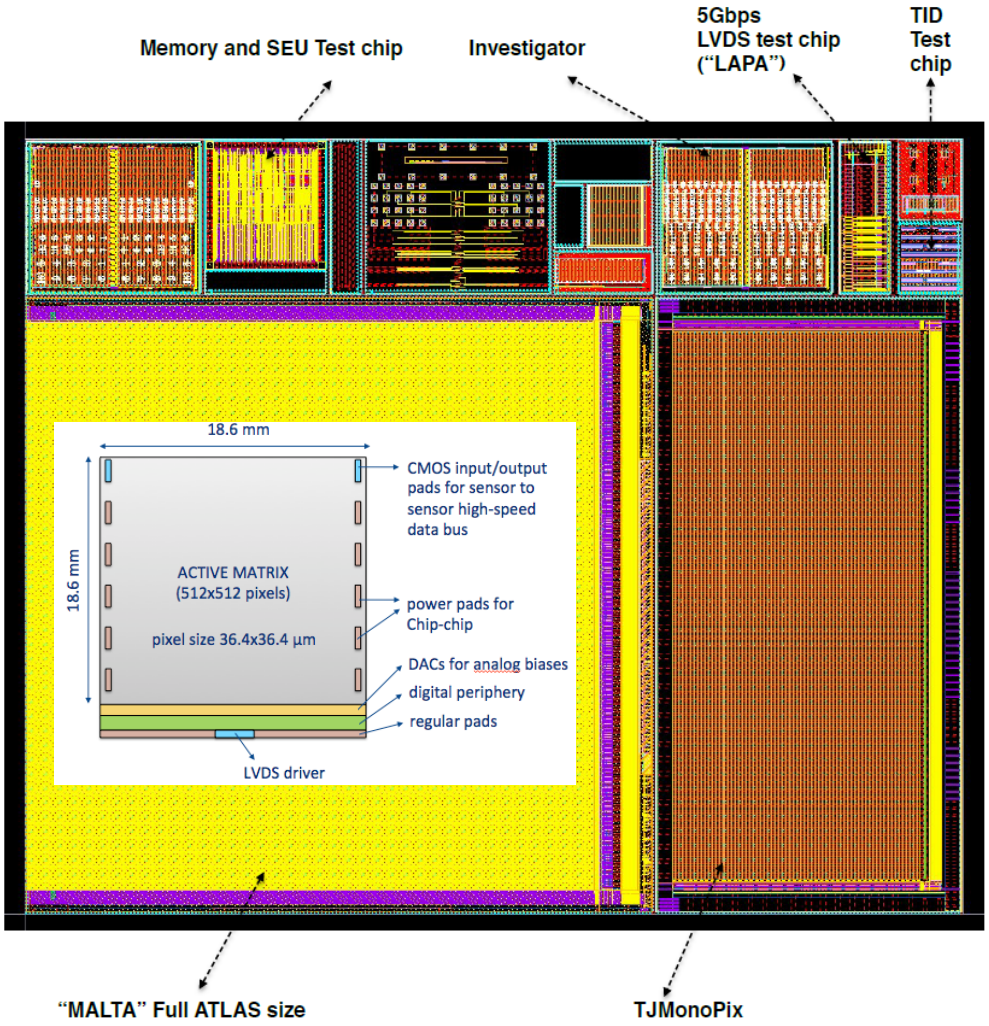
W. Snoeys, HSTD11, Okinawa, 2017

Example: MALTA & MONOPIX

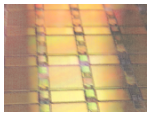


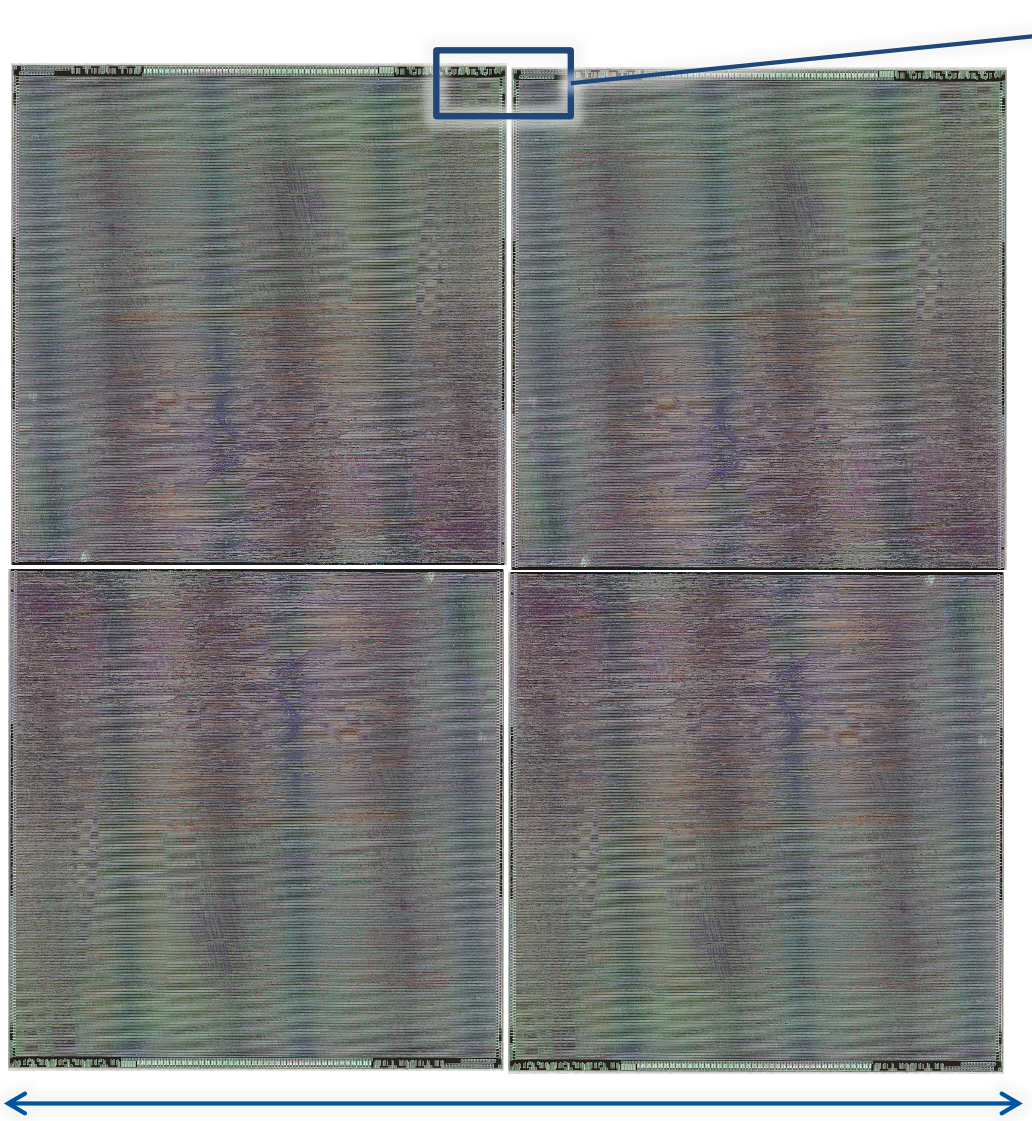
- Uses TJ180nm modified process
- **Full-scale demonstrators** with different readout architectures and optimized analog performance
  - MALTA: 20x22 mm^2 (full size)
  - MonoPix : 20x10 mm^2 (half size)



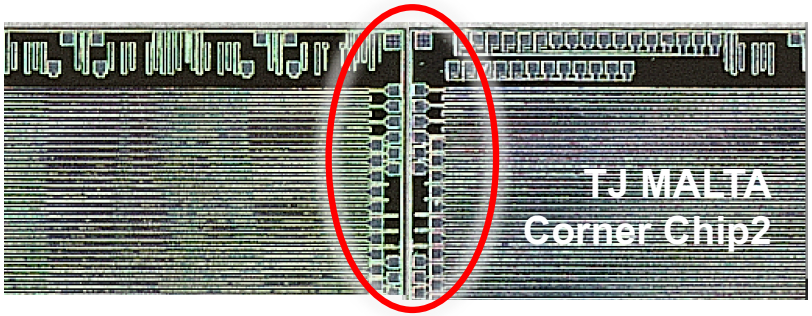


MALTA Module





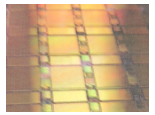
Chip-to-Chip data interconnection



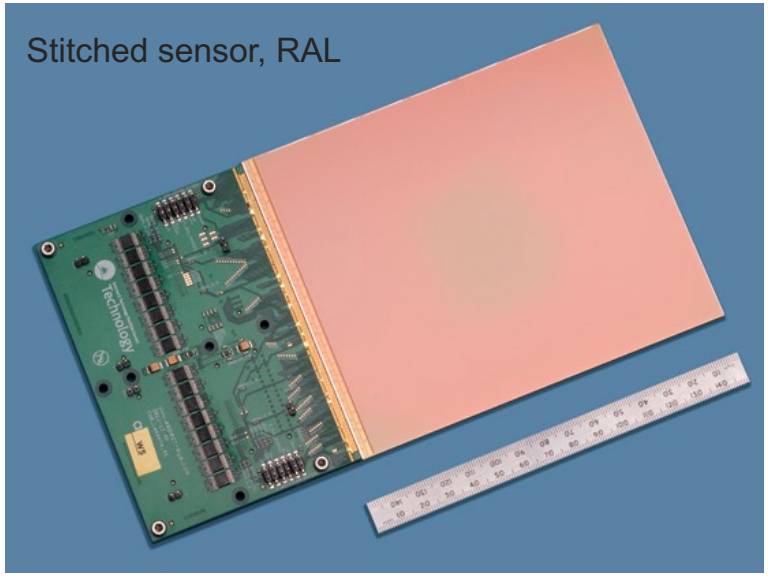
- Modules consisting of 4 MALTA chips (activity starting)
- Compatible with ATLAS Itk pixel module
- Use chip-to-chip connection pads to transfer data from one chip to the next

H. Pernegger, HSTD11, Okinawa, 2017

Module Building



- Typical chip sizes O(few cm^2) → not ideal for covering large surfaces O(10s of m^2)
- **Need larger chips and new assembly technologies to build low cost large area module**
- Explore CMOS options such as, e.g.:
  - Stitching
  - RDL to enable chip-to-chip connections for power and data
  - Pad over logic, etc.

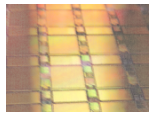


And if it would be flexible?

http://image-sensors-world.blogspot.fr/2014/06/

Cylindrically Curved CCD (Convex)

Summary



- Monolithic pixel detectors are being studied intensively for their use in HEP experiments. They provide potentially low cost high precision tracking sensors.

- Many different versions are under study, tackling the issues to make such detectors suitable for high radiation and high rate environments.

- Several experiments (ALICE, BELLE II, STAR) have chosen monolithic pixels for their upgrade.